

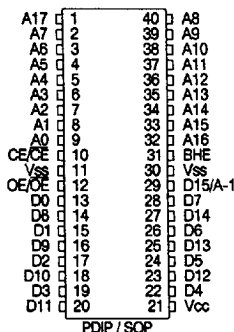
DESCRIPTION

The HY234100 is a 4Mbit mask-programmable ROM organized either as 524,288 x 8bit (Byte mode) or as 262,144 x 16bit (Word mode) depending on BHE level. It is fabricated using HYUNDAI's advanced CMOS process technology. The HY234100 operates with a 5V power supply and all inputs are TTL compatible. It satisfies user option modes with the polarity-programmable $\overline{CE}$ and $\overline{OE}$. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

FEATURES

- High speed- 120ns
- User-Switchable x8 / x16 Organization
- Single 5V $\pm$ 10% Power Supply
- Power Consumption (max.)
 - Operating : 40mA
 - Standby (CMOS) : 50 μ A
- Fully Static Operation
- Polarity-Programmable Pins
 - $\overline{CE}/\overline{CE}^*$, $\overline{OE}/\overline{OE}^*$
- TTL compatible inputs and outputs
- Tri-state output
- Packages :
 - 40 pin 600 mil PDIP
 - 40 pin 525 mil SOP

PIN CONNECTION

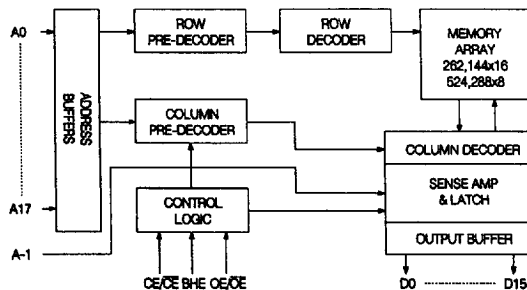


PIN DESCRIPTION

Pin Name	Pin Function
A0-A17	Address Inputs
D0-D15	Data Outputs
BHE	Byte/Word select
D15/A-1	Output D15 (Word mode)/ LSB Address (Byte mode)
$\overline{CE}/\overline{CE}^*$	Chip Enable
$\overline{OE}/\overline{OE}^*$	Output Enable
Vcc	Power
Vss	Ground

* User Selectable Polarity

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TBIAS	Temperature under BIAS	-10 to 85	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN	Voltage on Any Pin Relative to Vss	-0.3 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-0.3 to 7.0	V

Note:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C, Vcc= 5V ± 10%, Vss=0V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.2	-	Vcc + 0.5	V
VIL	Input Low Voltage	-0.5	-	0.8	V

TRUTH TABLE

MODE	CE/CE	OE/OE	BHE	D15/A-1	DATA	OPERATION
Non-Selected	L/H	X	X	X	High-Z	Standby
Output Disabled	H/L	L/H	X	X	High-Z	Active
Read	H/L	H/L	H	Output	D0-D15	Active
			L	Input	D8-D15 : High-Z	Active

Note: X=L or H

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V± 10%, V_{SS}=0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 to V _{CC}	-	10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0 to V _{CC}	-	10	μA
I _{CC}	Operating Current	ALL DOUT = open, f = 8.3MHz, CE = $\overline{OE}$ = V _{IL}	-	40	mA
		ALL DOUT = open, f = 1.0MHz, CE = $\overline{OE}$ = V _{IL}	-	20	mA
I _{SB1}	Standby Current (TTL)	$\overline{CE}$ = V _{IH} , ALL DOUT = open	-	1	mA
I _{SB2}	Standby Current (CMOS)	$\overline{CE}$ = V _{CC} , ALL DOUT = open	-	50	μA
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -1mA	2.4	-	V

Note: All Voltages are referenced to V_{SS}

AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V ±10%, unless otherwise noted.)

#	SYMBOL	PARAMETER	120		150		200		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	tRC	Read Cycle Time	120	-	150	-	200	-	ns
2	tACC	Address Access Time	-	120	-	150	-	200	ns
3	tOH	Output Hold from Address Change	0	-	0	-	0	-	ns
4	tCE	Chip Enable Access Time	-	120	-	150	-	200	ns
5	tOE	Output Enable Access Time	-	60	-	70	-	80	ns
6	tDF	Output or Chip Disable to Output High-Z	-	20	-	20	-	20	ns

AC TEST CONDITIONS

(TA=0°C to 70°C, VCC=5V ±10%)

PARAMETER	VALUE
Input Pulse Level	0.6 to 2.4V
Input Rise and Fall Time	10ns
Input/Output Timing Level	0.8V and 2.0V
Output Load	1TTL Gate and CL = 100pF

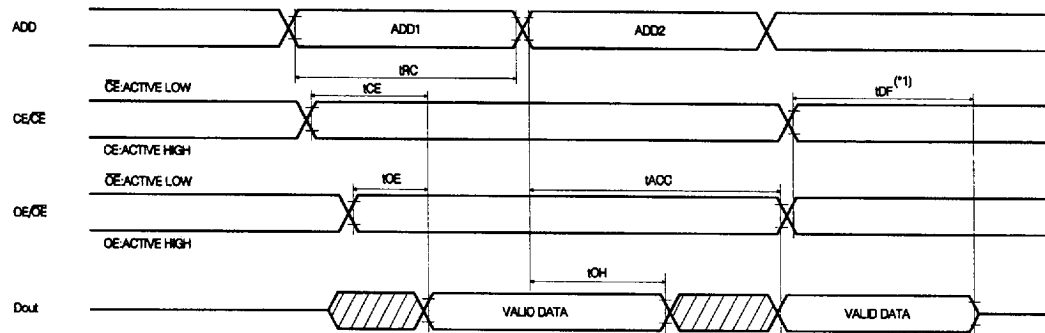
CAPACITANCE

(TA=25°C, f=1MHz, VCC=5V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	TYPE	MAX.	UNIT
CIN	Input Capacitance	VIN = 0V	-	15	pF
COUT	Output Capacitance	VOUT = 0V	-	15	pF

TIMING DIAGRAM

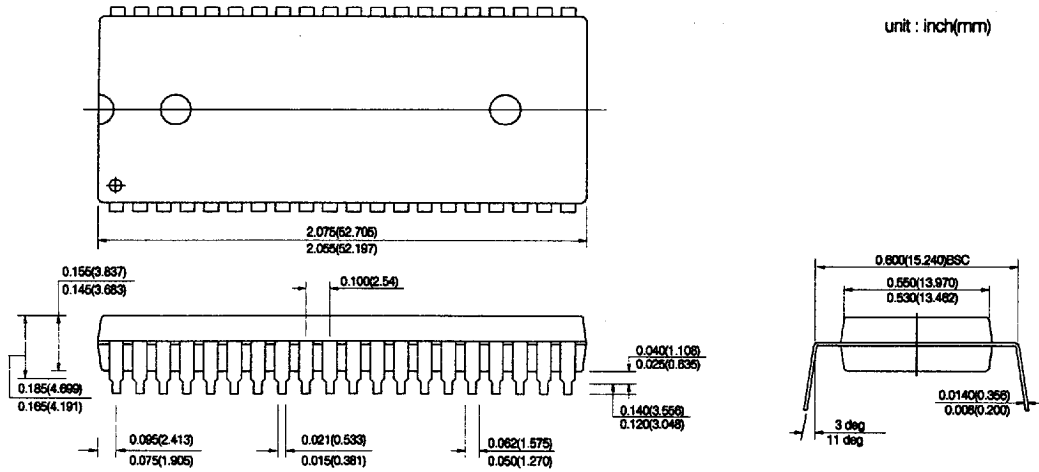
READ CYCLE



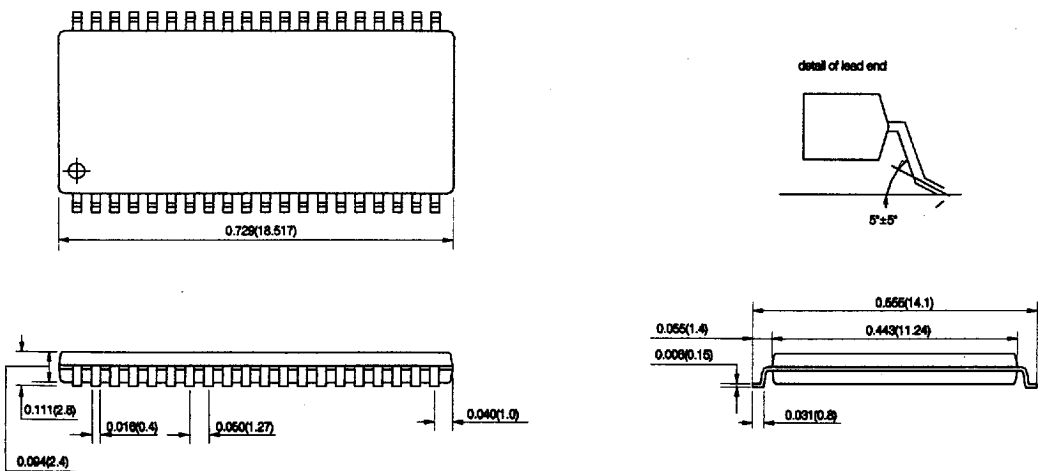
(*1) tDF is defined as the time which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} Level.

PACKAGE INFORMATION

40 Pin Plastic Dual In-Line Package - 600mil (P)



40 Pin Plastic Small Outline Package - 525mil (G)



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ORDERING INFORMATION

PART NO	SPEED	PACKAGE
HY234100P-XXX	120/150/200 ns	PDIP
HY234100G-XXX	120/150/200 ns	SOP