silicon systems®
A TDK Group Company

SSI 78Q2121
100Base-TX
Fast Ethernet Transceiver
Preliminary Data

March 1996

DESCRIPTION

The SSI 78Q2121 is a 100Base-TX Fast Ethernet transceiver with integrated transmit and clock recovery PLLs. The device interfaces directly to the DEC 21140 controller chip and alike, which has integrated 100Base-TX PCS functions, through a 15-bit 5B symbol interface. The transmitter includes on-chip pulse-shaper and a low power line driver, while the receiver has a sophisticated combination of AGC, real-time adaptive equalizer, and adaptive DC offset adjustment circuit to provide the best combination of ISI cancellation and baseline wander correction required for accurate clock and data recovery. The transceiver is used at the interface to Cat 5 UTP cabling, and is connected to the line media via simple 1:1 isolation transformers. No external filter is required.

The 78Q2121 is built in BiCMOS technology for high performance and low power operation, and can operate from a single 3.3V or 5V supply.

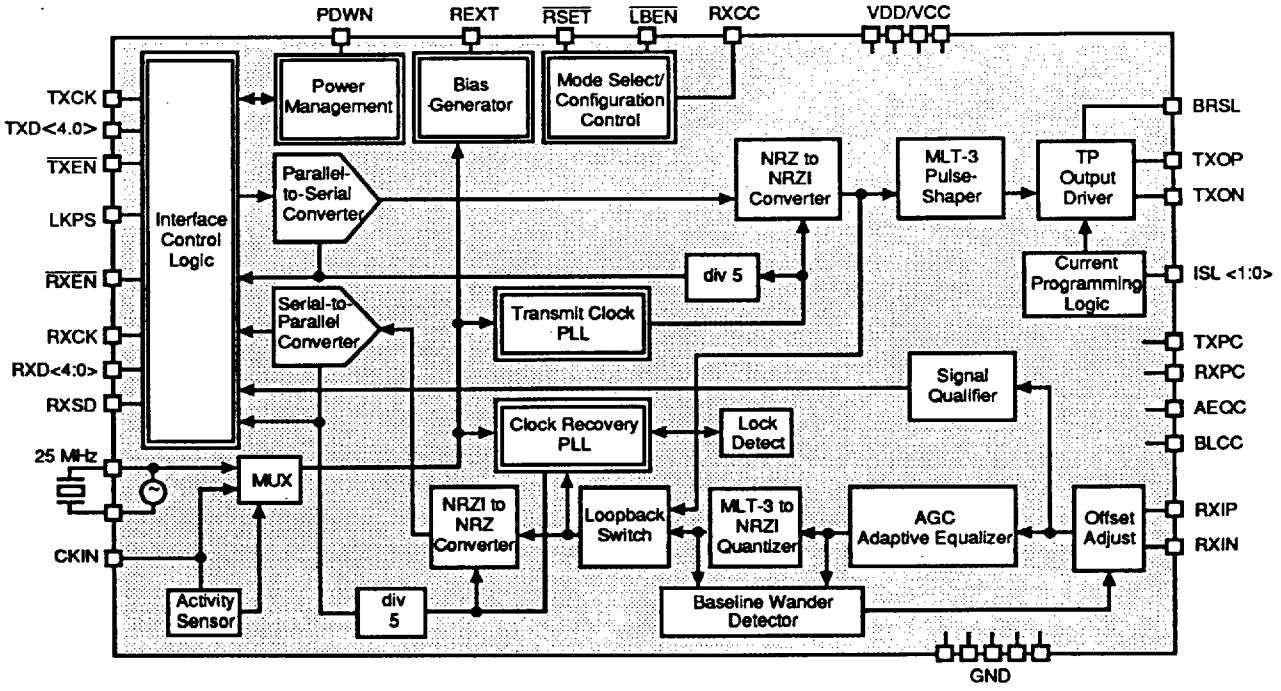
FEATURES

GENERAL

- **IEEE-802.3u compliant 100Base-TX TP-PMD transceiver for Cat 5 UTP cable**
- **Integrated transmit and clock-recovery PLLs**
- **Integrated power-on reset**
- **Supports full-duplex operation**
- **Internal loopback mode**
- **Chip power-down mode**
- **Automatic sensing of supply voltages**
- **Low power design with advanced power management**
- **Advanced BiCMOS technology in a 48-Lead TQFP package**

(continued)

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

GENERAL

Supply Voltage

The 78Q2121 can operate from a single 3.3V (± 0.3V) or 5V (± 5%) power supply. Detection of supply voltage is automatic. In the case when both 3.3V and 5V supplies are available, the 5V supply can be used to power the transmit line driver, with 3.3V supplying to the rest of the on-chip circuitry. This combination allows the use of a non center-tapped transmit transformer, thereby allowing line output drive current to be halved without sacrificing performance. This mode allows the most power efficient operation, and is selected when BRSL pin is tied high. Note that this feature is disabled when only 3.3V supply is used.

Clock Selection

The 78Q2121 will default to use the internal crystal oscillator upon power-on. If this is the desired mode of operation, the CKIN pin should be tied low. If the chip is required to use an external 25 MHz clock, connect the external clock to the CKIN pin. The chip will sense the activity on the CKIN pin, and will automatically configure itself to use the external clock instead. In this mode of operation, a crystal is not required. When no crystal is present, the XTLP and XTLN pins should be left unconnected.

Power Management

The 78Q2121 has two power saving modes:

- Chip Power-Down
- Receive Power Management

Chip power-down is activated by enabling the PWDN pin. When the chip is in power-down mode, all on-chip circuitry are shut off, and the device consumes minimum power. When power-down is deactivated, a reset pulse should be applied to restore the chip to its initial power-on state. Note that power-on-reset is activated only upon initial start-up, and is unaffected by chip power-down.

Receive power management is activated by asserting the RXCC pin. In this mode of operation, the clock recovery PLL, and other respective receive circuitry, will be powered down whenever no valid signal is present at all the receive line interface pins.

FEATURES (continued)

- 3.3V or 5V operation with optional dual-supply mode for minimum power consumption

SYM INTERFACE

- 5B NRZ symbol interface connects directly to controller chips with integrated 100Base-TX PCS functions
- Signal detect pin asserted as soon as recovered clock is locked onto receive data
- Receive data automatically blanked out when signal detect is inactive
- Receive clock configurable to be either active or inactive when signal detect is disasserted
- TTL compatible input
- Transmit and receive output pins can be tristated independently

CLOCK GENERATION/RECOVERY

- Generates 125 MHz transmit clock from either external 25 MHz clock source or internal crystal oscillator
- Automatic detection of external clock input
- Advanced lock detection circuit minimizes acquisition time and provides fast lock indication
- Receive clock automatically references to transmit clock when no receive signal is present

LINE DRIVER/RECEIVER

- Built-in transmit pulse-shaper, no external filter required
- Programmable output drive current
- Automatic receive gain and real-time adaptive equalization
- Adaptive baseline wander correction
- Built-in signal qualifier (detector) with 'smart' squelch feature
- Line input and/or output pin become high-Z when receive and/or transmit function is disabled respectively, allowing parallel connection of similar PMD devices

As soon as a valid signal is detected, all circuits will automatically be powered up to resume normal operation. Note that RXCK will be inactive when the clock recovery PLL is in power-down state.

Loopback Mode

Digital loopback mode can be enabled through the $\overline{\text{LBEN}}$ pin. This mode allows transmit NRZI bit stream to be looped back to the receive side prior to entering the pulse-shaper and line driver. The loopback data is subsequently re-timed by the clock recovery PLL and re-presented to the receive SYM interface. During loopback, the line transmit pins are tristated, and any data presented to the receive port is ignored.

SYM INTERFACE

The SYM interface is a 15-bit TTL compatible interface composed of two parts:

• Transmit:	transmit data	(TXD<4:0>)
	transmit clock	($\overline{\text{TXCK}}$)
	transmit enable	($\overline{\text{TXEN}}$)
• Receive:	receive data	(RXD<4:0>)
	receive clock	($\overline{\text{RXCK}}$)
	receive signal detect	($\overline{\text{RXSD}}$)
	receive enable	($\overline{\text{RXEN}}$)

Transmit

The 5-bit transmit data symbols are clocked in on every rising edge of TXCK. TXCK is a continuous 25 MHz clock referenced to either the internal crystal oscillator or the externally applied clock depending on the mode of operation. However, if the latter mode is used, absolute phase relation between TXCK and CKIN is not guaranteed.

The 5-bit data symbols are concatenated and presented to the analog transmitter as a 125 MHz bit stream, with TXD4 being the first bit to be transmitted, and TXD0 being the last. When $\overline{\text{TXEN}}$ is high, the transmit clock is disabled and TXCK pin becomes high impedence.

Receive

Data recovered from the line media is concatenated to groups of 5-bit symbols, with RXD4 being the first received bit, and RXD0 being the last. These symbols are clocked out to the PCS on the falling edge of the recovered 25 MHz clock (RXCK). RXCK can be pin configured to be either active or inactive when the signal detect pin (RXSD) is not asserted. If the former is selected, RXCK is continuously active. It is phase-locked to the receive data when RXSD is asserted, and is derived from the transmit clock when RXSD is disasserted. If the latter mode is selected, RXCK remains low whenever RXSD is not asserted.

RXSD is asserted as soon as the receive data is locked in and the recovered clock frequency is within 1% of the actual data-rate frequency. RXSD is disasserted when more than 150 consecutive bits of zeros are received. When RXSD is not asserted, all-zero data will appear on the RXD data bus. Note that data on the RXD bus is not aligned to symbol boundaries. When $\overline{\text{RXEN}}$ is high, all receive interface pins are tristated, allowing other chips to drive the MII/SYM signal lines.

TRANSMITTER

The transmit section of the chip contains all necessary circuitry to convert pre-scrambled, 5-bit NRZ symbol data from the PCS to an IEEE-802.3u compliant data-stream driving a pair of Cat-5 UTP cable.

The transmit section consist of three major blocks:
- Transmit PLL
- Pulse-Shaper
- Line Driver

Transmit PLL

The transmitter uses an on-chip low-jitter PLL synthesizer to generate the 125 MHz transmit clock. This PLL locks either to the local 25 MHz crystal oscillator, or the externally applied clock, depending on the mode of operation.

Pulse-Shaper

The pulse-shaper uses a sophisticated current modulation scheme to produce the desired output waveform. Controlled rise/fall time is achieved using accurately controlled C/I filter, and MLT-3 waveforms are generated through current modulation, allowing average drive current to be effectively halved compared to conventional approach.

FUNCTIONAL DESCRIPTION (continued)

Line Driver

The line driver is closely mingled with the pulse-shaper, combined to ensure the output waveform is sufficiently pulse-shaped to exceed FCC requirements. The 78Q2121 allows for programmable output drive current to compensate for insertion losses of various external magnetic modules. Output drive current can be set from 100% to 140% by pin selection through ISL<1:0> pins.

The line driver requires an external 1:1 isolation transformer to interface with the line media. For 3.3V operation, the transformer should be center-tapped to Vcc. In this mode, the transformer efficiency is 50%, and a nominal peak drive current of 40 mA is required. If a 5V supply is available to power the line driver (VPB pin), the advanced on-chip bridge driver can be activated to minimize power consumption.

In this mode, a non center-tapped transformer is used, and the required peak drive current is reduced to 20 mA. This power-saving mode is selected when BRSL pin is tied high. When $\overline{\text{TXEN}}$ is high, the line driver is disabled and the line transmit pins become high-impedence.

RECEIVER

The receive section contains three major blocks:

- Adaptive Equalizer/Baseline Wander Corrector
- Signal Qualifier
- Clock Recovery PLL

Adaptive Equalizer/Baseline Wander Corrector

On the receive side, a data signal from up to 100m of Cat-5 UTP cable enters the chip through a transformer. This signal goes through a combination of adaptive offset adjustment (baseline wander correction), automatic gain, and adaptive equalization. The effect of these circuits is to sense the amount of dispersion, distortion and attenuation caused by the cable and transformer, and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The equalized MLT-3 data signal is decoded and quantized through analog receivers. The recovered bit-stream is then presented the Clock Recovery PLL for clock acquisition.

Signal Qualifier

The integrated signal qualifier has separate squelched and unsquelched thresholds, and includes a built-in timer to ensure fast and accurate receive signal detection. Upon detection of two or more valid pulses on the line receive port, the pass indication, indicating the presence of valid receive signals, will be asserted. When pass is asserted, the signal detect threshold is lowered by about 60%, and all adaptive circuits are released from their quiescent operating conditions, allowing them to lock onto the incoming data. When no signal is presented for a period of about 1.2 µs, the pass indication will be disasserted, and the signal detect threshold will return to the squelched level. RXSD on the SYM interface is asserted if and only if pass is active and the recovered clock frequency is within 0.1% of the actual data-rate frequency.

Clock Recovery PLL

The 125 MHz receive clock is extracted using a low-jitter PLL. The AC coupled phase detector ensures that clock skew is minimized during periods when data transition density is low. When no receive signal is present, the PLL is directed to lock onto the transmit 125 MHz clock. When pass is asserted, the PLL will use the received NRZI signal as the clock reference. The recovered clock is used to re-time the data signal and, subsequently, converting the data to NRZ format.

BIASING

The 78Q2121 uses the reference clock to generate accurate bias voltages for setting the various precision circuitry on chip. This technique allows rise and fall times of transmit pulses to be controlled accurately, and also allows center frequencies of the two on-chip VCOs to be set precisely. All these are achieved without trimming or precision external components which are typical in other ICs requiring precision timing. The ability to set accurate center frequencies allow the use of narrow-band PLL circuits without the requirement of complex frequency discrimination circuits to aid clock acquisition. Only one external resistor is required for generating various precision bias currents for the bipolar circuits.

PIN DESCRIPTION

Note Abbreviations: S = Supply; IT = TTL Input; O4 = Output with I_{OL} = 4 mA @ Vcc = 3.3V or I_{OL} = 8 mA @ Vcc = 5.0V; A = Analog; IA = Analog Input; OA = Analog Output

NAME	TYPE	DESCRIPTION
VPA	S	Analog Supply
VNA	S	Analog Ground
VPB	S	Transmit Analog Supply
VNB	S	Transmit Analog Ground
VPC	S	CMOS Logic Supply
VNC	S	CMOS Logic Ground
VPD	S	Digital I/O Supply
VND	S	Digital I/O Ground
VNS	S	Substrate Ground
TXCK	O4	Transmit Clock
TXD[4:0]	IT	Transmit Data
$\overline{\text{TXEN}}$	IT	Transmit Enable
RXCK	O4	Receive Clock
RXD[4:0]	O4	Receive Data
RXSD	O4	Receive Signal Detection
$\overline{\text{RXEN}}$	IT	Receive Enable
LKPS	O4	Lock/Pass Indication
TXOP	OA	Transmit UTP Output +
TXON	OA	Transmit UTP Output -
RXIP	IA	Receive UTP Input +
RXIN	IA	Receive UTP Input -
CKIN	IT	External 25 MHz Clock
XTLP	A	25 MHz Crystal Pin +
XTLN	A	25 MHz Crystal Pin -
REXT	A	Bias Current Reference Resistor Pin
$\overline{\text{RSET}}$	IT	Chip Reset
$\overline{\text{LBEN}}$	IT	Loopback Enable
TSA0	IT	Test pin used by factory, leave open
TSA1	IT	Test pin used by factory, leave open
TSA2	IT	Test pin used by factory, leave open

PIN DESCRIPTION (continued)

Note Abbreviations: S = Supply; IT = TTL Input; O4 = Output with I_{OL} = 4 mA @ Vcc = 3.3V or I_{OL} = 8 mA @ Vcc = 5.0V; A = Analog; IA = Analog Input; OA = Analog Output

NAME	TYPE	DESCRIPTION
PDWN	IT	Chip Power-Down
ISL[1:0]	IT	Transmit Line Drive Current Selection
BRSL	IT	Bridge Driver Selection
RXCC	IT	Receive Power Management Enable
AEQC	A	Adaptive Equalizer Filter Voltage
BLCC	A	Baseline Corrector Filter Voltage
TXPC	A	Transmit PLL Filter Voltage
RXPC	A	Clock Recovery PLL Filter Voltage

CONFIGURATION CONTROL

The following section assumes the following:

Pin connection: H = Vcc; L = Gnd; Power Supply: 3.3V => 3.3 ± 0.3V; 5V => 5V ± 5%

SUPPLY VOLTAGE SELECTION

VNA = VNB = VNC = VND = VNS = Gnd

a) 5V only: VPA = VPB = VPC = VPD = 5V

b) 3.3V only: VPA = VPB = VPC = VPD = 3.3V

c) Dual Voltage mode: VPA = VPC = VPD = 3.3V; VPB = 5V

RECEIVE POWER MANAGEMENT MODE SELECTION

RXCC = H: Receive Power Management active (LKPS = pass)

= L: Receive Power Management inactive (LKPS = lock)

NOTE: pass = Signal Qualifier pass indication; lock = Clock Recovery PLL lock indication

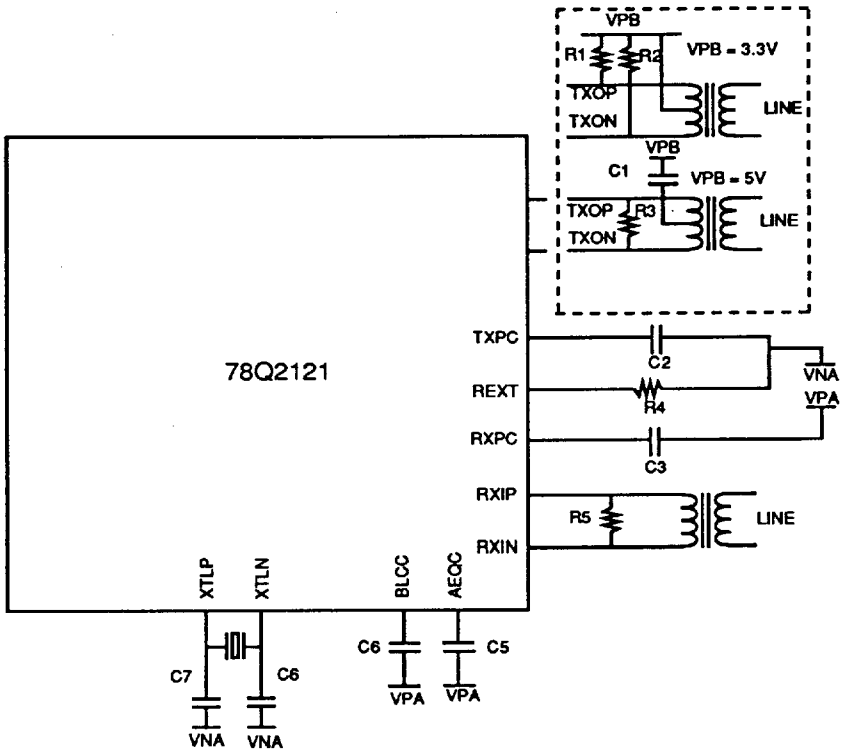
TRANSMIT LINE DRIVE CURRENT SELECTION

Select drive current based on insertion loss specification on line transformer.

ISL<1:0>	DRIVE CURRENT	INSERTION LOSS
00	100%	0.0 - 0.5 dB
01	110%	0.5 - 1.3 dB
10	120%	1.3 - 2.0 dB
11	140%	2.5 - 3.4 dB

EXTERNAL COMPONENTS

The chip requires a few external passive components to function properly. These components, with their recommended values, are shown below:



NAME	FUNCTION	VALUE	TOLERANCE	NOTE
R1	Back termination	50Ω	5%	For BRSL = L only
R2	Back termination	50Ω	5%	For BRSL = L only
R3	Back termination	100Ω	5%	For BRSL = H only
R4	Current setting	9.8 kΩ	1%	
R5	Line termination	100Ω	5%	
C1	Common-mode suppression	0.1 µF	20%	optional
C2	Transmit PLL filter	25 pF	20%	optional
C3	Receive PLL filter	25 pF	20%	optional
C4	Adaptive equalizer filter	10 pF	20%	optional
C5	Baseline corrector filter	5 pF	20%	optional
C6,C7	Crystal load capacitors	20 pF	10%	

EXTERNAL COMPONENTS (continued)

ISOLATION TRANSFORMERS

Two simple 1:1 isolation transformers are all that is required at the line interface, but transformers with integrated common-mode choke are recommended for exceeding FCC requirements. The line transformers should have the following characteristics:

NAME	VALUE	CONDITION
Turns Ratio	1 CT : 1 CT ± 5%	
Open-Circuit Inductance	350 µH (min)	@ 10 mV, 10 kHz
Leakage Inductance	0.40 µH (max)	@ 1 MHz (min)
Inter-Winding Capacitance	12 pF (max)	
DC Resistance	0.9Ω (max)	
Insertion Loss	1.1 dB (typ)	0 - 100 MHz
HIPOT	1500 Vrms	

NOTE: For the line transmit transformer, insertion loss up to 3.4 dB can be tolerated due to the programmability of the output drive current.

For the line receive transformer, OCL can be as low as 100 µH since the baseline wander correction circuit will be able to track the transformer droop.

REFERENCE CRYSTAL

If internal crystal oscillator is to be used, a crystal with the following characteristics should be chosen:

NAME	VALUE	UNITS
Frequency	25.00000	MHz
Load Capacitance	15	pF
Frequency Tolerance	±20	PPM
Aging	±2	PPM/yr
Temperature Stability (0 - 70°C)	±5	PPM
Oscillation Mode	Fundamental	
Parameters at 25°C ± 2°C; Drive Level = 0.5 mW		
Shunt Capacitance (max)	8	pF
Motional Capacitance (min)	10	*f*F
Series Resistance (max)	25	Ω
Spurious Response (max)	> 5 dB below main within 500 kHz	

ELECTRICAL SPECIFICATIONS

Operating Temperature Range: 0 - 70°C

DC ELECTRICAL CHARACTERISTICS

The following ratings assumes the nominal ISL setting of <00>

CHARACTERISTICS		CONDITION	MIN	NOM	MAX	UNIT
Supply Voltage	V_{CC}	V_{CC} = 3.3V V_{CC} = 5.0V	3.0 4.75		3.6 5.25	V V
TTL Input Voltage Low	V_{IL}	V_{CC} = 5.0V			0.8	V
TTL Input Voltage High	V_{IH}	V_{CC} = 5.0V	2.0			V
TTL Output Voltage High	V_{OH}	I_{OH} = 4.0 mA, Vcc = 3.0V	2.4			V
TTL Output Voltage Low	V_{OL}	I_{OL} = 4.0 mA, Vcc = 3.0V			0.4	V
Power-Down current	I_{PDN}				500	µA
Core Supply Current	I_{DDC}			35	50	mA
Line Driver Supply Current (average)	I_{DDB}	BRSL = L BRSL = H		20 10	25 12	mA mA
Total Supply Current (average)	$I_{DDT(AV)}$	BRSL = L BRSL = H		55 45		mA mA

ANALOG ELECTRICAL CHARACTERISTICS

The following electrical specifications assume proper termination of input and output ports and nominal connection to transmit and receive isolation transformers.

Unless otherwise stated, ISL setting is assumed to be <00> {default}.

TRANSMITTER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PLL Locking Time			3		µs
Output Jitter (Vp-p)				1.4	ns
Duty Cycle Distortion (Vp-p)				0.5	ns
UTP Pulse Rise/Fall Time			4		ns
UTP Rise/Fall Time Imbalance			±0.5		ns
Differential Output Signal (0-pk)	R_{load} = 50 Ω	950		1050	mV
Signal Amplitude Symmetry			± 2		%
Signal Amplitude Overshoot			3		%
Peak Output Drive Current	BRSL = L BRSL = H	38 19		42 21	mA mA
Peak Output Current Range	Nominal	100		140	%

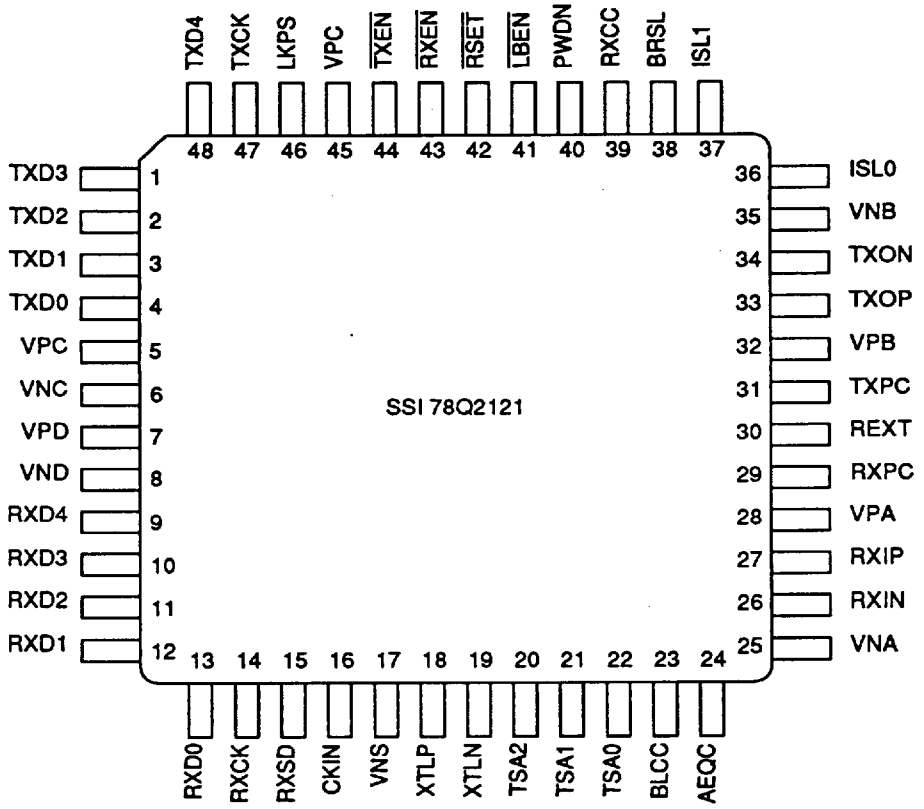
ELECTRICAL SPECIFICATIONS (continued)

RECEIVER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PLL Locking Time			2		µs
Jitter Tolerance			4.0		ns
Bit Error Ratio			10^{-10}		
Input Amplitude Range (0-pk)				1.2	V
Baseline Wander Tracking		-75		+75	%
Input Bias Level		Vcc - 0.5		Vcc	V
Input Squelched Threshold (Vp-p)		600	800	1000	mV
Input Unsquelched Threshold (Vp-p)		200	300	400	mV
Signal Detect Assertion Time				200	µs
Signal Detect De-assertion Time				1.4	µs

PACKAGE PIN DESIGNATIONS

(Top View)



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78Q2121 48-lead TQFP	78Q2121-CGT	78Q2121-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914