

4 M-BIT DYNAMIC RAM 1 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μ PD424400-L is a 1 048 576 words by 4 bits dynamic CMOS RAM. The fast page mode capability realize high speed access and low power consumption.

These are packed in 26-pin plastic TSOP(II), 26-pin plastic SOJ and 20-pin plastic ZIP.

Features

- 1 048 576 words by 4 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- Fast access and cycle time

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μ PD424400-60L	660 mW	1.1 mW (CMOS level input)	60 ns	120 ns	40 ns
μ PD424400-70L	550 mW		70 ns	140 ns	45 ns
μ PD424400-80L	495 mW		80 ns	160 ns	50 ns
μ PD424400-10L	440 mW		100 ns	190 ns	60 ns

- 1 024 refresh cycles/128 ms
- CAS before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- Multiplexed address inputs Row address : A0 to A9, Column address : A0 to A9

The information in this document is subject to change without notice.

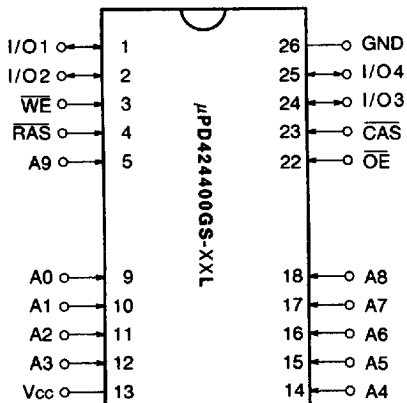
Ordering Information

Part number	Access time (MAX.)	Package	Quality grade
μPD424400GS-60L	60 ns	26-pin Plastic TSOP(II) (300 mil)	Standard
μPD424400GS-70L	70 ns		
μPD424400GS-80L	80 ns		
μPD424400GS-10L	100 ns		
μPD424400LA-60L	60 ns	26-pin Plastic SOJ (300 mil)	
μPD424400LA-70L	70 ns		
μPD424400LA-80L	80 ns		
μPD424400LA-10L	100 ns		
μPD424400V-60L	60 ns	20-pin Plastic ZIP (400 mil)	
μPD424400V-70L	70 ns		
μPD424400V-80L	80 ns		
μPD424400V-10L	100 ns		

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

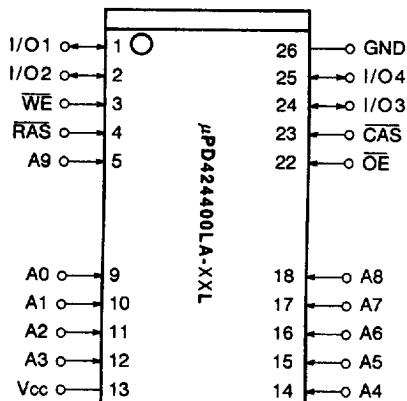
Pin Configurations (Marking Side)

26-pin Plastic TSOP(II) (300 mil)

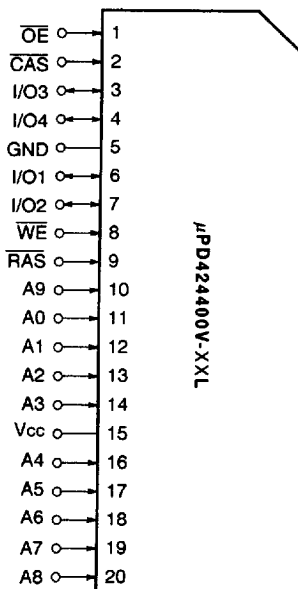


A0 to A9 : Address Inputs
 I/O1 to I/O4 : Data Inputs/Outputs
 $\overline{\text{RAS}}$: Row Address Strobe
 $\overline{\text{CAS}}$: Column Address Strobe
 $\overline{\text{WE}}$: Write Enable
 $\overline{\text{OE}}$: Output Enable
 Vcc : Power Supply
 GND : Ground

26-pin Plastic SOJ (300 mil)

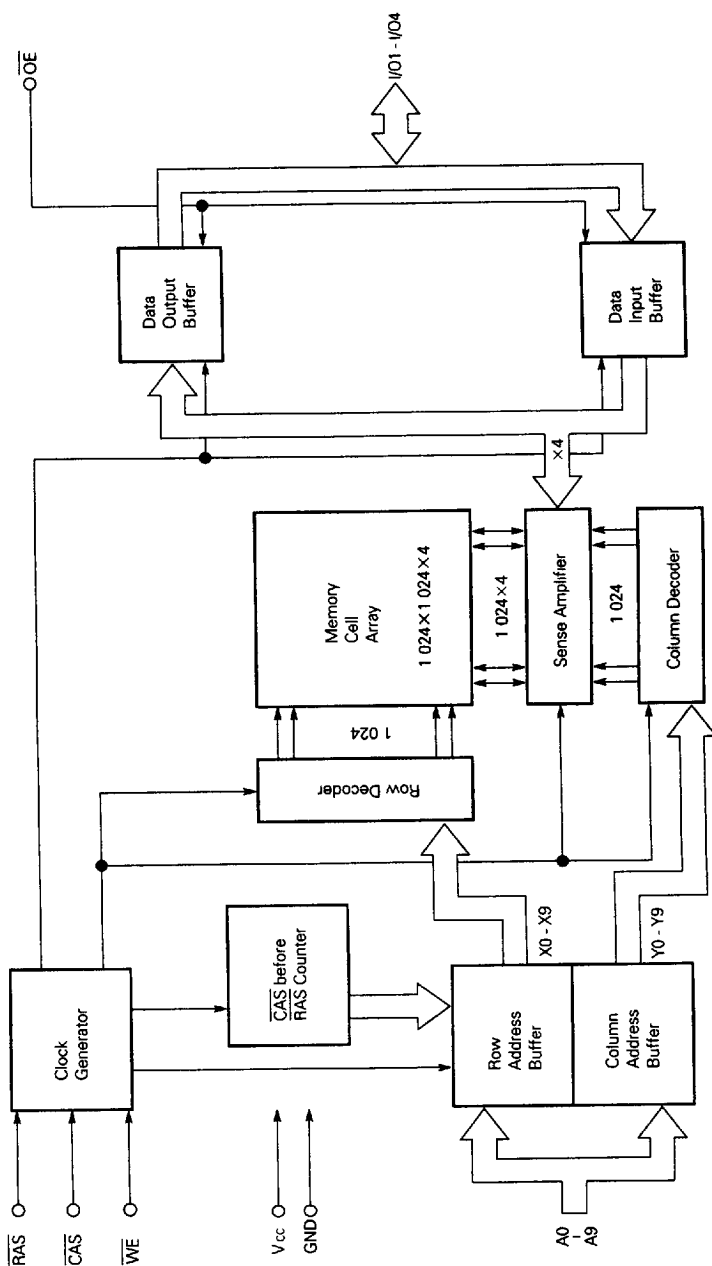


20-pin Plastic ZIP (400 mil)



- A0 to A9 : Address Inputs
 I/O1 to I/O4 : Data Inputs/Outputs
 RAS : Row Address Strobe
 CAS : Column Address Strobe
 WE : Write Enable
 OE : Output Enable
 Vcc : Power Supply
 GND : Ground

Block Diagram



Input/Output Pin Functions

The μPD424400-L has input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A9 and input/output pins I/O1 to I/O4.

Pin Name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address input)		Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (tASR, tASC) and hold time (tRAH, tCAH) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input/ Output	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data input/output)		4-bit data bus. I/O1 to I/O4 are used to input/output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	$^{\circ}\text{C}$

Capacitance ($T_a = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

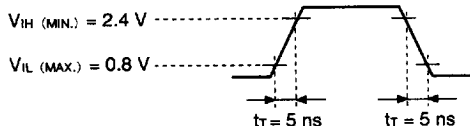
Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current	I _{CC1}	RAS, CAS Cycling t _{RC} = t _{RC} (MIN.) I _O = 0 mA	t _{RAC} = 60 ns		120	mA	1, 2, 3
			t _{RAC} = 70 ns		100		
			t _{RAC} = 80 ns		90		
			t _{RAC} = 100 ns		80		
Standby current	I _{CC2}	RAS, CAS ≥ V _{IH} (MIN.), I _O = 0 mA			2	mA	
		RAS, CAS ≥ V _{CC} - 0.2 V, I _O = 0 mA			0.2		
RAS only refresh current	I _{CC3}	RAS Cycling, CAS ≥ V _{IH} (MIN.) t _{RC} = t _{RC} (MIN.), I _O = 0 mA	t _{RAC} = 60 ns		120	mA	1,2,3,4
			t _{RAC} = 70 ns		100		
			t _{RAC} = 80 ns		90		
			t _{RAC} = 100 ns		80		
Operating current (Fast page mode)	I _{CC4}	RAS ≤ V _{IL} (MAX.), CAS Cycling t _{PC} = t _{PC} (MIN.), I _O = 0 mA	t _{RAC} = 60 ns		90	mA	1, 2, 5
			t _{RAC} = 70 ns		80		
			t _{RAC} = 80 ns		70		
			t _{RAC} = 100 ns		60		
CAS before RAS refresh current	I _{CC5}	RAS Cycling t _{RC} = t _{RC} (MIN.) I _O = 0 mA	t _{RAC} = 60 ns		120	mA	1, 2
			t _{RAC} = 70 ns		100		
			t _{RAC} = 80 ns		90		
			t _{RAC} = 100 ns		80		
CAS before RAS long refresh current (1 024 Cycles / 128 ms)	I _{CC6}	CAS before RAS refresh : 1 024 Cycles / 128 ms RAS, CAS : V _{CC} -0.2 V ≤ V _{IH} ≤ V _{IH} (MAX.) 0 V ≤ V _{IL} ≤ 0.2 V Standby : RAS, CAS ≥ V _{CC} -0.2 V Address : V _{IH} or V _{IL} WE, OE : V _{IH} I _O = 0 mA	t _{RAS} ≤ 200 ns		300	μA	1, 2
			t _{RAS} ≤ 1 μs		500		
Input leakage current	I _{I(L)}	V _I = 0 to 5.5 V All other pins not under test = 0 V	-10		+10	μA	
Output leakage current	I _{O(L)}	V _O = 0 to 5.5 V Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage	V _{OH}	I _O = -5.0 mA	2.4			V	
Low level output voltage	V _{OL}	I _O = +4.2 mA			0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during RAS ≤ V_{IL}(MAX.) and CAS ≥ V_{IH}(MIN.).
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

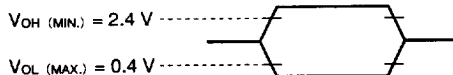
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		$t_{RAC} = 100 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{RC}	120	-	140	-	160	-	190	-	ns	
RAS Precharge Time	t_{RP}	50	-	60	-	70	-	80	-	ns	
CAS Precharge Time	t_{CPN}	10	-	10	-	10	-	10	-	ns	
RAS Pulse Width	t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
CAS Pulse Width	t_{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
RAS Hold Time	t_{RSH}	20	-	20	-	20	-	25	-	ns	
CAS Hold Time	t_{CSH}	60	-	70	-	80	-	100	-	ns	
RAS to CAS Delay Time	t_{RCD}	20	40	20	50	25	60	25	75	ns	1
RAS to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	1
CAS to RAS Precharge Time	t_{CRP}	10	-	10	-	10	-	10	-	ns	2
Row Address Setup Time	t_{ASR}	0	-	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	10	-	10	-	12	-	12	-	ns	
Column Address Setup Time	t_{ASC}	0	-	0	-	0	-	0	-	ns	
Column Address Hold Time	t_{CAH}	15	-	15	-	15	-	20	-	ns	
OE Lead Time Referenced to RAS	t_{OES}	0	-	0	-	0	-	0	-	ns	
CAS to Data Setup Time	t_{CLZ}	0	-	0	-	0	-	0	-	ns	
OE to Data Setup Time	t_{OLZ}	0	-	0	-	0	-	0	-	ns	
OE to Data Delay Time	t_{OED}	15	-	15	-	20	-	25	-	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh Time	t_{REF}	-	128	-	128	-	128	-	128	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{RAC} (MAX.)$	$t_{RAC} (MAX.)$
$t_{RAD} > t_{RAD} (MAX.)$ and $t_{RCD} \leq t_{RCD} (MAX.)$	$t_{AA} (MAX.)$	$t_{RAD} + t_{AA} (MAX.)$
$t_{RCD} > t_{RCD} (MAX.)$	$t_{CAC} (MAX.)$	$t_{RCD} + t_{CAC} (MAX.)$

$t_{RAD} (MAX.)$ and $t_{RCD} (MAX.)$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD} (MAX.)$ and $t_{RCD} \geq t_{RCD} (MAX.)$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycle.

Read Cycle

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		$t_{RAC} = 80 \text{ ns}$		$t_{RAC} = 100 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	-	60	-	70	-	80	-	100	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	-	15	-	20	-	20	-	25	ns	1
Access Time from Column Address	t_{AA}	-	30	-	35	-	40	-	50	ns	1
Access Time from $\overline{OE}$	t_{DEA}	-	20	-	20	-	20	-	25	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	-	35	-	40	-	50	-	ns	
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	-	10	-	10	-	10	-	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	-	0	-	0	-	0	-	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	3
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	0	25	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time(t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

- Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
- $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi - Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		tRAC = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Hold Time Referenced to CAS	twCH	15	–	15	–	15	–	20	–	ns	1
WE Pulse Width	tWP	15	–	15	–	15	–	20	–	ns	1
WE Lead Time Referenced to RAS	trWL	20	–	20	–	20	–	25	–	ns	
WE Lead Time Referenced to CAS	tcWL	15	–	15	–	15	–	20	–	ns	
WE Setup Time	twCS	0	–	0	–	0	–	0	–	ns	2
OE Hold Time	toEH	0	–	0	–	0	–	0	–	ns	
Data-in Setup Time	tDS	0	–	0	–	0	–	0	–	ns	3
Data-in Hold Time	tDH	15	–	15	–	15	–	20	–	ns	3

- Notes**
1. twP(MIN.) is applied for late write cycles or read modify write cycles. In early write cycles, twCH(MIN.) should be met.
 2. If twCS ≥ twCS(MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle.
 3. tDS(MIN.) and tDH(MIN.) are referenced to the CAS falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the WE falling edge.

Read Modify Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		tRAC = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trWC	165	–	185	–	210	–	250	–	ns	
RAS to WE Delay Time	trWD	80	–	90	–	105	–	130	–	ns	1
CAS to WE Delay Time	tcWD	40	–	40	–	45	–	55	–	ns	1
Column Address to WE Delay Time	tAWD	50	–	55	–	65	–	80	–	ns	1

- Notes**
1. If twCS ≥ twCS(MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If trWD ≥ trWD(MIN.), tcWD ≥ tcWD(MIN.), tAWD ≥ tAWD(MIN.), and tcPWD ≥ tcPWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

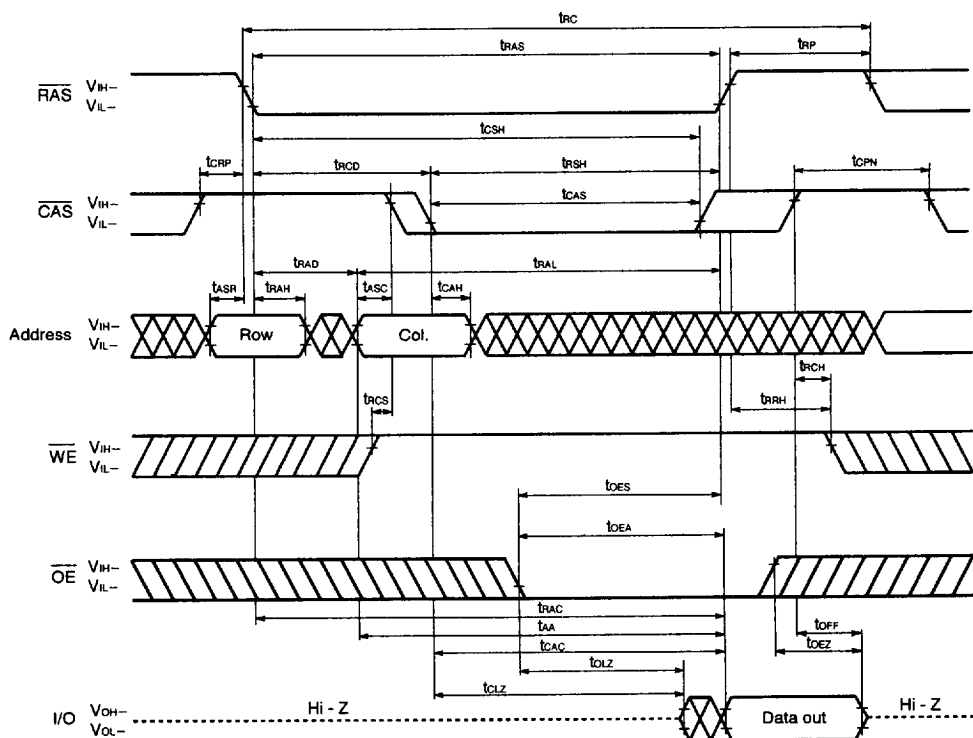
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	60	—	ns	
Access Time from CAS Precharge	t _{ACP}	—	35	—	40	—	45	—	55	ns	
RAS Pulse Width	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
CAS Precharge Time	t _{CP}	10	—	10	—	10	—	10	—	ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	35	—	40	—	45	—	55	—	ns	
Read Modify Write Cycle Time	t _{PRWC}	85	—	90	—	100	—	120	—	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	55	—	60	—	70	—	85	—	ns	1

Notes 1. If $t_{WCS} \geq t_{WCS(MIN)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{AWD} \geq t_{AWD(MIN)}$, $t_{CWD} \geq t_{CWD(MIN)}$, $t_{AWD} \geq t_{AWD(MIN)}$, and $t_{CPWD} \geq t_{CPWD(MIN)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

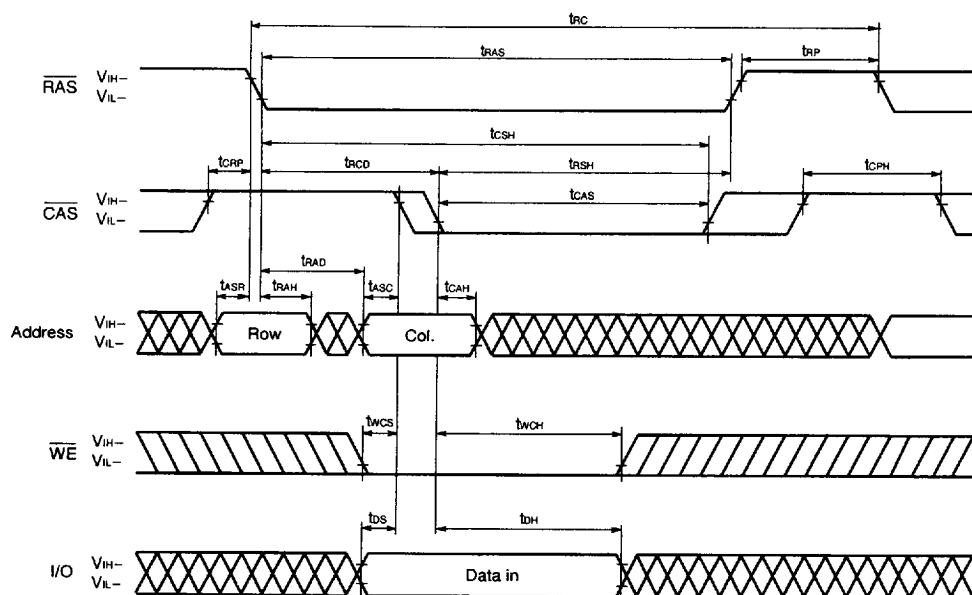
Refresh Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	15	—	15	—	15	—	20	—	ns	
RAS Precharge CAS Hold Time	t _{RPC}	10	—	10	—	10	—	10	—	ns	
WE Setup Time	t _{WSR}	10	—	10	—	10	—	10	—	ns	
WE Hold Time	t _{WHR}	15	—	15	—	15	—	20	—	ns	

Read Cycle

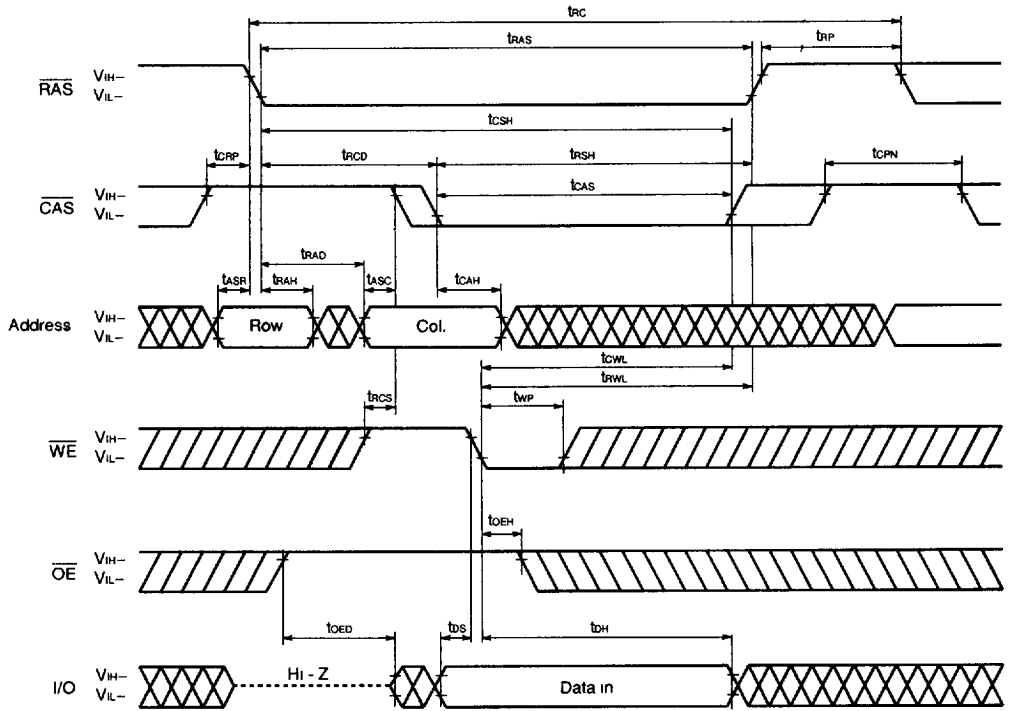


Early Write Cycle

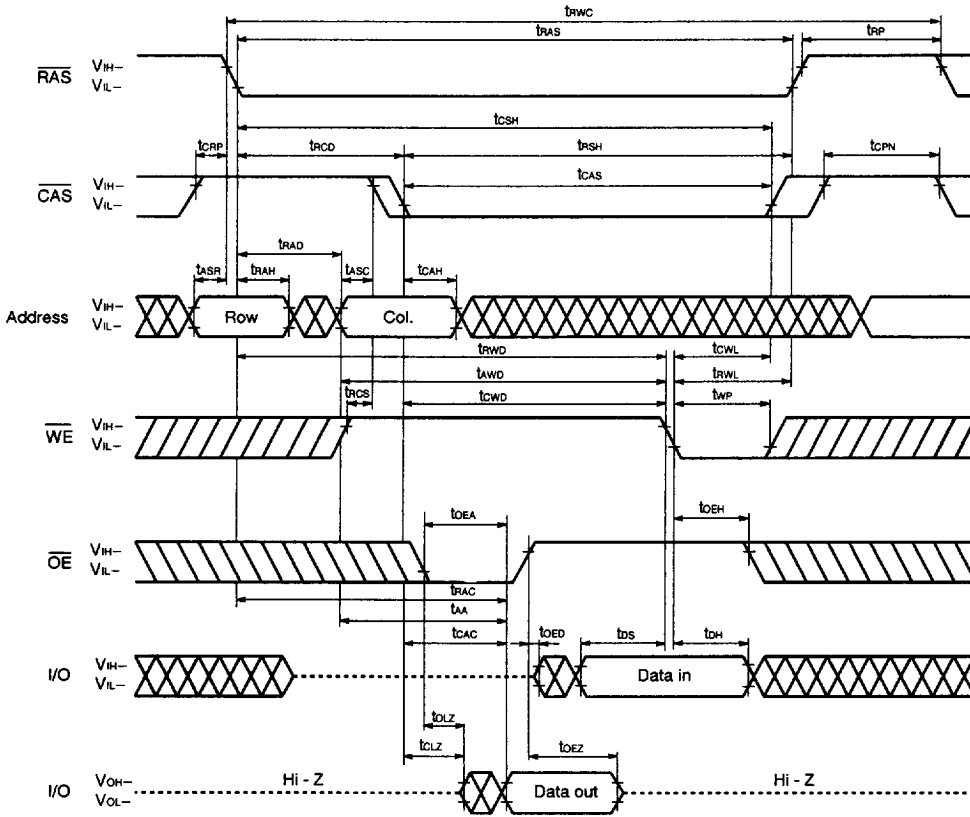


Remark $\overline{\text{OE}}$: Don't care

Late Write Cycle



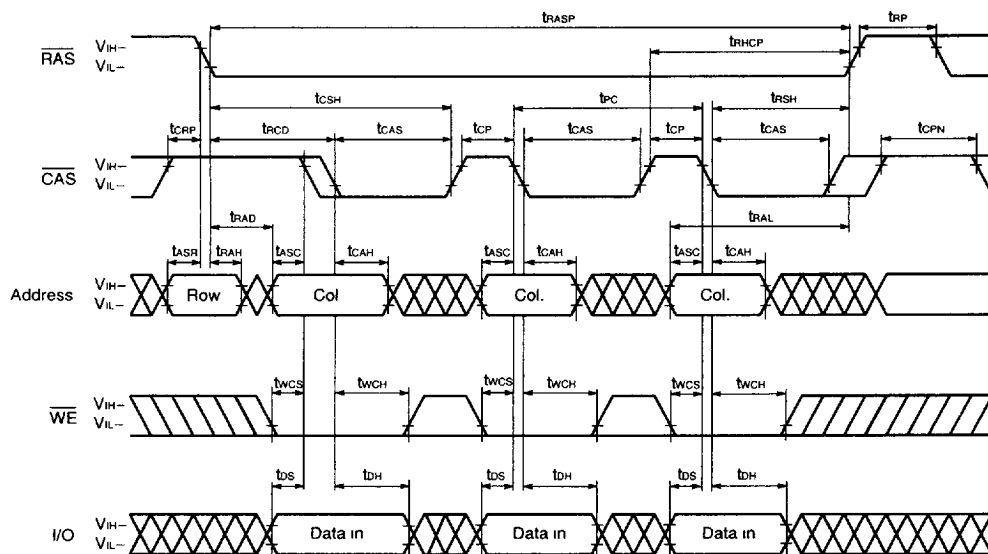
Read Modify Write Cycle



[illegible]

6427525 0055285 TT1

Fast Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

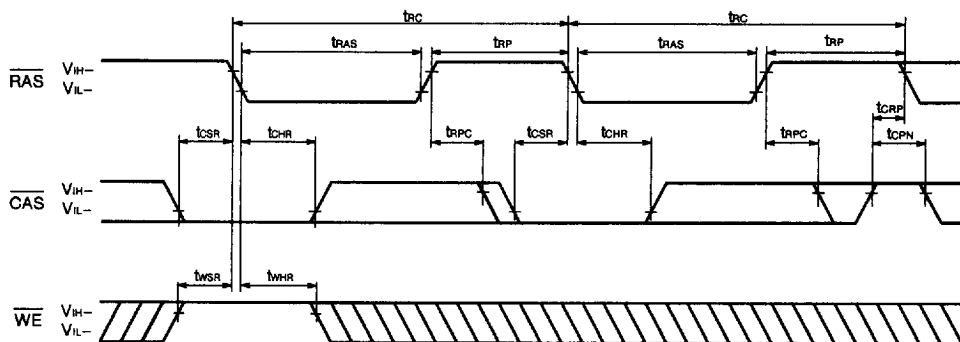
[illegible]

Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

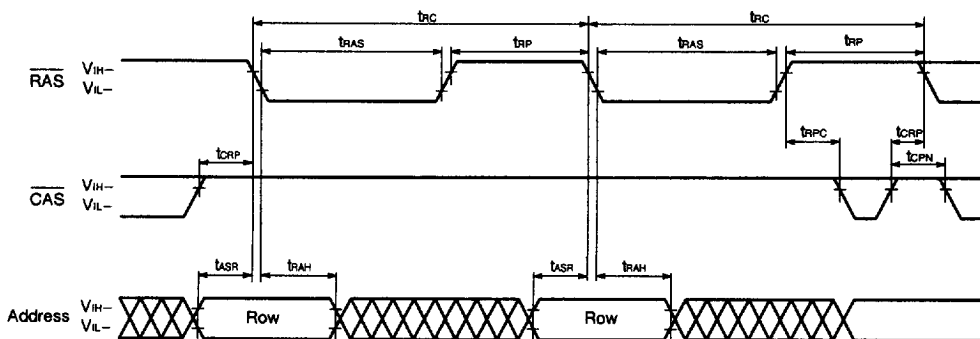
464 [REDACTED] 6427525 0055288 700 [REDACTED]

CAS Before RAS Refresh Cycle



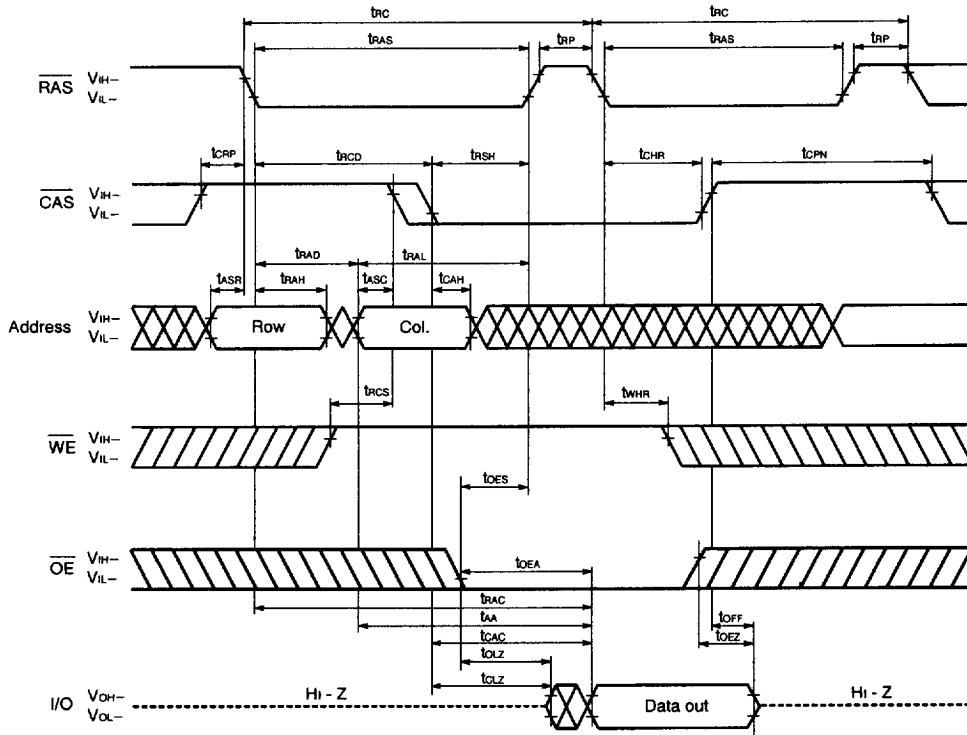
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

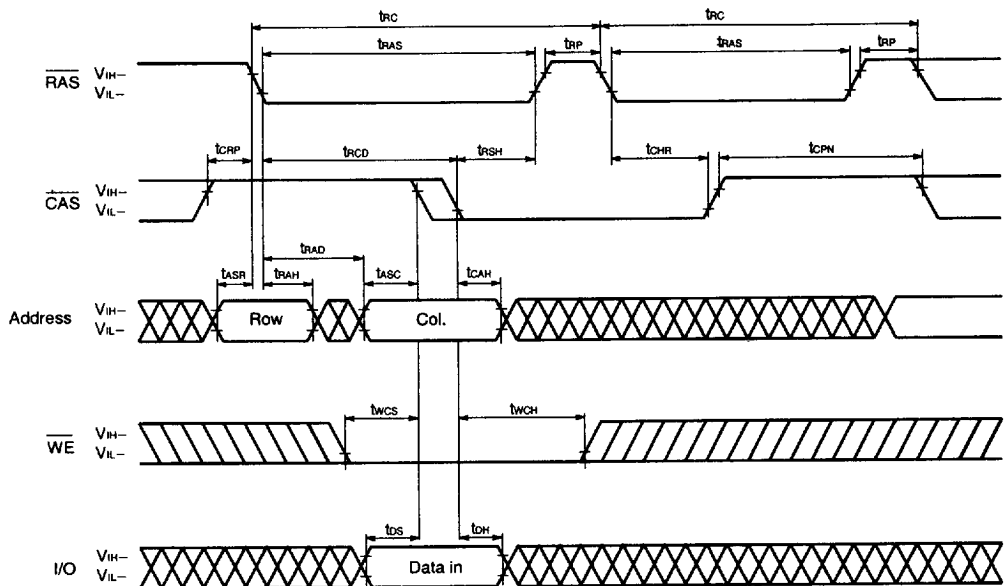


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

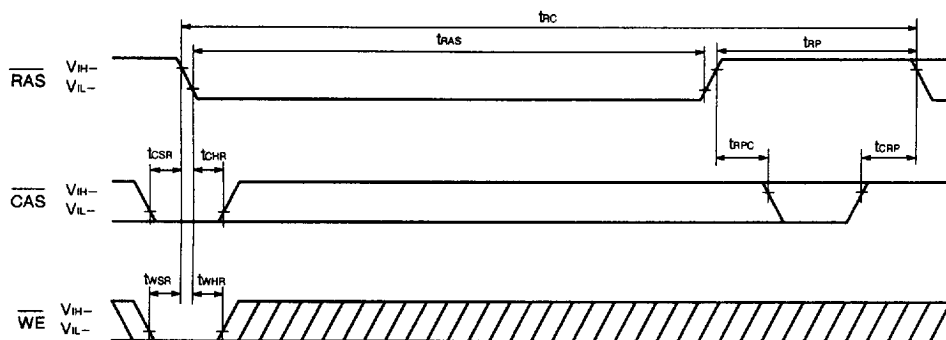


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)



Remark Address, $\overline{\text{OE}}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the X8-bit structure during test mode.

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 8 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output="1": Normal write (all memory cells)

Output="0": Abnormal write

(3) Refresh

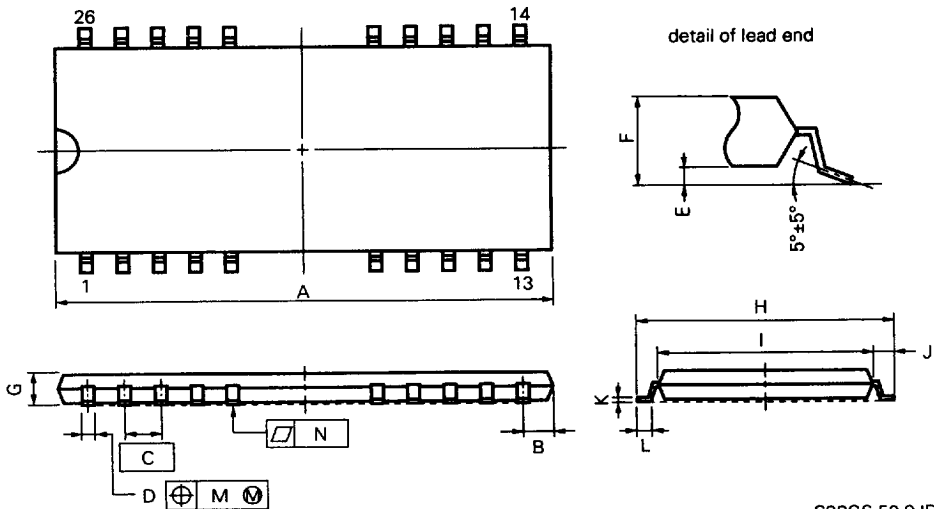
Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

Package Drawings

26 PIN PLASTIC TSOP(III) (300 mil)



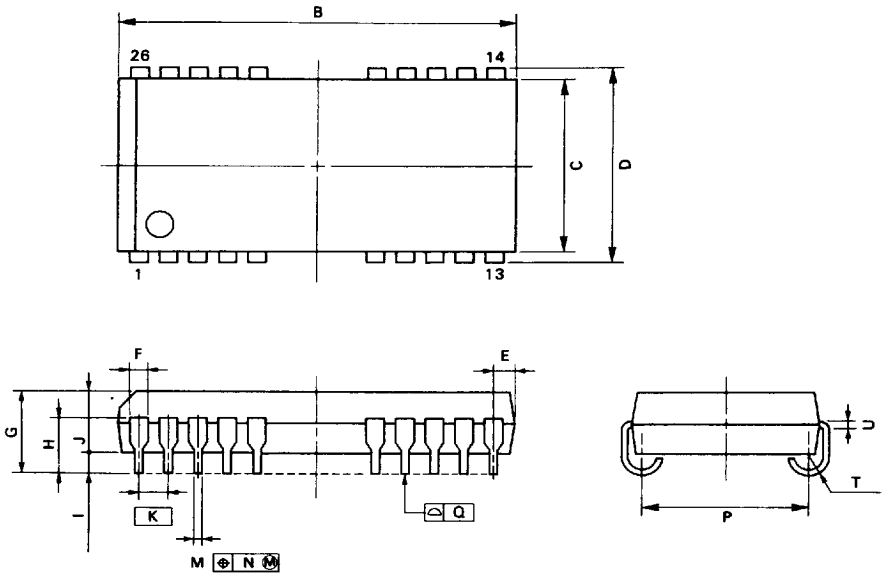
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S26GS-50-9JD-2

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.13 MAX.	0.045 MAX.
G	1.0	0.039
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

26PIN PLASTIC SOJ (300 mil)

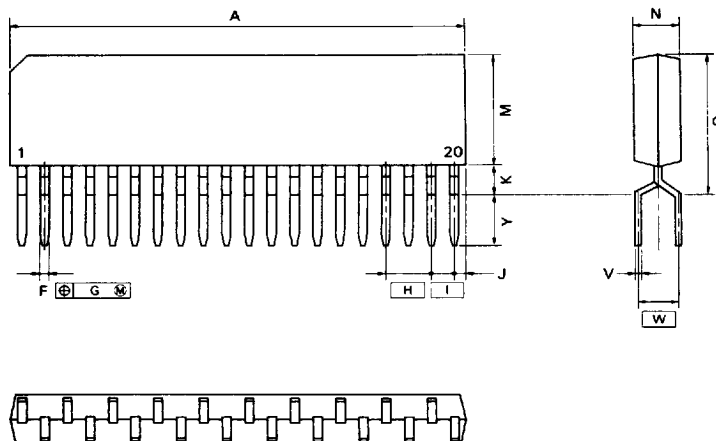


P26LA-50A-1

NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition

ITEM	MILLIMETERS	INCHES
B	17.4 ^{+0.2} _{-0.35}	0.685 ^{+0.008} _{-0.013}
C	7.57	0.298
D	8.47 ^{+0.2}	0.333 ^{+0.008} _{-0.008}
E	1.08 ^{+0.15}	0.043 ^{+0.008} _{-0.007}
F	0.6	0.024
G	3.5 ^{+0.2}	0.138 ^{+0.008}
H	2.4 ^{+0.2}	0.094 ^{+0.008} _{-0.008}
I	0.8 MIN	0.031 MIN
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 ^{+0.10}	0.016 ^{+0.004} _{-0.008}
N	0.12	0.005
P	6.73 ^{+0.20}	0.265 ^{+0.008}
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.06}	0.008 ^{+0.004} _{-0.002}

20PIN PLASTIC ZIP (400 mil)



NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T P) at maximum material condition

P20V-254-400A 1

ITEM	MILLIMETERS	INCHES
A	26.67 MAX	1.050 MAX.
F	$0.5^{+0.1}$	$0.020^{+0.004}$
G	φ0.25	φ0.010
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX	0.050 MAX
K	1.0 MIN	0.039 MIN
M	8.9 MAX	0.350 MAX
N	$2.8^{+0.2}$	$0.110^{+0.008}$
Q	10.16 MAX	0.400 MAX
V	$0.25^{+0.08}$	$0.010^{+0.003}$
W	2.54	0.100
Y	$3.3^{+0.5}$	$0.130^{+0.02}$

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD424400-L.
For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD424400GS : 28-pin plastic TSOP(II) (300 mll)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note}: 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit^{Note}: 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
 Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD424400LA : 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
 Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

Type of Through Hole Mount Device

μPD424400V : 20-pin plastic ZIP (400 mil)

Soldering process	Soldering conditions
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below
Partial heating method	Terminal temperature : 260 °C or below, Time : 10 seconds or below

Caution Do not jet molten solder on the surface of package.