INTRODUCTION

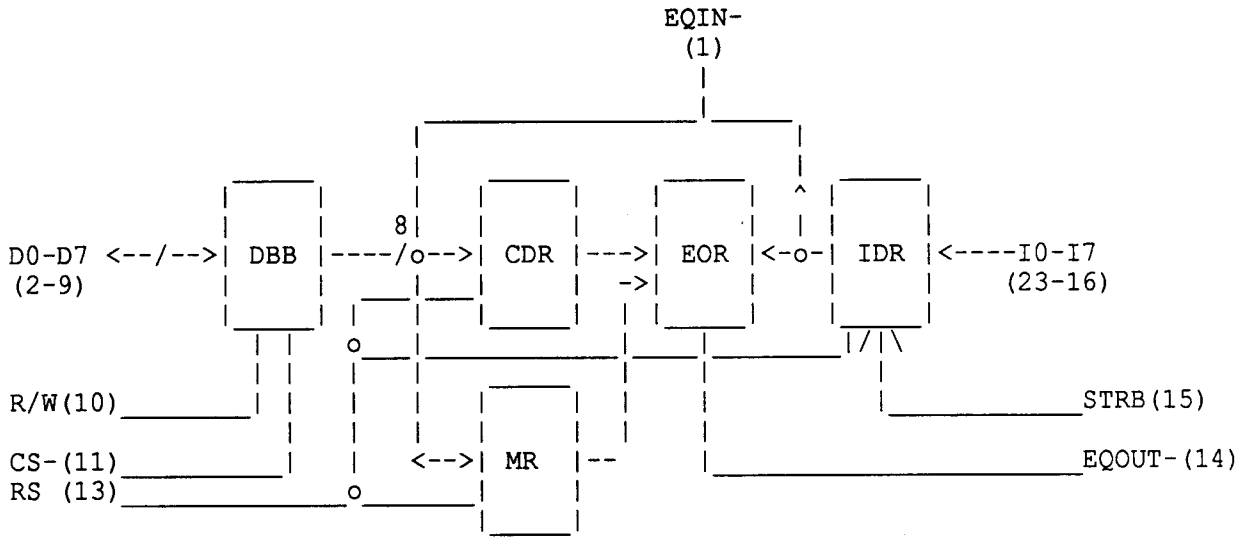
The W65C90 is a CMOS Eight-Bit-Comparator (EBC). The comparator consists of a Compare Data Register which contains the value to be compared to the input, and a Mask Register which allows individual bits to be masked out of the compare function. An Equal Output Bar pin indicates when there is a match and an Equal Input Bar pin allows the cascading of multiple devices.

KEY FEATURES OF THE W65C90

* CMOS 8-bit cascadable comparator
* W65Cxyz microprocessor bus compatible - 4, 6, and 8 MHz
* 24 pin package standard DIP in a width of 600 mils or skinny DIP in a width of 300 mils
* Each bit may be individually programmed for compare or "don't care"
* Wide operating supply range 1.8V-5.5V
* Fully static for Hi-Rel applications

SECTION 1

PIN FUNCTION DESCRIPTION



Note: Device pin numbers shown in parentheses.

Figure 1-1 W65C90 Internal Architecture Simplified Block Diagram

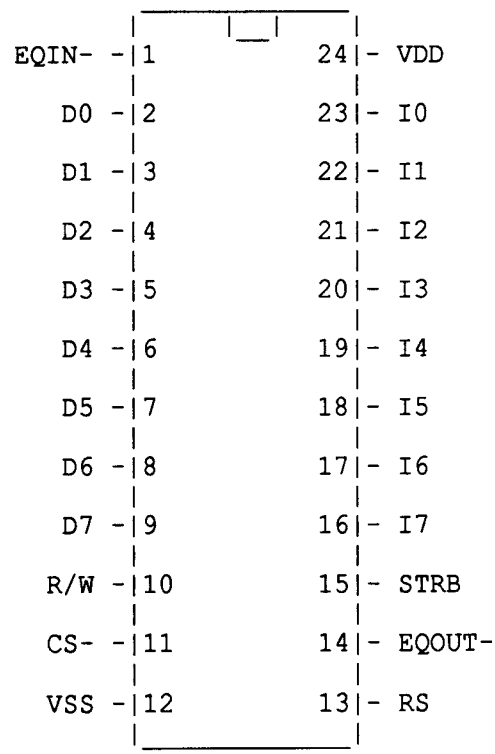


Figure 1-2 W65C90 24 Pin PDIP Pinout

Table 1-1 Pin Function Table

Pin	Description
CS-	Chip Select Input
D0-D7	Bidirectional Data Bus
EQIN-	EQual INput (active low)
EQOUT-	EQual OUTput
I0-I7	Input Port
RS	Register Select Input
R/W	Read/Write Input
STRB	Input Data Strobe
VDD	Positive Power Supply
VSS	Internal Logic Ground

1.1 Chip Select Input (CS-)

The Chip Select (CS-) line is a decoded microprocessor address conditioned by Phase 2 (PHI2). When the W65C90 is to be selected, the address should be decoded prior to PHI2 going high edge. When PHI2 goes high, CS- should go low, thus selecting the W65C90.

1.2 Bidirectional Data Bus (D0-D7)

The eight bidirectional data bus lines are used to transfer data between the W65C90 and the microprocessor. During a read operation, the contents of the selected W65C90 internal registers are tranferred to the microprocessor via the Data Bus lines. During a write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to the selected W65C90 register. The Data Bus lines are in the high impedance state when the W65C90 is unselected.

1.3 EQual INput (EQIN-)

EQual INput (EQIN-) is the cascadable input to the compare logic. When EQIN- is low, the EQual OUTput (EQOUT-) will go low if the Compare Data Register (CDR) contents equal the Input Data Register (IDR) contents, which are enabled by the Mask Register (MR) contents. A "1" in the associated MR bit enables the compare for that input data and compare data bit. (See EQOUT- Logic Equation, Table 4-2). When not used in a cascadable form, the EQIN- signal should be tied to VSS.

1.4 EQual OUTput (EQOUT-)

The EQual OUTput (EQOUT-) goes low when the CDR contents "equals" the IDR contents when enabled by the MR.

1.5 Input Ports (I0-I7)

The Input Data Port (I0-I7) is an 8-line bus used for the data input to the comparator. The input data is latched by the Input Data Strobe. The EQOUT- signal follows changes in the IDR contents so while Input Data Strobe is high, EQOUT- could be considered invalid for some applications.

1.6 Register Select Input (RS)

The Register Select (RS) input allows the microprocessor to select one of 3 internal registers. The RS line selects either the CDR or MR during a write operation. The RS line selects either the IDR or MR during a read operation. If RS is a logic "1", the Read/Write (R/W) input will determine if a read of the IDR or a write of the CDR is done. If RS is a logic "0", the R/W input will determine if a read or write of the MR is done.

1.7 Read/Write Input (R/W)

The Read/Write (R/W) signal is generated by the microprocessor and is used to control the transfer of data between the W65C90 and the microprocessor. When R/W is in the high state (Logic 1) and the chip is selected (CS-=0), data is transferred from the W65C90 to the microprocessor (Read Operation). Conversely, when R/W is in the low state (Logic 0) and the chip is selected (CS-=0), data is transferred from the microprocessor to the selected W65C90 register (Write Operation). R/W must always be set up prior to the W65C90 CS- negative edge.

1.8 Input Data Strobe (STRB)

The Input Data Strobe (STRB) signal loads data from the input port lines I0-I7 into the IDR when STRB equals a logic "1". When STRB goes low (logic "0"), the port I/O data lines are latched in the IDR and I0-I7 may now change without changing the IDR values. The STRB signal should be used to "capture" data in the IDR when the I/O, Data Bus, Multiplexed Data line, or other changing signal tied to I0-I7 change before the microprocessor can read the IDR.

1.9 VDD and VSS (VDD, VSS)

VDD is the positive supply voltage and VSS is the system logic ground.

SECTION 2

TIMING, AC AND DC CHARACTERISTICS

2.1 Absolute Maximum Ratings

Table 2-1 Absolute Maximum Ratings

Rating	Symbol	Value
Supply Voltage	VDD	-0.3 to +7.0V
Input Voltage	VIN	-0.3 to VDD +0.3V
Operating Temperature	TA	0 °C to +70°C
Storage Temperature	TS	-55 °C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Note: Exceeding these ratings may result in permanent damage.
Functional operation under these conditions is not implied.

2.2 DC Characteristics: VDD=5.0V +/- 10%, VSS=0V, TA=0 °C to +70°C

Table 2-2 DC Characteristics

Parameter	Symbol	Min	Max	Unit
Input High Voltage	Vih	2.0	VDD + 0.3	V
Input Low Voltage	Vil	-0.3	0.8	V
Leakage Current (all pins) (25oC) Vin = .05V, 5.45V	Iin	-	+/-30	nA
Output Low Current (D0-D7) Vol= 0.4V (EQOUT-)	Iol	3.2	-	mA
Output High Current (D0-D7) Voh= 2.4V (EQOUT-)	Ioh	-3.2	-	mA
Supply Current (No load)	Idd	-	0.5	mA/MHz
Standby Current (25oC) (Inputs= VDD) (No load)	Isby	-	50.0	uA
Pin Capacitance, f= 1MHz	C	-	10.0	pF

2.3 Low Voltage AC Characteristics: VDD=1.8V to 5.5V, VSS=0V, TA=0 °C to +70°C
Notes 1,2

Table 2-3 Low Voltage AC Characteristics

Parameter	Symbol	250 KHz Min	250 KHz Max
Chip Select Cycle Time	tCYC	4000	inf
Chip Select Clock Width Low	tCSL	1990	inf
Chip Select Clock Width High	tCSH	1990	inf
Output Rise Time, Fall Time	tOR,tOF	-	100
Access Time	tACC	-	1130
Input Data Setup Time	tIS	320	-
Output Data Delay Time	tOD	-	800
Hold Time	tH	10	-
Capacitive Load (all pins)	CL	-	70

2.4 High Voltage AC Characteristics: VDD=5.0V+/-10%, VSS=0V, TA=0 °C to +70°C
Notes 1,2

Table 2-4 High Voltage AC Characteristics

Parameter	Symbol	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	8 Mhz Min	8 Mhz Max	Unit
Chip Select Cycle Time	tCYC	250	inf	165	inf	125	inf	nS
Chip Select Width Low	tCSL	120	inf	80	inf	60	inf	nS
Chip Select Width High	tCSH	120	inf	80	inf	60	inf	nS
Output Rise and Fall Time	tOR,tOF	-	100	-	100	-	100	nS
Access Time	tACC	-	90	-	60	-	50	nS
Input Setup Time	tIS	20	-	10	-	10	-	nS
Output Delay Time	tOD	-	60	-	40	-	30	nS
Hold Time	tH	10	-	10	-	10	-	nS
Capacitive Load	CL	70		70		70		pF

Notes:

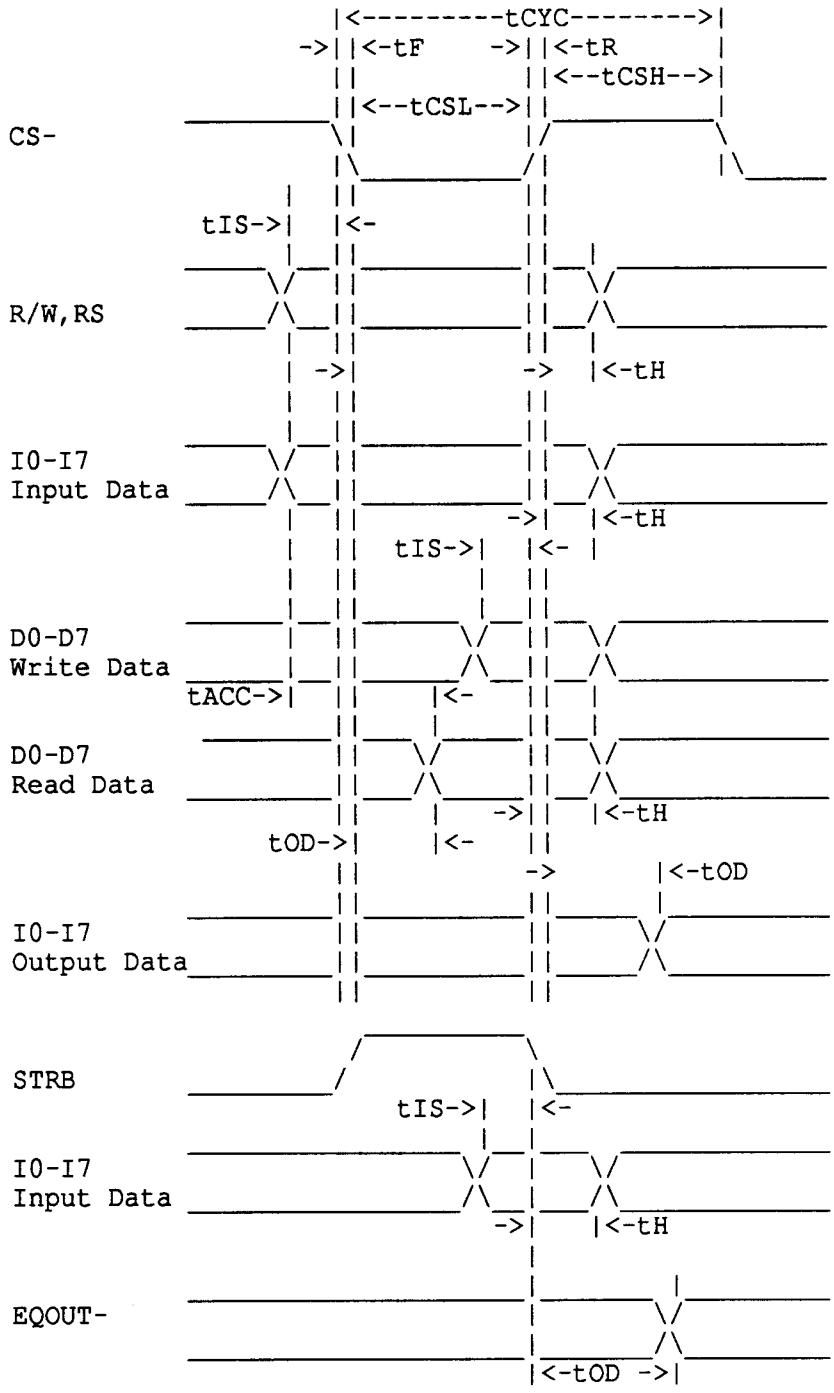
1. The tOR and tOF of 100ns indicate output rise and fall times. The tOR and tOF for all output signals are measured on a sample basis from .3xVDD to .7xVDD.

   The tR and tF are not programmable on the automated test system that is used for production testing. A typical tR and tF is 5-10ns; therefore, the spec indicates the duty cycle of the clock as tested (tCSL=tCYC/2-tF).

   The most critical Rise and Fall times are for CS- because all timing is related to CS-.

   The input Rise and Fall times can affect the input setup time (tIS), output delay time (tOD) and hold time (tH). This must be taken into account in an application. At 4MHz the worst case input Rise and Fall times may prevent a system from working. The CS- input Rise and Fall times will require the application engineer add this time onto the output delay time, input setup time and hold time.

2. Hold Time for all inputs and outputs relative to the appropriate edge of CS- or STRB.



Notes: 1. Voltage levels shown are VL=0.1V, VH=VDDx0.8 for RES-, CS-.
All other inputs are VL=0.4V, VH=2.4V.
2. Measurement points shown are 2.5V.

Figure 2-1 General Timing Diagram

SECTION 3

ORDERING INFORMATION

```
                                  W  65C90 P     -4
Description                       |    |   |   |  |
W-Standard                        |    |   |   |  |
                                  |    |   |   |  |
Product Identification Number     |    |   |   |  |
                                       |   |   |  |
Package                                |   |   |  |
P- 24 pin plastic dual in line package     |   |  |
                                           |   |  |
Temperature/Processing                     |   |  |
Blank- 0oC to +70oC                            |  |
                                               |  |
Performance Designator                         |  |
Designators selected for speed and power
-4 4MHz      -6 6MHz      -8 8MHz      -10 10MHz
```

General sales or technical assistance, and information about devices supplied to a custom specification may be requested from:

The Western Design Center, Inc.
2166 East Brown Road
Mesa, Arizona 85213
Phone: 602-962-4545 Fax: 602-835-6442

WARNING:

MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

SECTION 4

APPLICATION INFORMATION

* Bus monitor device for address, data, control, or I/O
* Address comparator for "breakpoint" generation
* Address bounds register for memory management
* ABORT generation for the W65C816 16-bit microprocessor for memory management

Table 4-1 W65C90 Truth Table

CS-	RS	R/W	DATA BUS
H	X	X	Hi-Z
L	L	L	Write Mask Register (MR)
L	L	H	Read Mask Register (MR)
L	H	L	Write Compare Data Register (CDR)
L	H	H	Read Input Data Register (IDR)

STRB	Input Data Register (IDR)
H	I/O Data into Input Data Register (IDR)
L	I/O Data Latched into Register (IDR)

Table 4-2 EQOUT- Logic Equation

$$EQOUT = EQIN \cdot (\overline{MR0} + CDR0 \cdot IDR0 + \overline{CDR0} \cdot \overline{IDR0}) \cdot$$
$$(\overline{MR1} + CDR1 \cdot IDR1 + \overline{CDR1} \cdot IDR1) \cdot$$
$$(\overline{MR2} + CDR2 \cdot IDR2 + \overline{CDR2} \cdot \overline{IDR2}) \cdot$$
$$(\overline{MR3} + CDR3 \cdot IDR3 + \overline{CDR3} \cdot \overline{IDR3}) \cdot$$
$$(\overline{MR4} + CDR4 \cdot IDR4 + \overline{CDR4} \cdot \overline{IDR4}) \cdot$$
$$(\overline{MR5} + CDR5 \cdot IDR5 + \overline{CDR5} \cdot \overline{IDR5}) \cdot$$
$$(\overline{MR6} + CDR6 \cdot IDR6 + \overline{CDR6} \cdot \overline{IDR6}) \cdot$$
$$(\overline{MR7} + CDR7 \cdot IDR7 + \overline{CDR7} \cdot IDR7) \cdot$$

NOTE: EQOUT- is the compliment of EQOUT.