FINAL

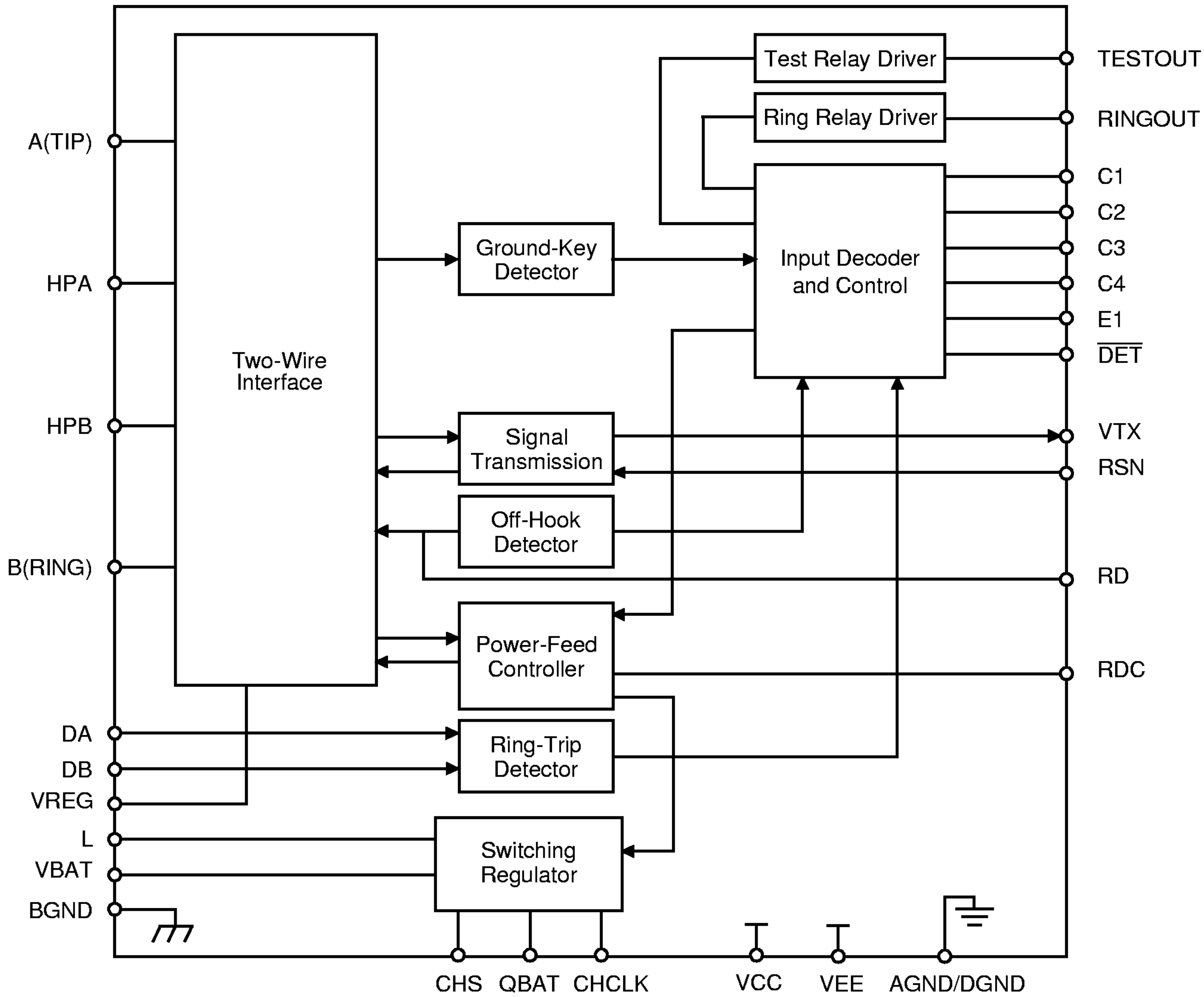
Am79512/4

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Programmable constant-current feed
- Programmable loop-detect threshold
- On-chip switching regulator for low-power dissipation
- Polarity reversal feature
- Optimized for –60 V battery
- Line feed characteristics independent of battery variations
- Two-wire impedance set by single external impedance
- Tip Open state for ground-start lines
- Ring and test relay drivers
- On-hook transmission

BLOCK DIAGRAM



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Issue Date: **July 1998**

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am7951X **–1** **J** **C**

TEMPERATURE RANGE
C = Commercial (0°C to 70°C)*

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)
P = 28-pin Plastic DIP (PD 028)
D = 28-pin Ceramic DIP (CD 028)

PERFORMANCE GRADE
–1 = Performance Grading
–2 = Performance Grading

DEVICE NUMBER/DESCRIPTION
Am7951X
Subscriber Line Interface Circuit

Valid Combinations		
Am7951X	–1 –2	DC JC PC

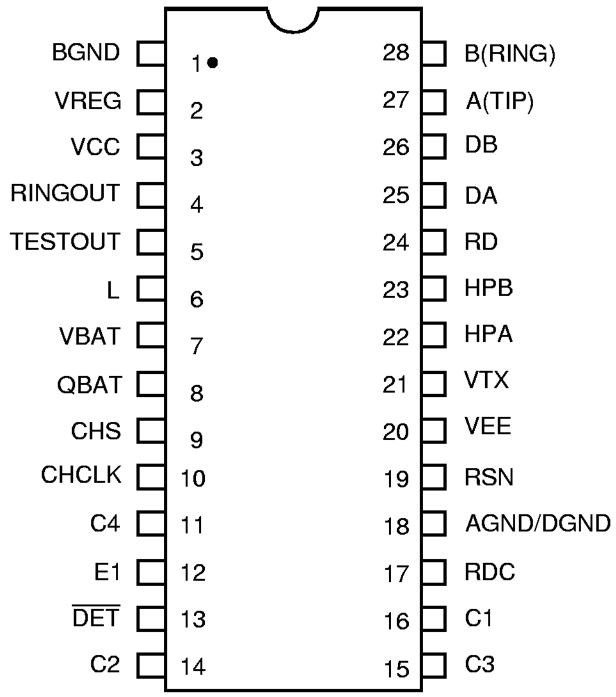
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

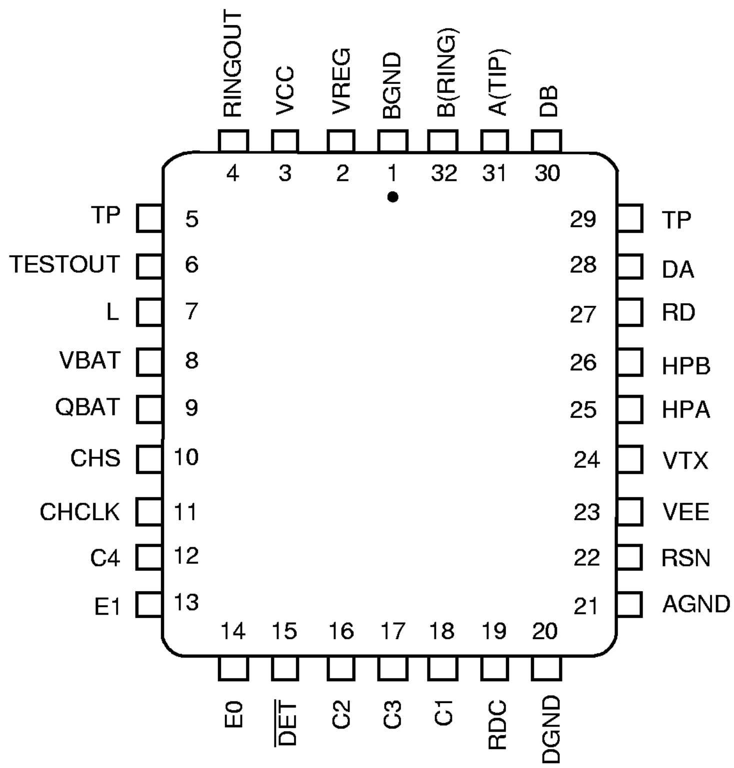
Note:
** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAMS
Top View

Am79512



Am79514



Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate.*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND	Gnd	(Am79514) Analog ground
AGND/DGND	Gnd	(Am79512) Analog and Digital ground are connected internally to a single pin.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Inputs	Decoder. C3 is MSB and C1 is LSB.
C4	Input	TTL compatible. A logic High enables the driver.
CHCLK	Input	Input to switching regulator (TTL compatible) Frequency = 256 kHz (nominal).
CHS	Input	Chopper Stabilization. Connection for external stabilization components.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
DET	Output	Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1 and E1 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
DGND	Gnd	(Am79514) Digital ground.
E0	Input	Read enable. A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$.
E1	Input	E1 = High connects the ground-key detector to $\overline{DET}$, and E1 = Low connects the off-hook or ring-trip detector to $\overline{DET}$.
HPA	Capacitor	High-pass filter capacitor; A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor; B(RING) side of high-pass filter capacitor.
L	Output	Switching Regulator Power Transistor. Connection point for filter inductor and anode of catch diode. Has up to 60 V pulse waveform; isolated from sensitive circuits. You must keep the diode connections short because of the high currents and high di/dt.
QBAT	Battery	Quiet battery. Filtered battery supply for the signal processing circuits. Connect external 100 Ω, 1/8 Ω resistor between QBAT and VBAT pins.
RD	Resistor	Detector resistor. Threshold modification/filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network, which also connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver; sourcing from BGND with internal diode to QBAT.
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) = 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Route the 256-kHz chopper clock and switch lines away from the RSN node.
TESTOUT	Output	Test relay driver. Sourcing from BGND with internal diode to QBAT.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation
VBAT	Battery	Battery supply.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VREG	Input	Regulated voltage. Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio; Unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature .... –55°C to +150°C

V_{CC} with respect to AGND/DGND ..... –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND...... +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND..... +0.4 V to –70 V

Note: *Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.*

BGND with respect to AGND/DGND.. +1.0 V to –3.0 V

A(TIP) or B(RING) to BGND:

Continuous .... –70 V to +1.0 V
10 ms (f = 0.1 Hz) .... –70 V to +5.0 V
1 µs (f = 0.1 Hz) .... –90 V to +10 V
250 ns (f = 0.1 Hz) .... –120 V to +15 V

Current from A(TIP) or B(RING)....................... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT .... BGND to 70 V above Q_{BAT}

Current through relay drivers .... 60 mA

Voltage on ring-trip inputs DA and DB .... V_{BAT} to 0 V

Current into ring-trip inputs................................. ±10 mA

Peak current into regulator switch (L pin) .... 150 mA

Switcher transient peak off voltage on L pin ...... +1.0 V

C4–C1, E1, CHCLK,
to AGND/DGND .... –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, (see note) ...... T_A = 70°C

In 28-pin ceramic DIP package.................... 2.58 W
In 28-pin plastic DIP package .... 1.4 W
In 32-pin PLCC package.............................. 1.74 W

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature .... 0°C to +70°C*

V_{CC} .... 4.75 V to 5.25 V

V_{EE} .... –4.75 V to –5.25 V

V_{BAT} .... –40 V to –63 V

AGND/DGND .... 0 V

BGND with respect to
AGND/DGND........................ –100 mV to +100 mV

Load resistance on VTX to ground .... 10 kΩ min

Operating Ranges define those limits between which the functionality of the device is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Analog (V_{TX}) output impedance			3	20	W	
Analog (V_{TX}) output offset	0°C to +70°C –40°C to +85°C	–35 –40		+35 +40	mV	— 4
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	W	
Longitudinal impedance at A or B				35		
Overload level Z_{2WIN} = 600 Ω to 900 Ω	4-wire 2-wire	–3.1 –3.1		+3.1 +3.1	Vpk	2 —
Transmission Performance, 2-Wire Impedance						
2-wire return loss (See Test Circuit D)	300 Hz to 500 Hz 500 Hz to 2500 Hz 2500 Hz to 3400 Hz	26 26 20			dB	4 — —
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C)						
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz: –1* normal polarity 0°C to +70°C –2 normal polarity –40°C to+85°C –2 reverse polarity –2	50 63 58 58			dB	 5
	1 kHz to 3.4 kHz: –1* normal polarity 0°C to +70°C –2 normal polarity –40°C to +85°C –2 reverse polarity –2	52 58 54 54				
Longitudinal sum (L-T) + (T-L)	300 to 3400 Hz	95				
Longitudinal signal generation 4-L or T-L	300 to 800 Hz 800 to 3400 Hz	40 35				
Longitudinal current capability per wire	Active state OHT state			17 8	mArms	
Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B)						
Gain accuracy	0 dBm, 1 kHz, 0°C to +70°C 0 dBm, 1 kHz, –40°C to +85°C 0 dBm, 1 kHz, 0°C to +70°C –1* 0 dBm, 1 kHz, –40°C to +85°C –1	 –0.15 –0.20 –0.1 –0.15		 +0.15 +0.20 +0.1 +0.15	dB	 4 4
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz 0°C to +70°C –40°C to +85°C	 –0.1 –0.15		 +0.1 +0.15		 4
Gain tracking	+7 dBm to –55 dBm 0°C to +70°C –40°C to +85°C	 –0.1 –0.15		 +0.1 +0.15		

Note:
** P.G. = Performance Grade*

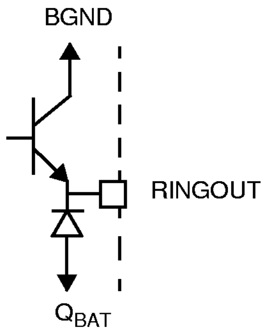
ELECTRICAL CHARACTERISTICS (CONTINUED)

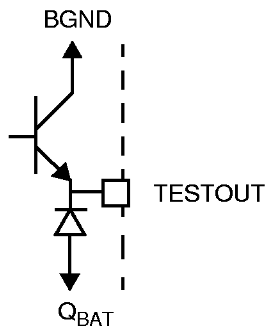
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Balance Return Signal (4-Wire to 4-Wire, See Test Circuit B)						
Gain accuracy	0 dBm, 1 kHz, 0°C to +70°C 0 dBm, 1 kHz, –40°C to +85°C 0 dBm, 1 kHz, 0°C to +70°C –1* 0 dBm, 1 kHz, –40°C to +85°C –1	–0.15 –0.20 –0.1 –0.15		+0.15 +0.20 +0.1 +0.15	dB	 4 4
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz 0°C to +70°C –40°C to +85°C	–0.1 –0.15		+0.1 +0.15	dB	 4
Gain tracking	+7 dBm to –55 dBm 0°C to +70°C –40°C to +85°C	–0.1 –0.15		+0.1 +0.15	dB	
Group delay	f = 1 kHz		5.3		µs	
Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire, See Test Circuits A and B)						
Distortion level	0 dBm, 300 Hz to 3400 Hz		–64	–50	dB	
Distortion level	+9 dBm		–55	–40	dB	
Idle Channel Noise						
Psophometric weighted noise	2-wire 0°C to +70°C 2-wire –40°C to +85°C		–83 –83	–78 –75	dBmp	7 4, 7
	4-wire 0°C to +70°C 4-wire –40°C to +85°C		–83 –83	–78 –75	dBmp	7 4, 7
Single Frequency Out-of-Band Noise (See Test Circuit E)						
Metallic	4 kHz to 9 kHz 9 kHz to 1 MHz 256 kHz and harmonics		–76 –76 –57		dBm	 4, 5, 9 4, 5
Longitudinal	1 kHz to 15 kHz Above 15 kHz 256 kHz and harmonics		–70 –85 –57		dBm	 4, 5, 9 4, 5
DC Feed Current and Voltage (See Figure 1) Unless otherwise noted, Battery = 60 V (V_{BAT} = –59.3 V)						
Active state loop-current accuracy	I_{LOOP} (nominal) = 40 mA R_L = 2000 Ω, Battery = 62 V –1* R_L = 2080 Ω –2	–7.5 23 22.7		+7.5	% mA mA	 4
On-hook loop voltage	R_L = ∞	47.5	49		V	
OHT state Tip Open state Disconnect state	R_L = 600 Ω R_L = 600 Ω R_L = 0	18	20	22 1.0 1.0	mA	
Power Dissipation, Battery = –60 V						
On-hook Open Circuit state On-hook OHT state On-hook Active state Off-hook OHT state Off-hook Active state	 R_L = 600 Ω R_L = 600 Ω		50 175 260 500 650	120 250 400 750 1000	mW	

ELECTRICAL CHARACTERISTICS (CONTINUED)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Supply Currents						
V_{CC} On-hook supply current	Open Circuit state OHT state Active state		3 6 7.5	4.5 10 12	mA	
V_{EE} On-hook supply current	Open Circuit state OHT state Active state		1.0 2.2 2.7	2.3 3.5 6.0	mA	
V_{BAT} On-hook supply current	Open Circuit state OHT state Active state		0.4 3.0 4.0	1.0 5.0 6.0	mA	
Power Supply Rejection Ratio (V_{RIPPLE} = 50 mVrms)						
V_{CC}	40 Hz to 3400 Hz 3.4 kHz to 50 kHz	20 20	35 30		dB	6, 7 —
V_{EE}	40 Hz to 3400 Hz 3.4 kHz to 50 kHz	20 15	30 25		dB	6, 7 —
V_{BAT}	40 Hz to 3400 Hz 3.4 kHz to 50 kHz	27 20	30 30		dB	6, 7 —
Off-Hook Detector						
Current threshold	$I_{DET} = 365/R_D$	–20		+20	%	
Ground-Key Detector Thresholds Active State, Battery = –60 V						
Ground-key resistance threshold	B(RING) to GND	2.0	4.2	10.0	kΩ	
Ground-key current threshold	B(RING) or midpoint to GND		9		mA	8
Ring-Trip Detector Input						
Bias current		–5	–0.05		µA	
Offset voltage	Source resistance = 0 to 200 kΩ	–50	0	+50	mV	
Logic Inputs (C4–C1, E1, and CHCLK)						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current	All inputs except E1 Input E1	–75 –75		40 45	µA	
Input Low current		–0.4			mA	
Logic Output ($\overline{DET}$)						
Output Low voltage	I_{OUT} = 0.8 mA			0.4	V	
Output High voltage	I_{OUT} = –0.1 mA	2.4			V	
Relay Driver Outputs (RINGOUT, TESTOUT)						
On voltage	50 mA source	B_{GND} –2			V	
Off leakage			0.5	100	µA	
Clamp voltage	50 mA sink	Q_{BAT} –2			V	

RELAY DRIVER SCHEMATICS



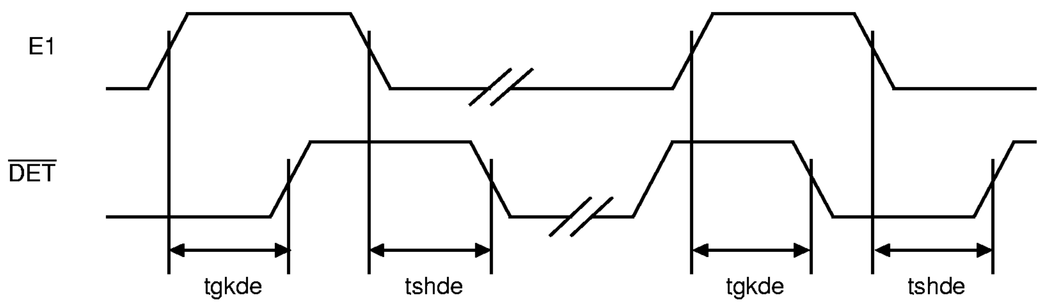


SWITCHING CHARACTERISTICS

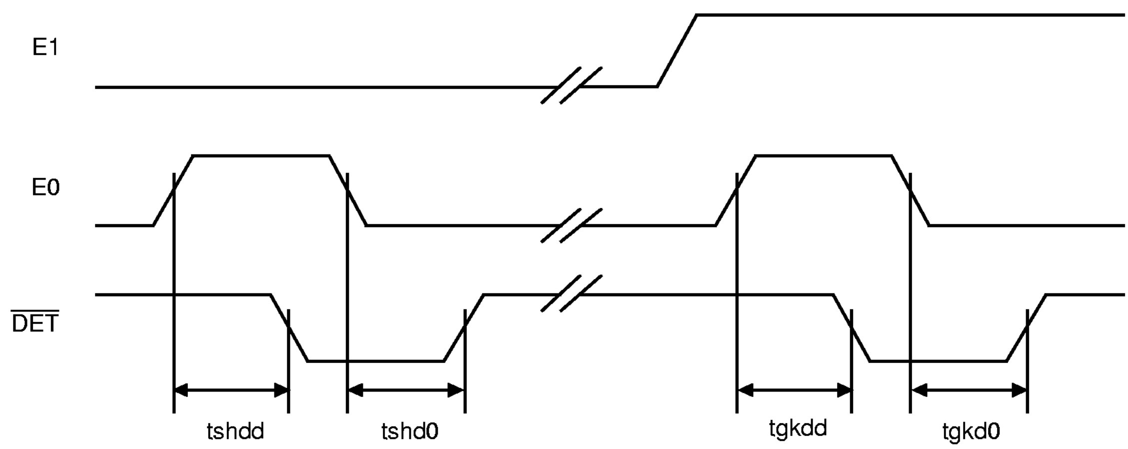
Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-key Detect state R_L open, R_G connected (See Figure H)	0°C to +70°C –40°C to +85°C			3.8 4.0	µs	4
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to +70°C –40°C to +85°C			1.1 1.6		
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)		0°C to +70°C –40°C to +85°C			1.1 1.6		
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)		0°C to +70°C –40°C to +85°C			3.8 4.0		
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switchhook Detect state R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C –40°C to +85°C			1.2 1.7		
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C –40°C to +85°C			3.8 4.0		
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)		0°C to +70°C –40°C to +85°C			1.1 1.6		
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)		0°C to +70°C –40°C to +85°C			3.8 4.0		

SWITCHING WAVEFORMS

E1 to $\overline{DET}$



E0 to $\overline{DET}$



Note:
All delays measured at 1.4 V level.

Notes:

1. *Unless otherwise noted, test conditions are BAT = –60 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 0.33 μF, R_{DC1} = R_{DC2} = 31.25 kΩ, C_{DC} = 0.1 μF, Rd = 51.1 kΩ, no fuse resistors, two-wire AC output impedance programming impedance (Z_T) = 600 kΩ resistive, receive input summing impedance (Z_{RX}) = 300 kΩ resistive. (See Table 2 for component formulas.)*
2. *Overload level is defined when THD = 1%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *These tests are performed with a longitudinal impedance of 90 Ω and metallic impedance of 300 Ω for frequencies below 12 kHz and 135 Ω for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout. Please refer to application notes for details.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
7. *When the SLIC is in the Anti-Sat 2 operating region, this parameter is degraded. The exact degradation depends on system design. The Anti-Sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than approximately 15 V.*
8. *"Midpoint" is defined as the connection point between two 300 Ω series resistors connected between A(TIP) and B(RING).*
9. *Fundamental and harmonics from 256 kHz switch regulator chopper are not included.*

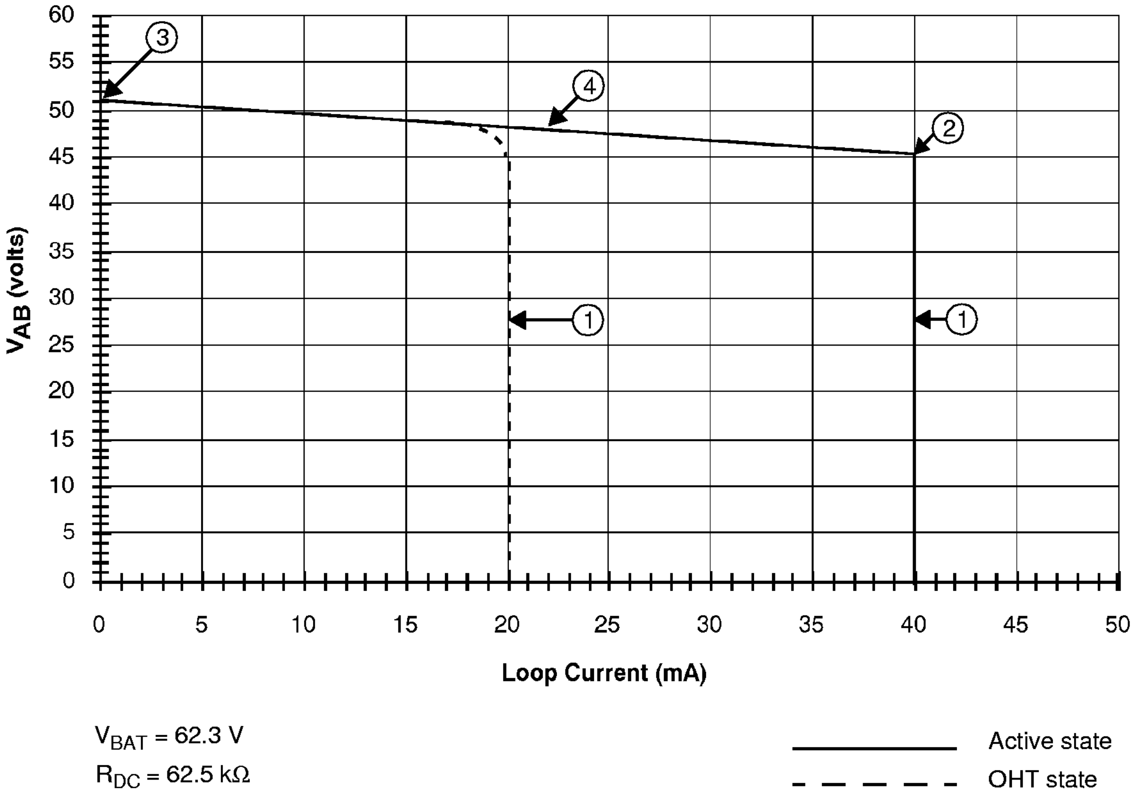
Table 1. SLIC Decoding

State	C3 C2 C1	Two-Wire Status	$\overline{DET}$ Output E1 = 0	$\overline{DET}$ Output E1 = 1
0	0 0 0	Open Circuit	Ring trip	Ring trip
1	0 0 1	Ringing	Ring trip	Ring trip
2	0 1 0	Active	Loop detector	Ground key
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key
4	1 0 0	Tip Open	Loop detector	—
5	1 0 1	Reserved	Loop detector	—
6	1 1 0	Active Polarity Reversal	Loop detector	Ground key
7	1 1 1	OHT Polarity Reversal	Loop detector	Ground key

Table 2. User-Programmable Components

$Z_T = 1000(Z_{2WIN} - 2R_F)$	Where Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{1000 \bullet Z_T}{Z_T + 1000(Z_L + 2R_F)}$	Where Z_{RX} is connected from V_{RX} to the RSN pin, Z_T is defined above, G_{42L} is the desired receive gain, and Z_L is the 2-wire load impedance.
$R_{DC1} + R_{DC2} = \frac{2500}{I_{FEED}}$	Where R_{DC1}, R_{DC2}, and C_{DC} form the network C_{DC} = (1.5 ms)(R_{DC1} + R_{DC2})/($R_{DC1} \bullet R_{DC2}$) connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = \frac{365}{I_T}, \quad C_D = \frac{0.5\ ms}{R_D}$	Where R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on hook and off hook.

DC FEED CHARACTERISTICS



Notes:

1. *Constant-current region:*

Active state, $I_L = \frac{2500}{R_{DC}}$

OHT state, $I_L = \frac{1}{2} \bullet \frac{2500}{R_{DC}}$

2. *Anti-sat cut-in:*
   $V_{AB} = 46\ V, \qquad |V_{BAT}| \geq 58.9\ V$
   $V_{AB} = 1.087|V_{BAT}| - 18.017, \qquad |V_{BAT}| < 58.9\ V$

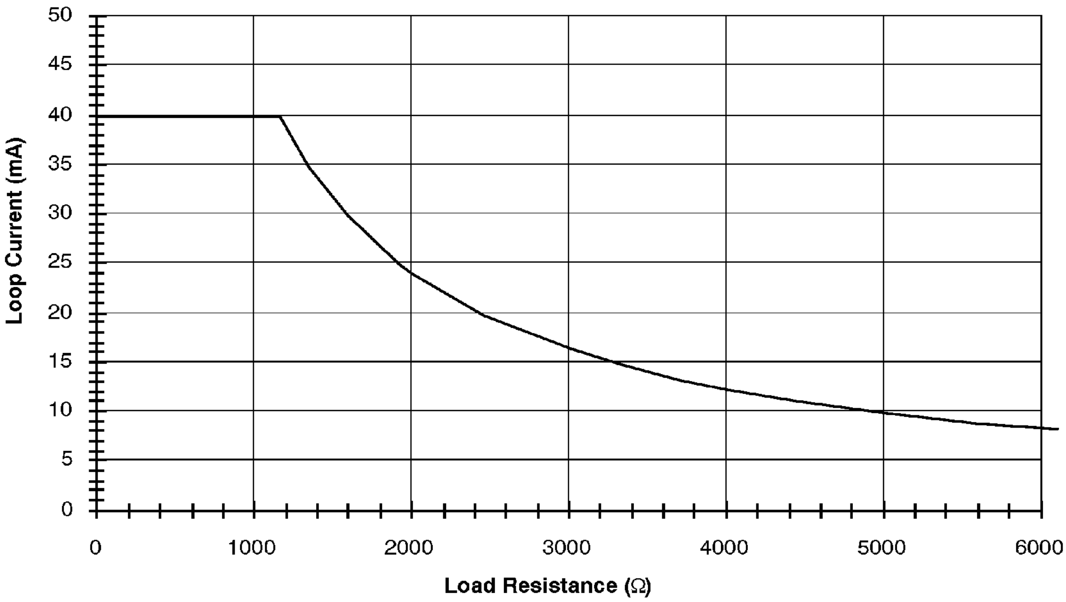
3. *Open Circuit voltage:*
   $V_{AB} = 51.23\ V, \qquad |V_{BAT}| \geq 61.5\ V$
   $V_{AB} = 1.073|V_{BAT}| - 14.72, \qquad |V_{BAT}| < 61.5\ V$

4. *Anti-sat 1 region:*
   $V_{AB} = 51.23 - I_L \frac{R_{DC}}{488.3}$

5. *Anti-sat 2 region:*
   $V_{AB} = 1.073|V_{BAT}| - 14.72 - I_L \frac{R_{DC}}{1071}$

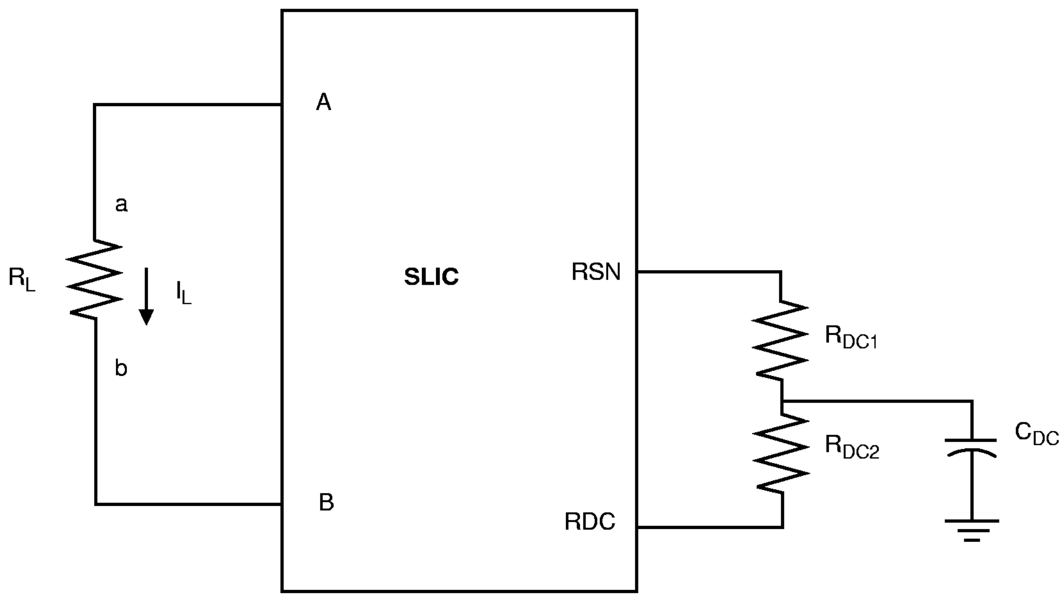
a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)



V_{BAT} = 62.3 V
R_{DC} = 62.5 kΩ

b. Loop Current vs. Load Resistance (Typical)

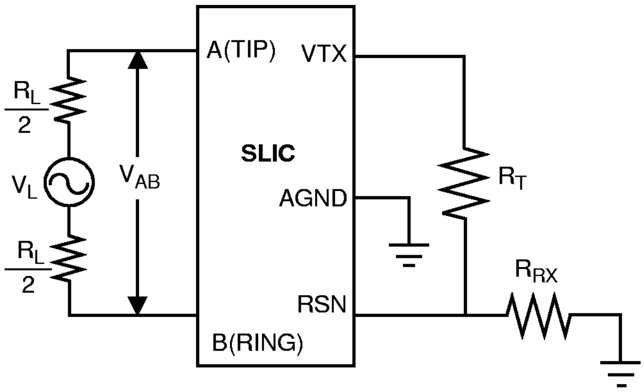


Feed current programmed by R_{DC1} and R_{DC2}

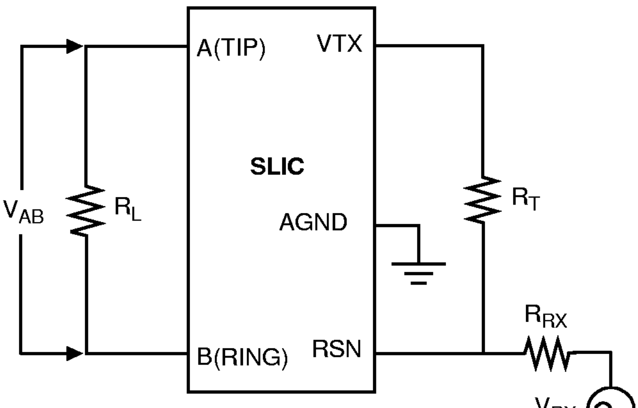
c. Feed Programming

Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

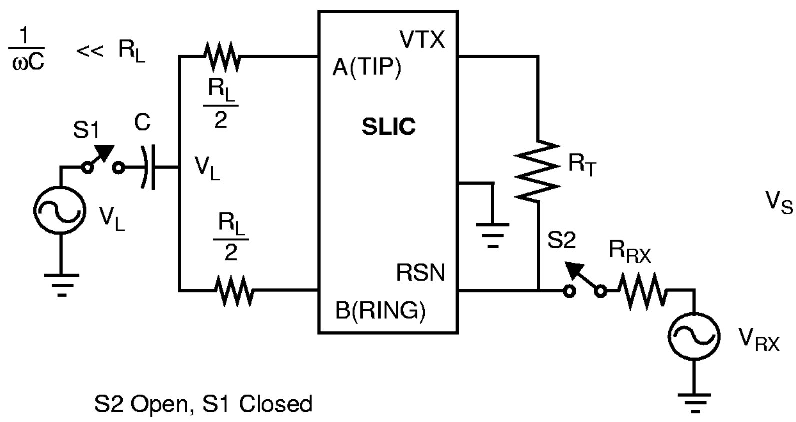


$I_{L4-2} = 20 \log (V_{AB} / V_{TX})$

$BRS = 20 \log (V_{TX} / V_{AB})$

A. Two- to Four-Wire Insertion Loss

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

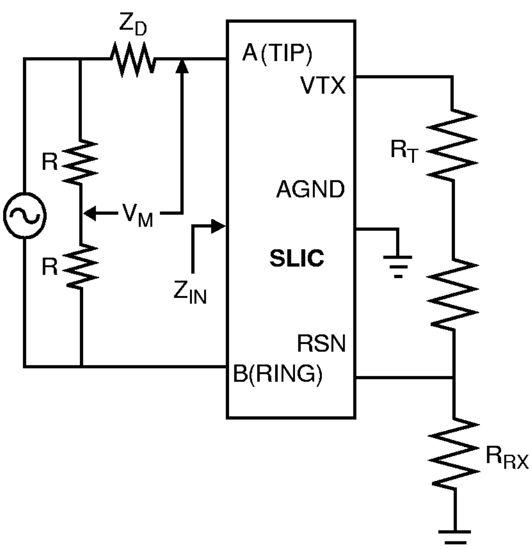
L-T Long. Bal. = $20 \log (V_{AB} / V_L)$

L-4 Long. Bal. = $20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open

4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance

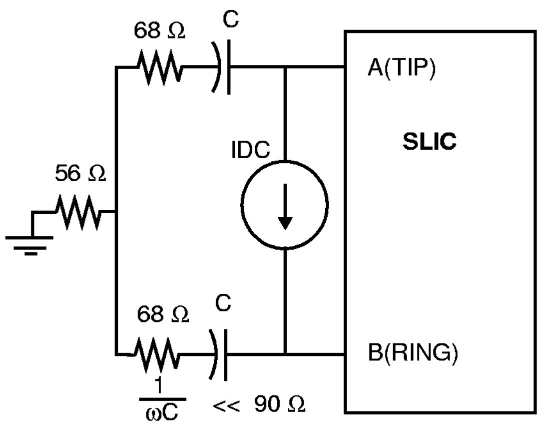


Note:
ZD is the desired impedance (e.g., the characteristic impedance of the line).

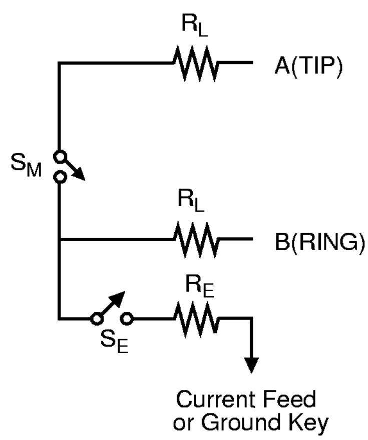
$R_L = -20 \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

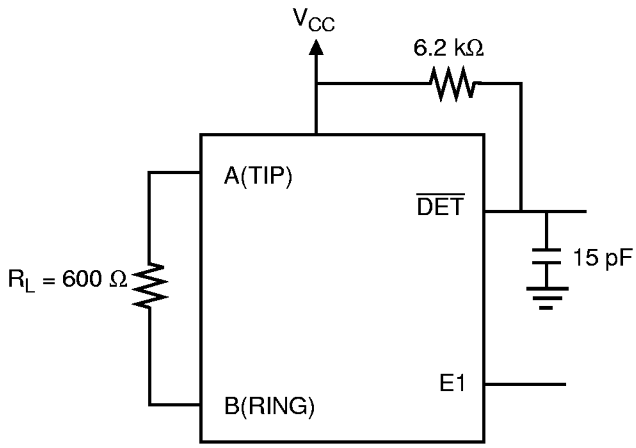
TEST CIRCUITS (continued)



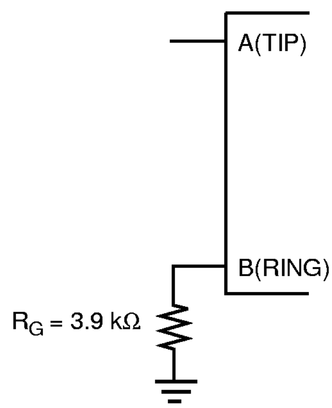
E. Single-Frequency Noise



F. Ground-Key Detection



G. Loop-Detector Switching



H. Ground-Key Switching

REVISION SUMMARY

Revision A to Revision B

- Minor changes were made to the data sheet style and format to conform to AMD standards.

Revision B to Revision C

- In Pin Description table, inserted/changed TP pin description to: "Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation."
- Minor changes were made to the data sheet style and format to conform to AMD standards.

Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

The count registers should be programmed before attempting to use the timers, since they are not automatically initialized to zero.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while Timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two MAX COUNT values whenever the current maximum count is reached. A timer resets when the timer count register equals the MAX COUNT value being used. If the timer count register or the MAX COUNT register is changed so that the MAX COUNT is less than the timer count the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the MAX COUNT value, and then resets.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going High.
- The contents of the count registers are indeterminate.

INTERRUPT CONTROLLER

The 80C186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80C186 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 19.

The 80C186 has a special slave mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register (see Slave Mode section).

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (cascade mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (cascade mode) with externally generated interrupt vectors.

External sources in the cascade mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80C186 on the second cycle. The capability to interface to external 82C59A programmable interrupt controllers is provided when the inputs are configured in cascade mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the 82C59A. The interrupt controller responds identically to internal interrupts in all three modes; the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

Fully Nested Mode

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 20. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate

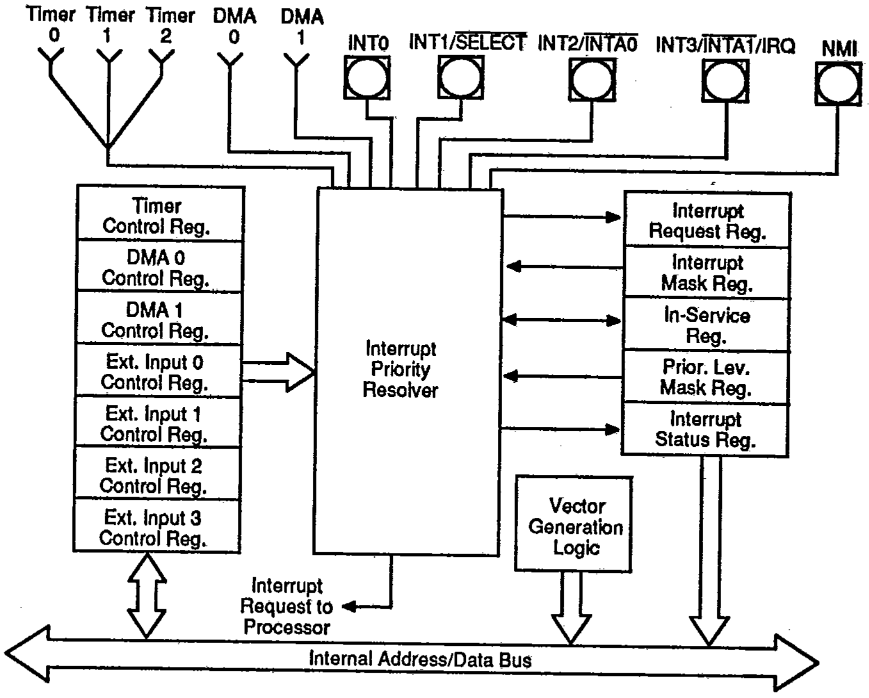


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Figure 19. Interrupt Controller Block Diagram

Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 3).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 3 is used. If the serviced interrupt routine reenables interrupts, it allows other interrupt requests to be serviced.

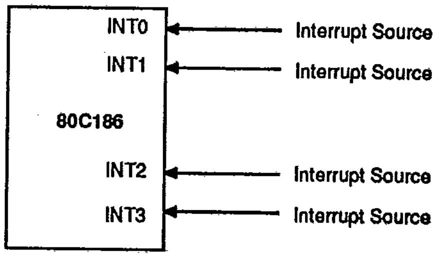

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Figure 20. Fully Nested (Direct) Mode Interrupt Controller Connections

SWITCHING CHARACTERISTICS (continued)

Ready, Peripheral, and Queue Status Timings

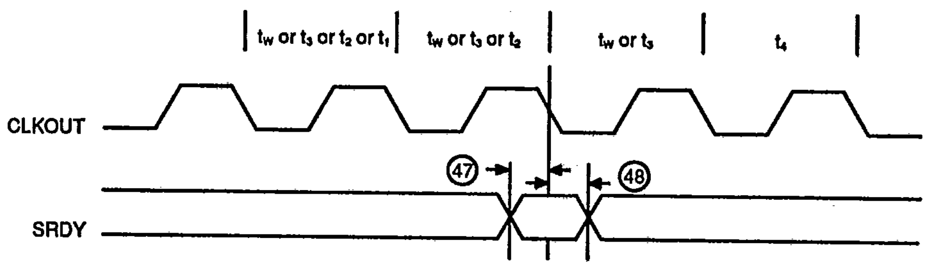
$T_A = 0°C$ to $+70°C$, $V_{CC} = 5$ V ±10% except $V_{CC} = 5$ V ±5% at f > 12.5 MHz

			Preliminary								
			80C186		80C186-12		80C186-16		80C186-20		
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit
80C186 Ready and Peripheral Timing Requirements											
47	t_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		15		15		10		ns
48	t_{CLSRY}	SRDY Transition Hold Time(1)	15		15		15		10		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		15		15		10		ns
50	t_{CLARX}	ARDY Active Hold Time(1)	15		15		15		10		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	15		15		15		10		ns
52	t_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		25		25		20		ns
53	t_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	15		15		15		15		ns
54	t_{INVCL}	DRQ0, DRQ1, Setup Time(2)	15		15		15		15		ns
80C186 Peripheral and Queue Status Timing Responses											
55	t_{CLTMV}	Timer Output Delay		40		33		27		25	ns
56	t_{CHQSV}	Queue Status Delay		37		32		30		23	ns

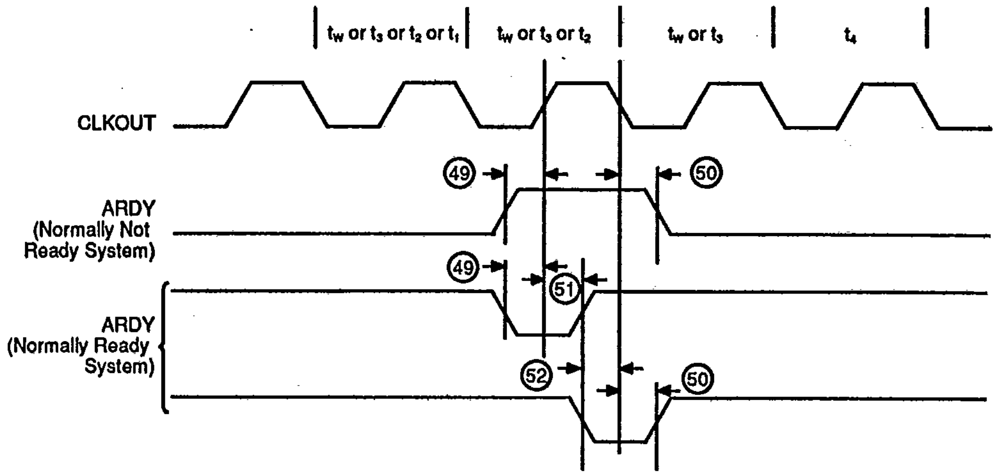
All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50–200$ pF (10 MHz) and $C_L = 50–100$ pF (12.5–20 MHz).
For AC tests, input $V_{IL} = 0.45$ V and $V_{IH} = 2.4$ V except at X_1 where $V_{IH} = V_{CC} - 0.5$ V.

Notes: 1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

Synchronous Ready (SRDY) Waveforms



Asynchronous Ready (ARDY) Waveforms



Peripheral and Queue Status Waveforms