•Creation Date: February 1994
Revision Date: June 6, 1996

Aptos SEMICONDUCTOR

AP32M128

128K x 32 Static RAM Module

Features

- High-density, 4-megabit, asynchronous Static RAM
- Low profile FR-4 SIMM
- High-speed, -15*, -20 and -25 ns
- Single 5V 10% power supply
- TTL-compatible inputs and outputs
- JEDEC-compatible pinout

Functional Description

The Aptos AP32M128 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four, 128K x 8 fast static RAMS mounted on a 64-pin, double-sided, FR-4-printed circuit board.

The AP32M128 offers the optimum in packaging density and profile height. It is packaged on a 64-lead SIMM (single in-line memory module). The dual row configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.58 inches high, this low profile package is ideal for systems with minimum board spacing.

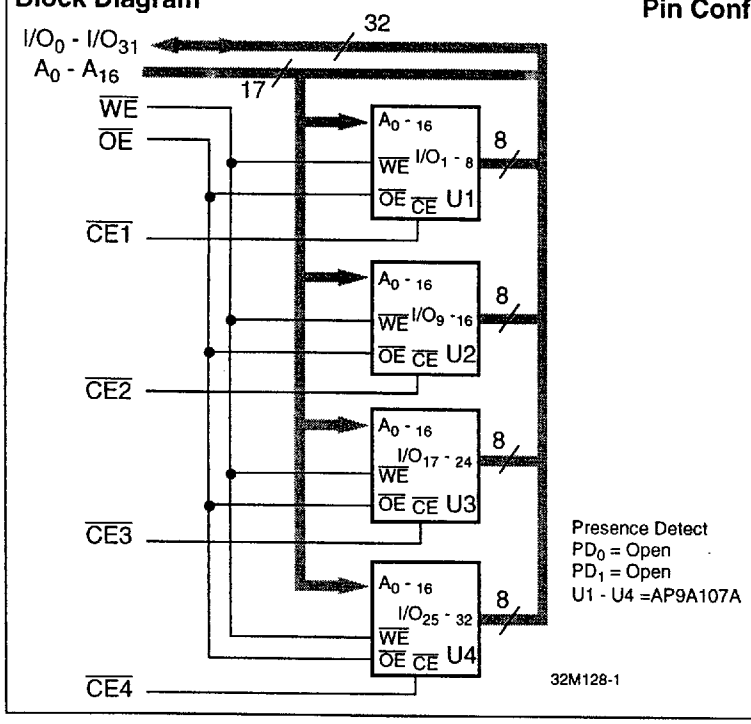
All inputs and outputs of the AP32M128 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Reading the device is accomplished by taking the chip select ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

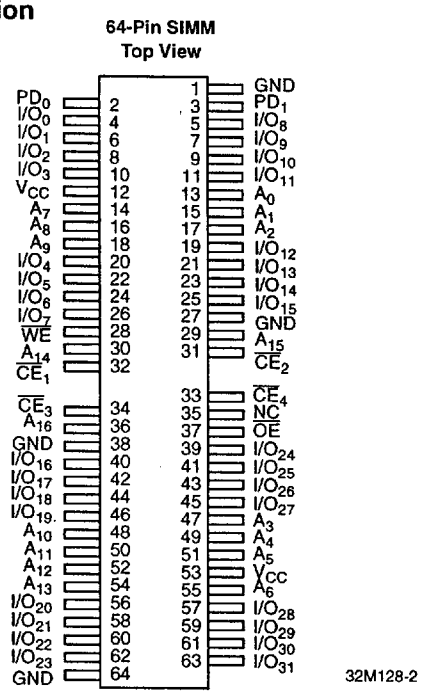
Writing to each byte is accomplished when the appropriate chip select and write enable inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{16}).

PD_0 and PD_1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, $\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ and $\overline{CE}_4$, are used to enable the module's 4 bytes independently.

Block Diagram



Pin Configuration



Selection Guide

	AP32M128-15	AP32M128-20	AP32M128-25
Maximum Access Time (ns)	15	20	25
Maximum Operating Current (mA)	760	620	500
Maximum Standby Current (mA)	20	20	20

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... -55 C to +125 C

Ambient Temperature with Power Applied..... -0 C to +70 C

V_{CC} Supply Relative to GND .....-0.5 V to +7.0 V

Voltage on Any Pin Relative to GND-0.5 V to V_{CC} +0.5 V

Short Circuit Output Current[1]40 mA

Power Dissipation4.0 W

Electrical Characteristics Over the Operating Range (0 C T A 70 C, V CC = 5V 10%)

Symbol	Parameter	Test Conditions	32M128-15		32M128-20		32M128-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current [2]			760		620		500	mA
I_{SB1}	TTL Standby Current -TTL Inputs	$\overline{CE}$ V_{IH}, I_{OUT} = 0		180		140		120	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	$\overline{CE}$ V_{CC} -0.2 V, I_{OUT} = 0		20		20		20	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	-20	20	-20	20	-20	20	A
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-5	5	-5	5	-5	5	A
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage [3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Capacitance (T_A = 25 C, f=1, V_{CC} = 5V)[4]

Symbol	Description	Max.	Unit
C_{I1} (A_0 - A_{17}, $\overline{WE}$, $\overline{OE}$)	Input Capacitance	35	pF
C_{I2} ($\overline{CE}_1$ - $\overline{CE}_4$)	Input Capacitance	10	pF
C_{I3} (I/O_0 - I/O_{31})	I/O Capacitance	10	pF

Notes:

1. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.
3. Negative undershoot of up to 3.0 V is permitted once per cycle.
4. Sample tested, only.

Switching Characteristics Over the Operating Range[5, 6]

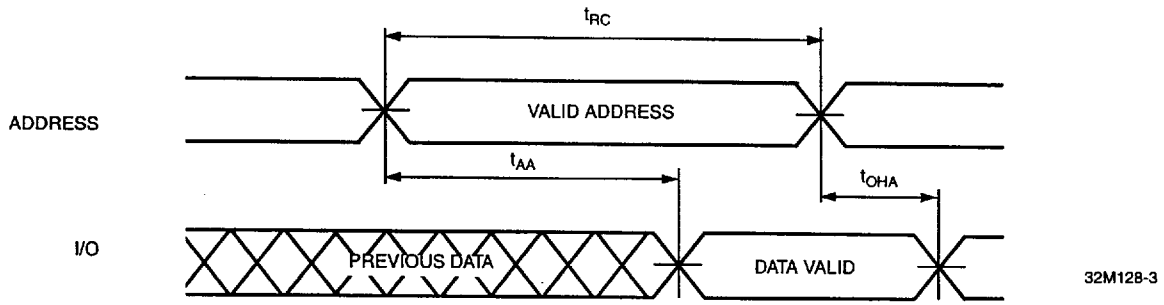
Parameter	Description	32M128-15		32M128-20		32M128-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	15		20		25		ns
t_{AA}	Address Access Time		15		20		25	ns
t_{OHA}	Output Hold Time	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Valid Data		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Output Active	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to Output High-Z		6		8		10	ns
t_{AOE}	$\overline{OE}$ LOW to Valid Data		5		7		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Output Active	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to Output High-Z		5		6		10	ns
t_{PU}	$\overline{CE}$ to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down		15		20		25	ns
Write Cycle[3]								
t_{WC}	Write Cycle Time	15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Valid to Write End	10		12		25		ns
t_{HA}	Address Hold to Write End	0		0		0		ns
t_{SA}	Address Set-up Time	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		12		15		ns
t_{SD}	Data Set-up to Write End	7		9		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z Output		7		8		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Output Active	3		3		3		ns

Notes:

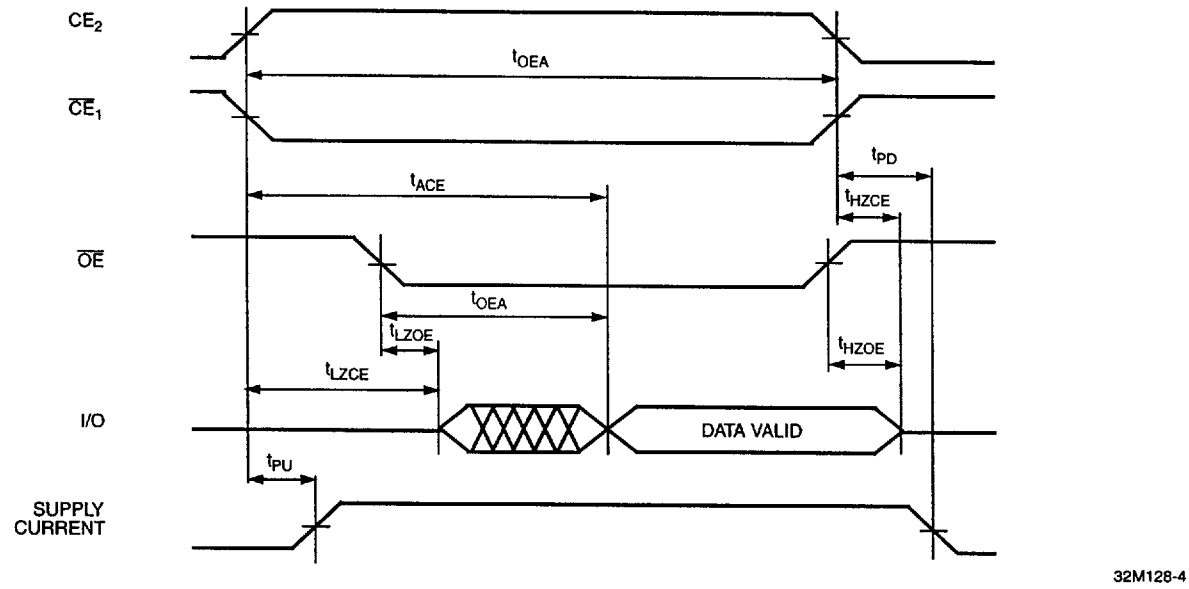
5. Active output to High-Z and High-Z to output active tests specified for a 500mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
6. Guaranteed, but not tested.

Switching Waveforms

Read Cycle No. 1 ($\overline{WE}$ and CE_2 are HIGH, $\overline{CE}_1$ and $\overline{OE}$ are LOW)[7]



Read Cycle No. 2 ($\overline{WE}$ is HIGH)[8]



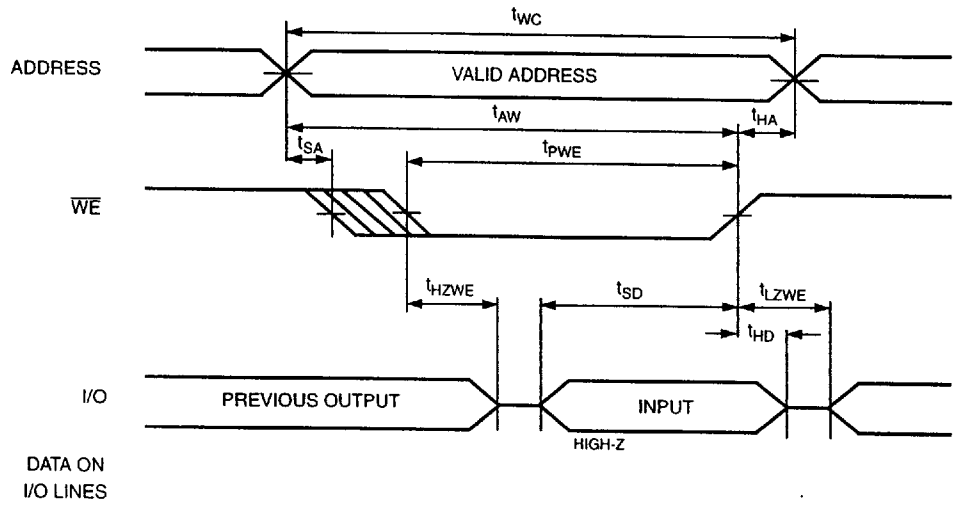
Notes:

7. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of hte I/O implies that data lines are in the Low-Z state and the data may not be valid until t_{AA}.

8. Timing illustrated for hte case when addresses are valid before $\overline{CE}_1$ and CE_2 are both asserted. I/O is not specified until t_{ACE} or t_{AOE}, but may become valid as soon as t_{HZCE} or t_{LZOE}. Output will transition from High-Z to valid data out. Valid data will be present following t_{AOE}, only if t_{ACE} timing is met.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ controlled) [9, 10]



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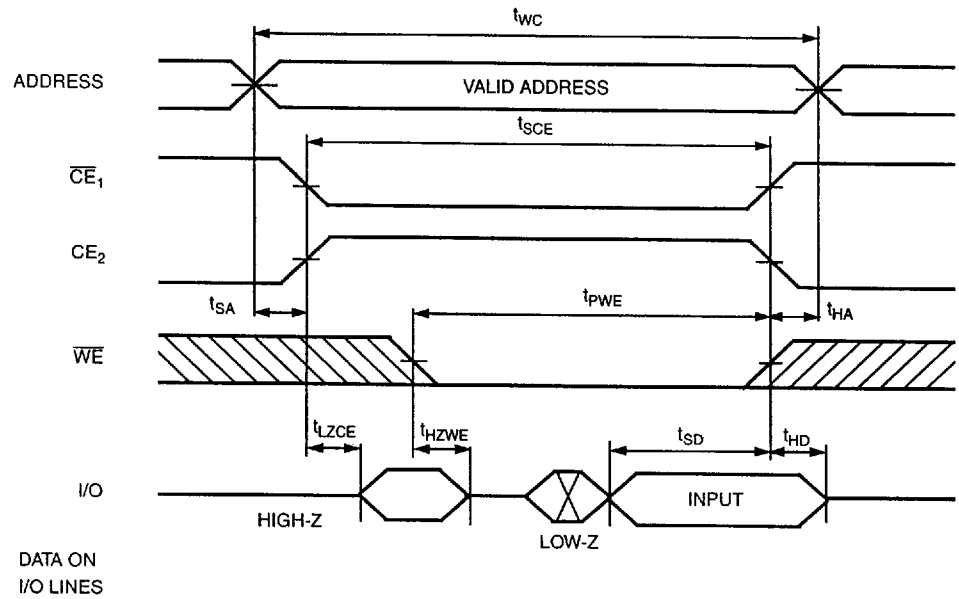
Write Cycle No.2 ($\overline{CE}$ controlled) [9, 11]



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Notes:

9. Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{WE}$ is LOW when both $\overline{CE}_1$ and CE_2 are asserted. If $\overline{OE}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{OE}$ asserted, it is recommended that $\overline{OE}$ be held HIGH for all write cycles. This will prevent outputs from becoming asserted, preventing bus contention, thereby reducing system noise.

10. Chip is selected; $\overline{CE}_1$ and $\overline{OE}$ are LOW, CE_2 is HIGH. Using only $\overline{WE}$ to control Write cycles may not offer the best device performance, since both t_{HZWE} and t_{SD} timing specifications must be met.

11. $\overline{OE}$ is LOW. I/O lines may transition to Low-Z if the falling edge of $\overline{WE}$ occurs after the falling edge of $\overline{CE}$.

Truth Table

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O	V_{CC}
Standby	X	H	X	High-Z	Standby
Read	H	L	L	Output	Active
Read	H	L	H	High-Z	Active
Write	L	L	X	Input	Active

Ordering Information

Speed	Part Number	Package Name	Package Type
15	AP32M128M-15	M64.1	64-Pin SIMM
20	AP32M128M-20	M64.1	64-Pin SIMM
25	AP32M128M-25	M64.1	64-Pin SIMM

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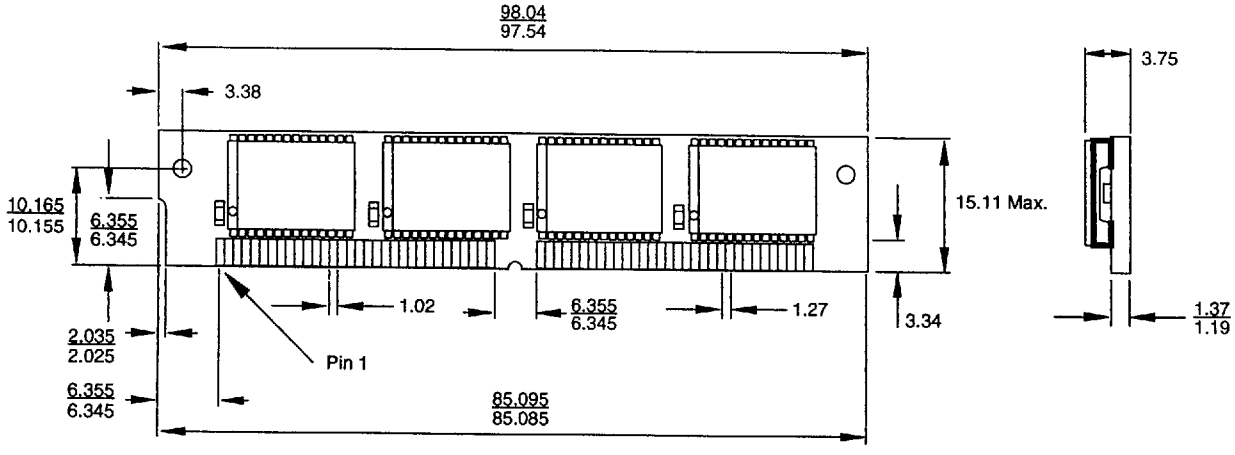
Package Diagram

M64.1 - 64-Pin Single In-Line Memory Module (SIMM) - Single Sided



Measurements are in Millimeters unless otherwise specified $\left(\frac{MAX}{MIN}\right)$ or typical if not noted.