PRELIMINARY

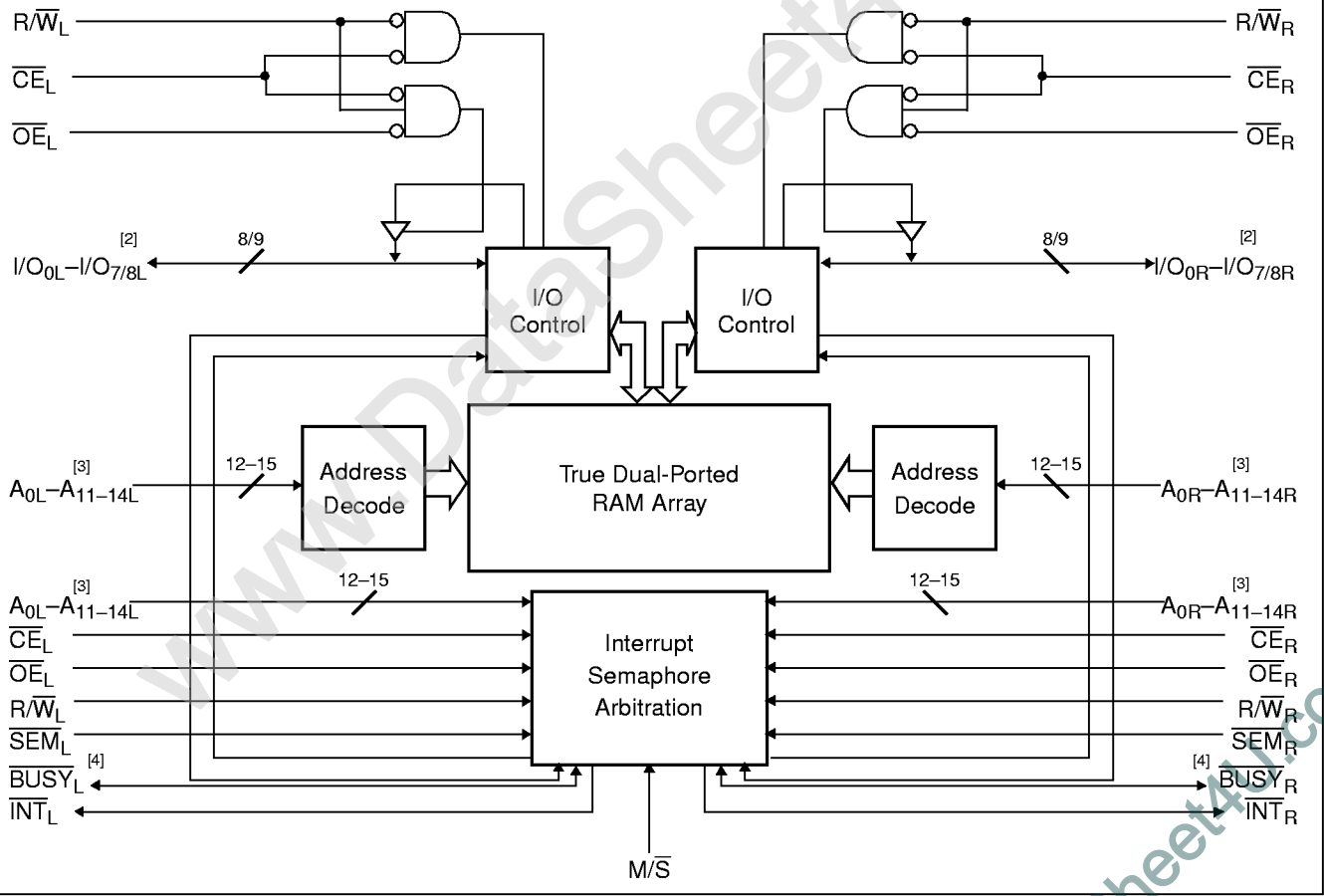
# CY7C138V/144V/006V/007V
# CY7C139V/145V/016V/017V

## 3.3V 4K/8K/16K/32K x 8/9 Dual-Port Static RAM

### Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- 4K/8K/16K/32K x 8 organizations (CY7C0138V/144V/006V/007V)
- 4K/8K/16K/32K x 9 organizations (CY7C0139V/145V/016V/017V)
- 0.35-micron CMOS for optimum speed/power
- High-speed access: 15[1]/20/25 ns
- Low operating power
  - Active: $I_{CC}$ = 115 mA (typical)
  - Standby: $I_{SB3}$ = 10 µA (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 16/18 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flag for port-to-port communication
- Pin select for Master or Slave
- Commercial and Industrial Temperature Ranges
- Available in 68-pin PLCC (all), 64-pin TQFP (7C006V & 7C144V)
- Pin-compatible and functionally equivalent to IDT70V05, 70V06, and 70V07.

### Logic Block Diagram




**Notes:**

1. Call for availability
2. $I/O_0$–$I/O_7$ for x8 devices; $I/O_0$–$I/O_8$ for x9 devices.
3. $A_0$–$A_{11}$ for 4K devices; $A_0$–$A_{12}$ for 8K devices; $A_0$–$A_{13}$ for 16K devices; $A_0$–$A_{14}$ for 32K devices.
4. $\overline{BUSY}$ is an output in master mode and an input in slave mode.

## Functional Description

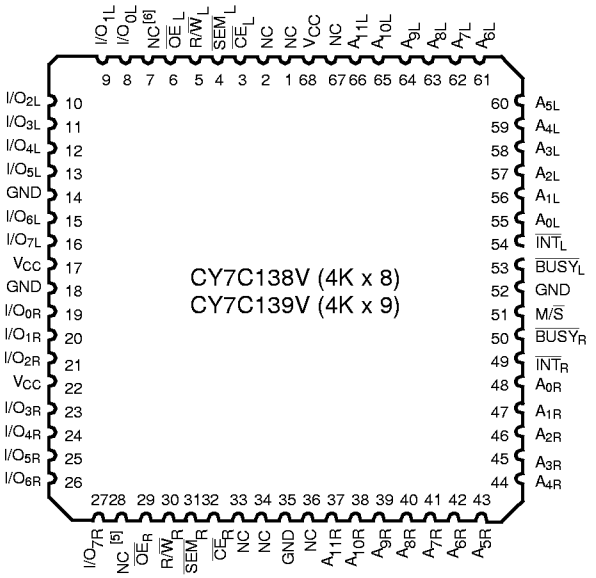
The CY7C138V/144V/006V/007V and CY7C139V/145V/016V/017V are low-power CMOS 4K, 8K, 16K, and 32K x8/9 dual-port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 8/9-bit dual-port static RAMs or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$), Read or Write Enable (R/$\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip select ($\overline{CE}$) pin.

.

## Pin Configurations

**68-Pin PLCC**
**Top View**

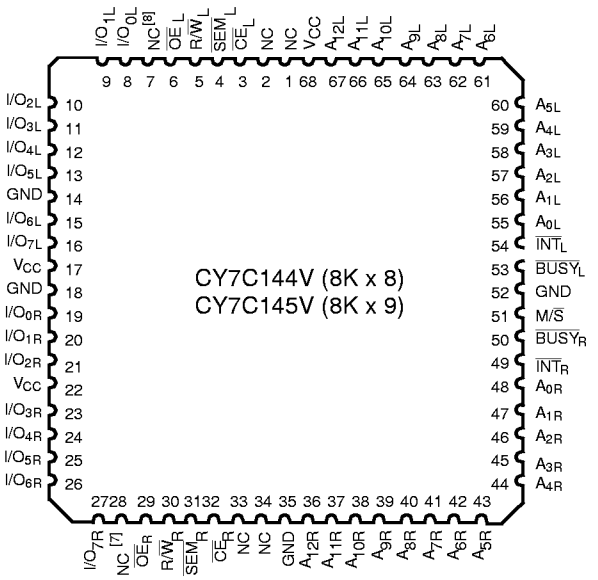



**Notes:**

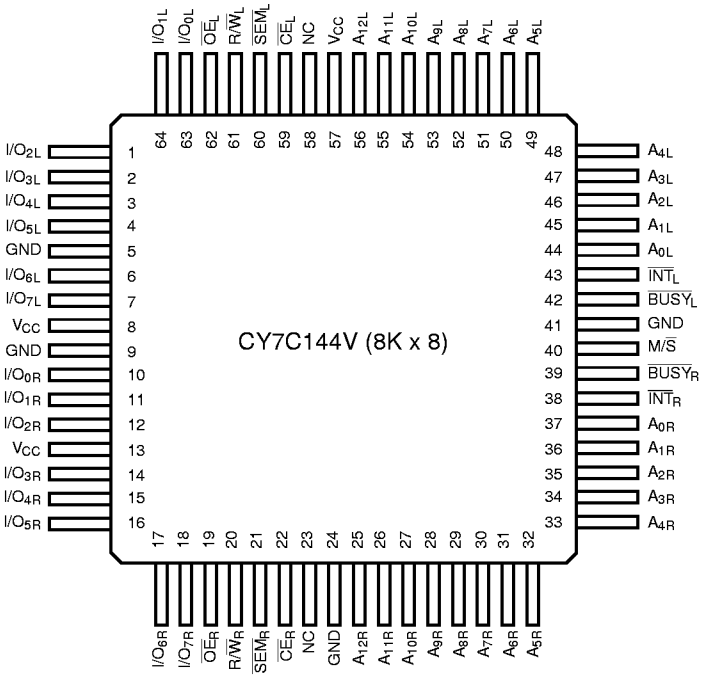
5. $I/O_{8R}$ on the CY7C139V.
6. $I/O_{8L}$ on the CY7C13V9.

## Pin Configurations (continued)

**68-Pin PLCC**
**Top View**



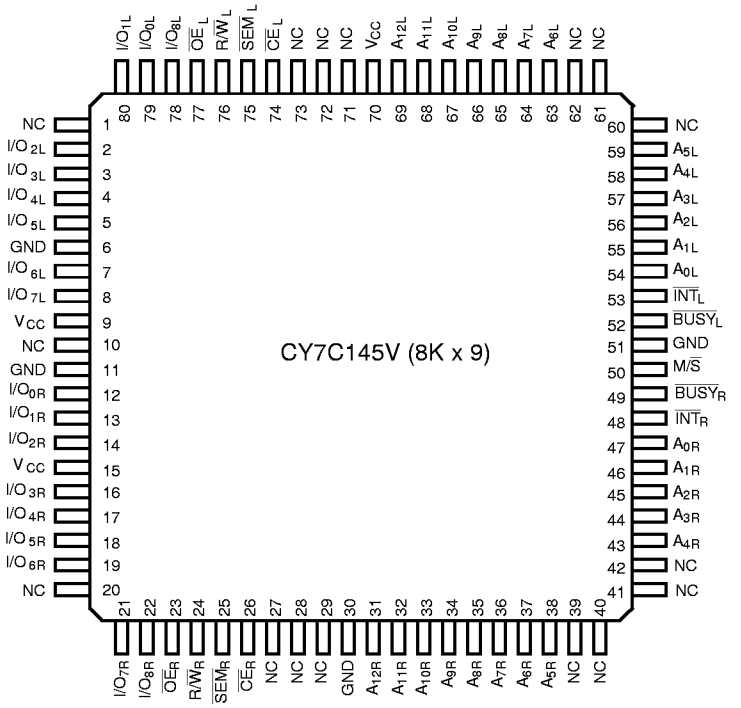

**64-Pin TQFP**
**Top View**



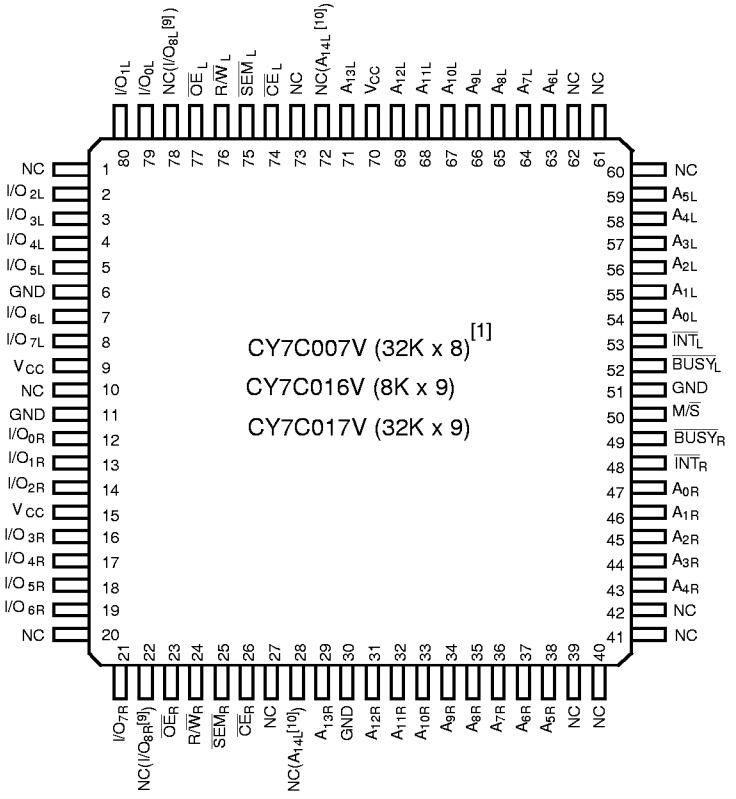

**Notes:**
7. $I/O_{8R}$ on the CY7C145V.
8. $I/O_{8L}$ on the CY7C145V.

## Pin Configurations (continued)

**80-Pin TQFP**
**Top View**



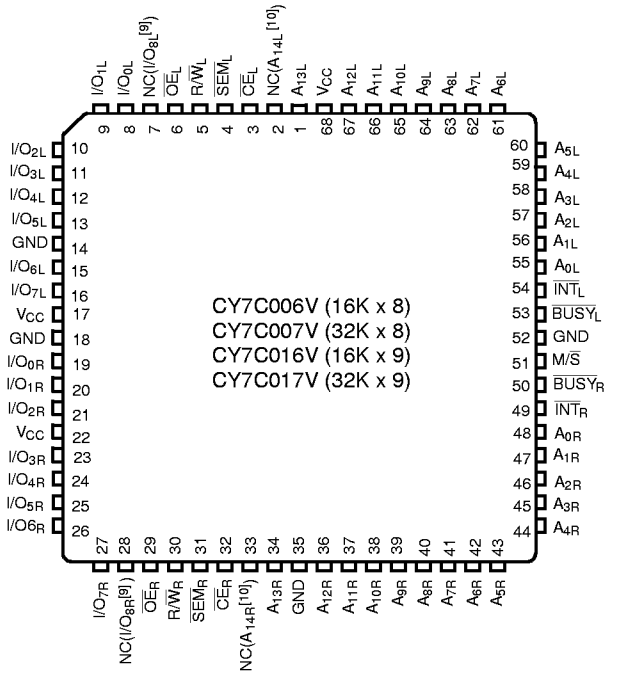

**80-Pin TQFP**
**Top View**



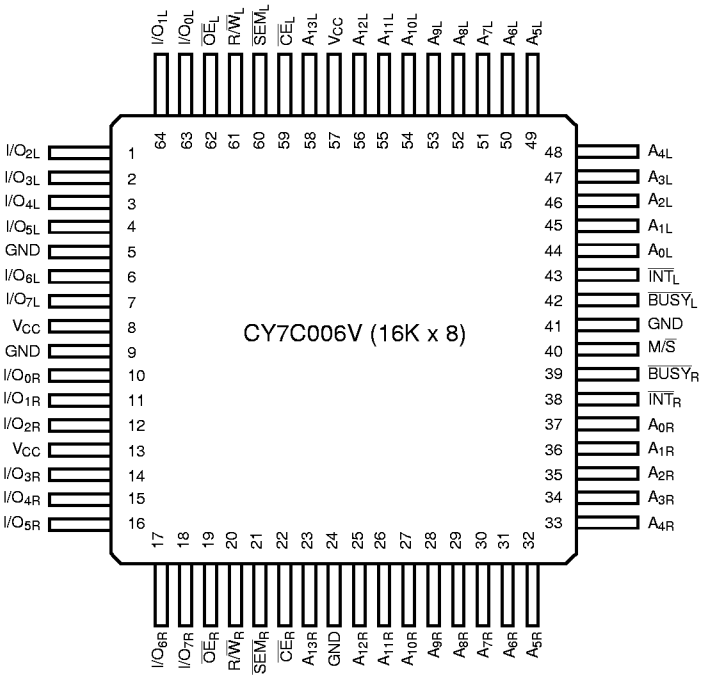

**Notes:**
9. I/O for CY7C016V and CY7C017V only.
10. Address line for CY7C007V and CY7C01V7 only.

## Pin Configurations (continued)

**68-Pin PLCC**
**Top View**




**64-Pin TQFP**
**Top View**



## Selection Guide

| | CY7C138V/144V/006V/007V CY7C139V/145V/016V/017V -15[1] | CY7C138V/144V/006V/007V CY7C139V/145V/016V/017V -20 | CY7C138V/144V/006V/007V CY7C139V/145V/016V/017V -25 |
|---|---|---|---|
| Maximum Access Time (ns) | 15 | 20 | 25 |
| Typical Operating Current (mA) | 125 | 120 | 115 |
| Typical Standby Current for $I_{SB1}$ (mA) (Both Ports TTL level) | 35 | 35 | 30 |
| Typical Standby Current for $I_{SB3}$ (µA) (Both Ports CMOS level) | 10 µA | 10 µA | 10 µA |

Shaded areas contain advance information.

## Pin Definitions

| Left Port | Right Port | Description |
|---|---|---|
| $\overline{CE}_L$ | $\overline{CE}_R$ | Chip Enable |
| R/$\overline{W}_L$ | R/$\overline{W}_R$ | Read/Write Enable |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable |
| $A_{0L}$–$A_{14L}$ | $A_{0R}$–$A_{14R}$ | Address ($A_0$–$A_{11}$ for 4K devices; $A_0$–$A_{12}$ for 8K devices; $A_0$–$A_{13}$ for 16K devices; $A_0$–$A_{14}$ for 32K) |
| $I/O_{0L}$–$I/O_{8L}$ | $I/O_{0R}$–$I/O_{8R}$ | Data Bus Input/Output ($I/O_0$–$I/O_7$ for x8 devices and $I/O_0$–$I/O_8$ for x9) |
| $\overline{SEM}_L$ | $\overline{SEM}_R$ | Semaphore Enable |
| $\overline{INT}_L$ | $\overline{INT}_R$ | Interrupt Flag |
| $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | Busy Flag |
| M/$\overline{S}$ | | Master or Slave Select |
| $V_{CC}$ | | Power |
| GND | | Ground |
| NC | | No Connect |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State .....–0.5V to $V_{CC}$+0.5V

DC Input Voltage[11].....–0.5V to $V_{CC}$+0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V

Latch-Up Current..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 300 mV |
| Industrial | –40°C to +85°C | 3.3V ± 300 mV |

Shaded areas contain advance information.

**Note:**
11. Pulse width < 20 ns.

## Electrical Characteristics Over the Operating Range

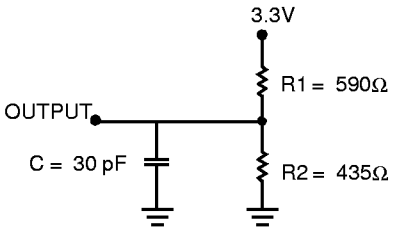
| Parameter | Description | | CY7C138V/144V/006V/007V CY7C139V/145V/016V/017V | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -15[1] | | | -20 | | | -25 | | | |
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{OH}$ | Output HIGH Voltage ($V_{CC}$ = 3.3V) | | 2.4 | | | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | | | | 0.4 | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | | | 0.8 | | | 0.8 | V |
| $I_{OZ}$ | Output Leakage Current | | –10 | | 10 | –10 | | 10 | –10 | | 10 | µA |
| $I_{CC}$ | Operating Current ($V_{CC}$ = Max., $I_{OUT}$ = 0 mA) Outputs Disabled | Com'l. | | 125 | 185 | | 120 | 175 | | 115 | 165 | mA |
| | | Indust. | | | | | 140 | 195 | | 135 | 185 | mA |
| $I_{SB1}$ | Standby Current (Both Ports TTL Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$ | Com'l. | | 35 | 50 | | 35 | 45 | | 30 | 40 | mA |
| | | Indust. | | | | | 45 | 55 | | 40 | 50 | mA |
| $I_{SB2}$ | Standby Current (One Port TTL Level) $\overline{CE}_L$ \| $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$ | Com'l. | | 80 | 120 | | 75 | 110 | | 65 | 95 | mA |
| | | Indust. | | | | | 85 | 130 | | 75 | 105 | mA |
| $I_{SB3}$ | Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$ – 0.2V, f = 0 | Com'l. | | 10 | 500 | | 10 | 500 | | 10 | 500 | µA |
| | | Indust. | | | | | 10 | 500 | | 10 | 500 | µA |
| $I_{SB4}$ | Standby Current (One Port CMOS Level) $\overline{CE}_L$ \| $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$[12] | Com'l. | | 75 | 105 | | 70 | 95 | | 60 | 80 | mA |
| | | Indust. | | | | | 80 | 105 | | 70 | 90 | mA |

Shaded areas contain advance information.

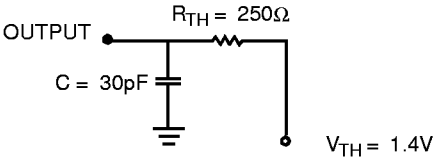
## Capacitance[13]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

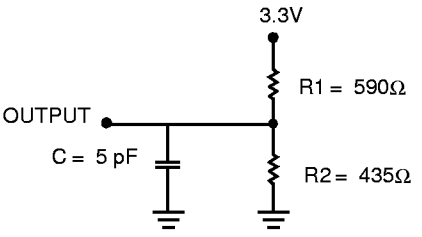
## AC Test Loads and Waveforms



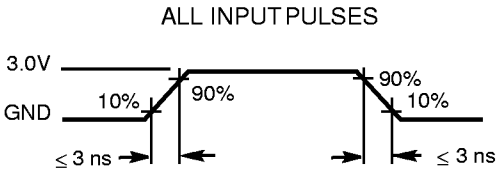

(a) Normal Load (Load 1)




(b) ThéveninEquivalent (Load 1)




(c) Three-State Delay (Load 2)
(Used for $t_{LZ}$, $t_{HZ}$, $t_{HZWE}$ & $t_{LZWE}$ including scope and jig)




**Notes:**

12. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby $I_{SB3}$.
13. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics Over the Operating Range[14]

| Parameter | Description | CY7C138V/144V/006V/007V CY7C139V/145V/016V/017V | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | –15[1] | | -20 | | -25 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 15 | | 20 | | 25 | | ns |
| $t_{AA}$ | Address to Data Valid | | 15 | | 20 | | 25 | ns |
| $t_{OHA}$ | Output Hold From Address Change | 3 | | 3 | | 3 | | ns |
| $t_{ACE}$[15] | $\overline{CE}$ LOW to Data Valid | | 15 | | 20 | | 25 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 10 | | 12 | | 13 | ns |
| $t_{LZOE}$[16, 17, 18] | $\overline{OE}$ Low to Low Z | 3 | | 3 | | 3 | | ns |
| $t_{HZOE}$[16, 17, 18] | $\overline{OE}$ HIGH to High Z | | 10 | | 12 | | 15 | ns |
| $t_{LZCE}$[16, 17, 18] | $\overline{CE}$ LOW to Low Z | 3 | | 3 | | 3 | | ns |
| $t_{HZCE}$[16, 17, 18] | $\overline{CE}$ HIGH to High Z | | 10 | | 12 | | 15 | ns |
| $t_{PU}$[18] | $\overline{CE}$ LOW to Power-Up | 0 | | 0 | | 0 | | ns |
| $t_{PD}$[18] | $\overline{CE}$ HIGH to Power-Down | | 15 | | 20 | | 25 | ns |
| $t_{ABE}$[15] | Byte Enable Access Time | | 15 | | 20 | | 25 | ns |
| **WRITE CYCLE** | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 15 | | 20 | | 25 | | ns |
| $t_{SCE}$[15] | $\overline{CE}$ LOW to Write End | 12 | | 16 | | 20 | | ns |
| $t_{AW}$ | Address Valid to Write End | 12 | | 16 | | 20 | | ns |
| $t_{HA}$ | Address Hold From Write End | 0 | | 0 | | 0 | | ns |
| $t_{SA}$[15] | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | Write Pulse Width | 12 | | 16 | | 20 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 10 | | 12 | | 15 | | ns |
| $t_{HD}$ | Data Hold From Write End | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$[17, 18] | R/$\overline{W}$ LOW to High Z | | 10 | | 12 | | 15 | ns |
| $t_{LZWE}$[17, 18] | R/$\overline{W}$ HIGH to Low Z | 3 | | 3 | | 3 | | ns |
| $t_{WDD}$[19] | Write Pulse to Data Delay | | 30 | | 40 | | 50 | ns |
| $t_{DDD}$[19] | Write Data Valid to Read Data Valid | | 25 | | 30 | | 35 | ns |
| **BUSY TIMING**[20] | | | | | | | | |
| $t_{BLA}$ | $\overline{BUSY}$ LOW from Address Match | | 15 | | 20 | | 20 | ns |
| $t_{BHA}$ | $\overline{BUSY}$ HIGH from Address Mismatch | | 15 | | 20 | | 20 | ns |
| $t_{BLC}$ | $\overline{BUSY}$ LOW from $\overline{CE}$ LOW | | 15 | | 20 | | 20 | ns |
| $t_{BHC}$ | $\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH | | 15 | | 16 | | 17 | ns |
| $t_{PS}$ | Port Set-Up for Priority | 5 | | 5 | | 5 | | ns |
| $t_{WB}$ | R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave) | 0 | | 0 | | 0 | | ns |
| $t_{WH}$ | R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave) | 13 | | 15 | | 17 | | ns |

**Note:**

14. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
15. To access RAM, $\overline{CE}$=L, $\overline{SEM}$=H. To access semaphore, $\overline{CE}$=H and $\overline{SEM}$=L. Either condition must be valid for the entire $t_{SCE}$ time.
16. At any given temperature and voltage condition for any given device, $t_{HZCE}$ is less than $t_{LZCE}$ and $t_{HZOE}$ is less than $t_{LZOE}$.
17. Test conditions used are Load 3.
18. This parameter is guaranteed but not tested.For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
19. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
20. Test conditions used are Load 2.

## Switching Characteristics Over the Operating Range[14] (continued)

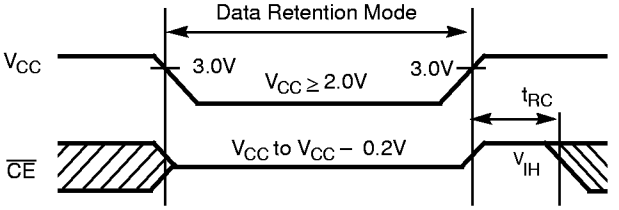
| Parameter | Description | CY7C138V/144V/006V/007V CY7C139V/145V/016V/017V | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | –15[1] | | -20 | | -25 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{BDD}$[21] | $\overline{BUSY}$ HIGH to Data Valid | | 15 | | 20 | | 25 | ns |
| **INTERRUPT TIMING**[20] | | | | | | | | |
| $t_{INS}$ | $\overline{INT}$ Set Time | | 15 | | 20 | | 20 | ns |
| $t_{INR}$ | $\overline{INT}$ Reset Time | | 15 | | 20 | | 20 | ns |
| **SEMAPHORE TIMING** | | | | | | | | |
| $t_{SOP}$ | SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$) | 10 | | 10 | | 12 | | ns |
| $t_{SWRD}$ | SEM Flag Write to Read Time | 5 | | 5 | | 5 | | ns |
| $t_{SPS}$ | SEM Flag Contention Window | 5 | | 5 | | 5 | | ns |
| $t_{SAA}$ | SEM Address Access Time | | 15 | | 20 | | 25 | ns |

## Data Retention Mode

The CY7C0138V/144V/006V/007V and CY7C139V/145V/016V/017V are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip enable ($\overline{CE}$) must be held HIGH during data retention, within $V_{CC}$ to $V_{CC}$ – 0.2V.
2. $\overline{CE}$ must be kept between $V_{CC}$ – 0.2V and 70% of $V_{CC}$ during the power-up and power-down transitions.
3. The RAM can begin operation >$t_{RC}$ after $V_{CC}$ reaches the minimum operating voltage (3.0 volts).

## Timing



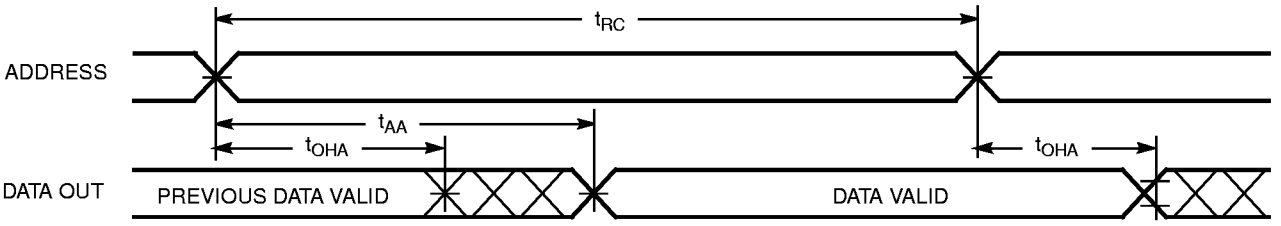

| Parameter | Test Conditions[22] | Max. | Unit |
|---|---|---|---|
| $ICC_{DR1}$ | @ $VCC_{DR}$ = 2V | 50 | µA |

**Notes:**

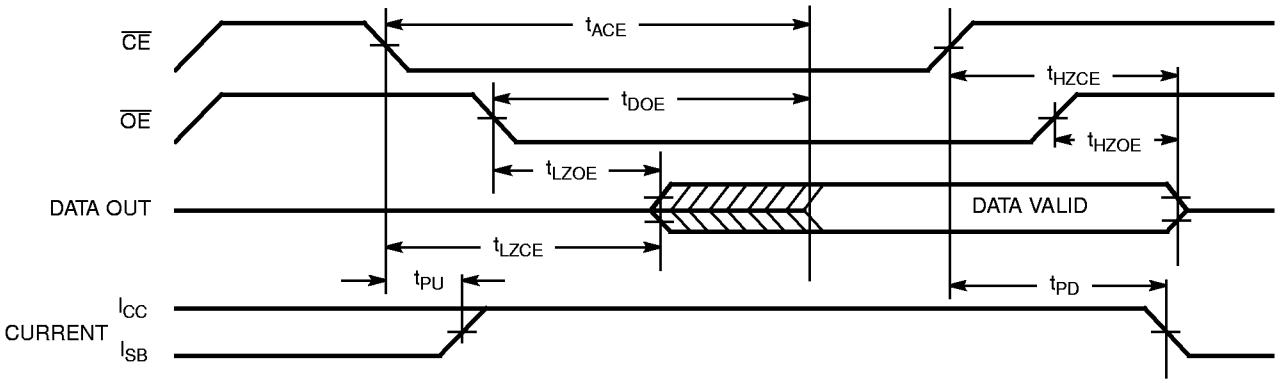
21. $t_{BDD}$ is a calculated parameter and is the greater of $t_{WDD}$–$t_{PWE}$ (actual) or $t_{DDD}$–$t_{SD}$ (actual).
22. $\overline{CE}$ = $V_{CC}$, $V_{in}$ = GND to $V_{CC}$, $T_A$ = 25°C. This parameter is guaranteed but not tested.

## Switching Waveforms

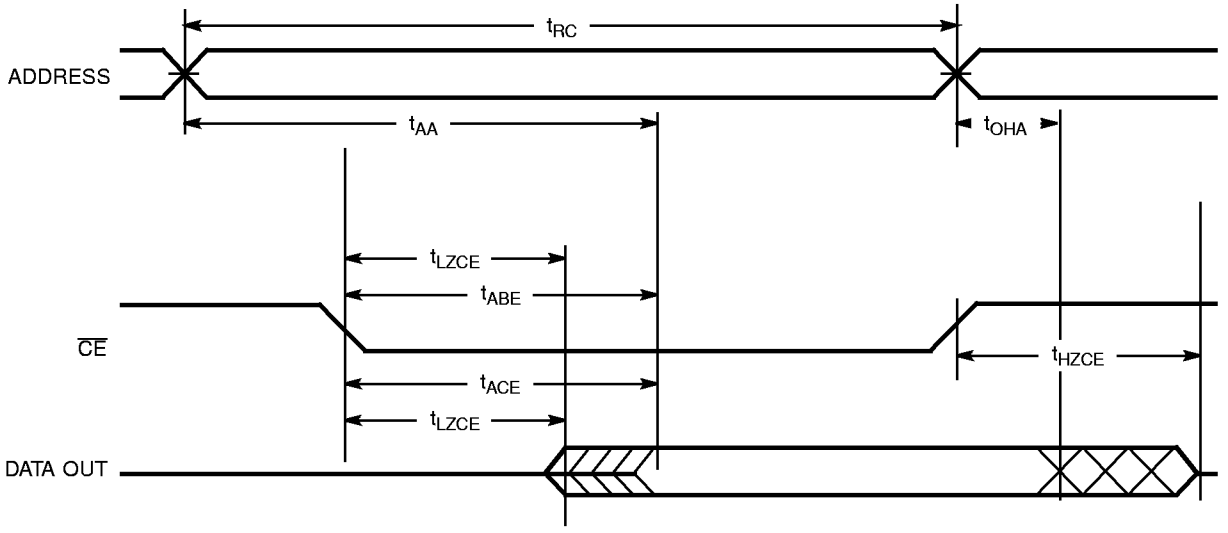
### Read Cycle No. 1 (Either Port Address Access)[23, 24, 25]




### Read Cycle No .2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[23, 26, 27]



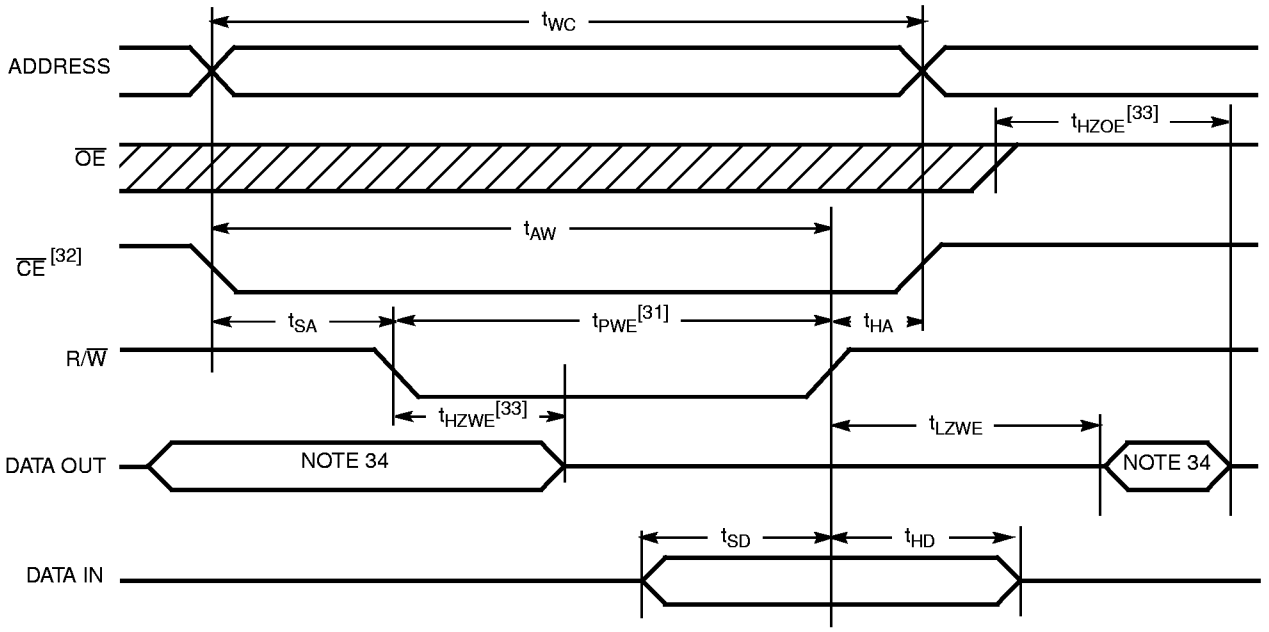

### Read Cycle No. 3 (Either Port)[23, 25, 26, 27]



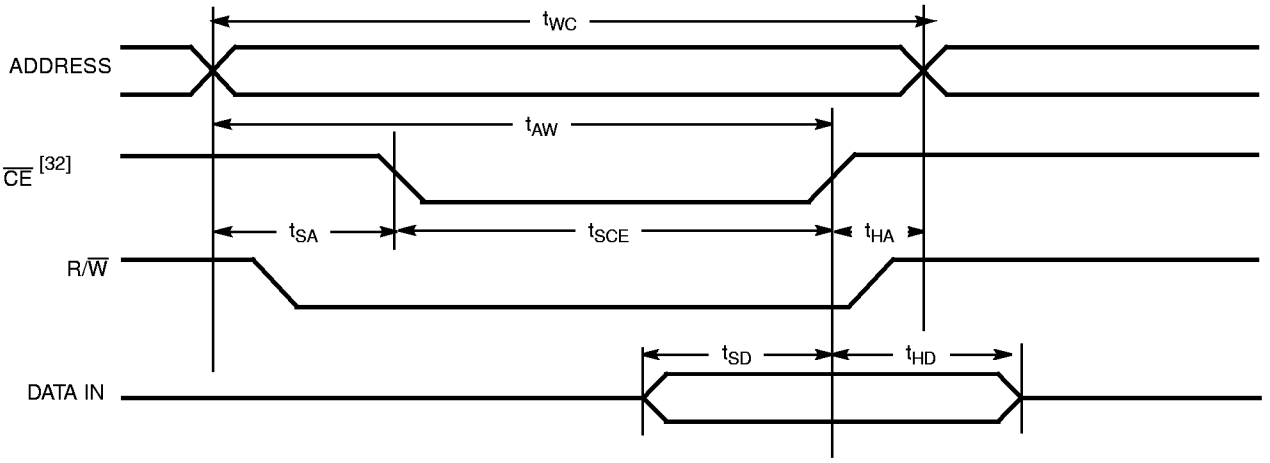

**Notes:**
23. R/$\overline{W}$ is HIGH for read cycles.
24. Device is continuously selected $\overline{CE} = V_{IL}$. This waveform cannot be used for semaphore reads.
25. $\overline{OE} = V_{IL}$.
26. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
27. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

## Switching Waveforms (continued)

### Write Cycle No. 1: R/$\overline{W}$ Controlled Timing[28, 29, 30, 31]




### Write Cycle No. 2: $\overline{CE}$ Controlled Timing[28, 29, 30, 35]

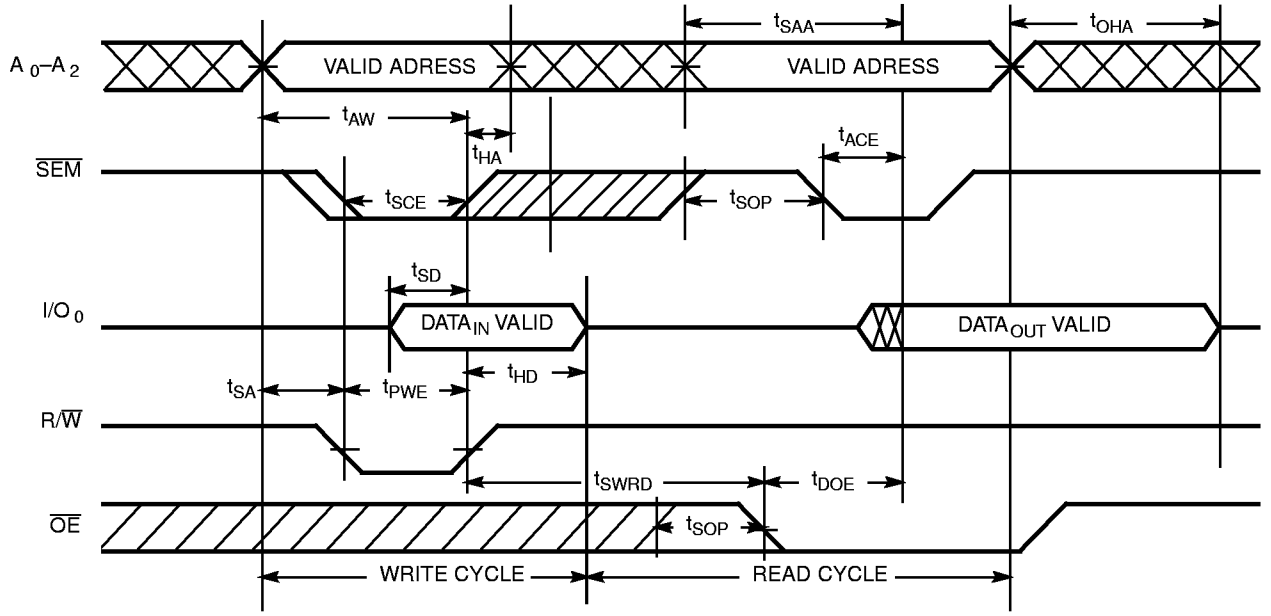



**Notes:**

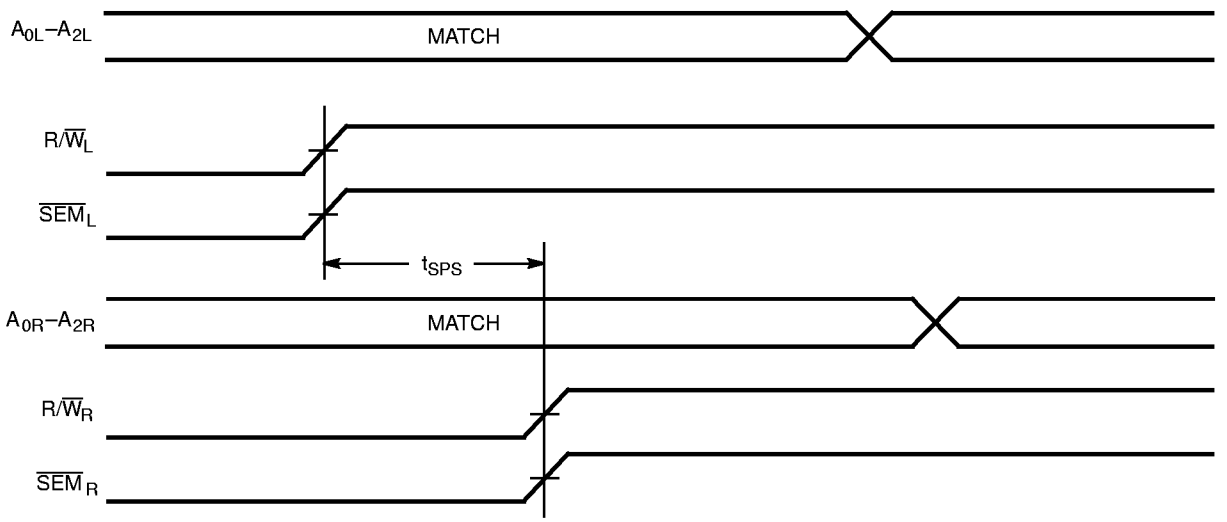
28. R/$\overline{W}$ must be HIGH during all address transitions.
29. A write occurs during the overlap ($t_{SCE}$ or $t_{PWE}$) of a LOW $\overline{CE}$ or $\overline{SEM}$.
30. $t_{HA}$ is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
31. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of $t_{PWE}$ or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{SD}$. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{PWE}$.
32. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$.
33. Transition is measured ±500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
34. During this period, the I/O pins are in the output state, and input signals must not be applied.
35. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

## Switching Waveforms (continued)

### Semaphore Read After Write Timing, Either Side[36]



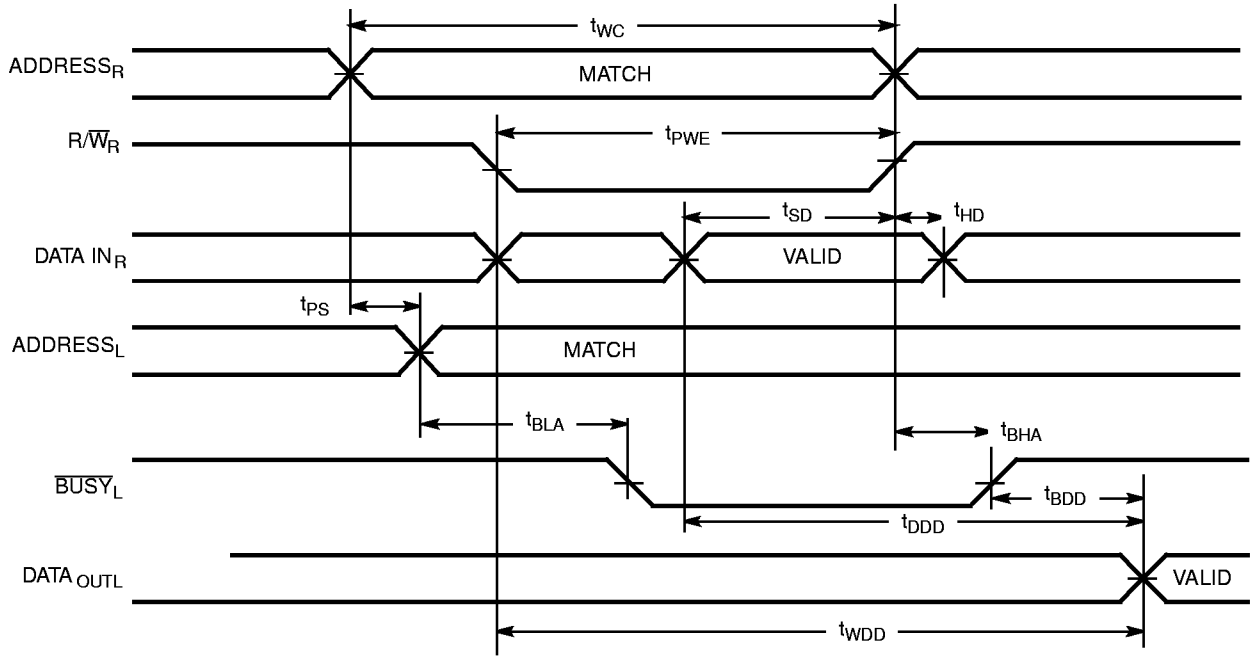

### Timing Diagram of Semaphore Contention[37, 38, 39]



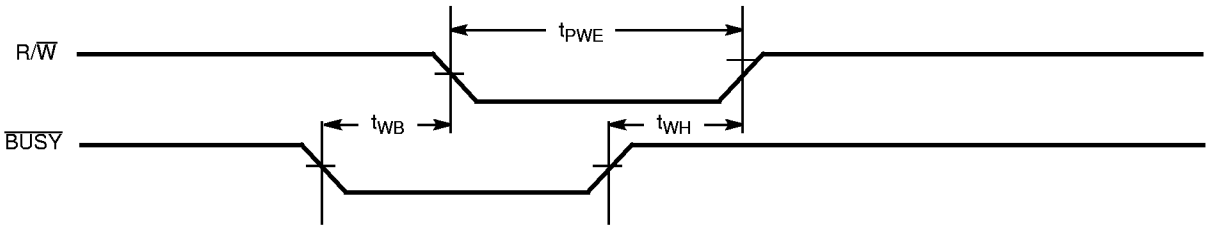

**Notes:**
36. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
37. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
38. Semaphores are reset (available to both ports) at cycle start.
39. If $t_{SPS}$ is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

## Switching Waveforms (continued)

### Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[40]



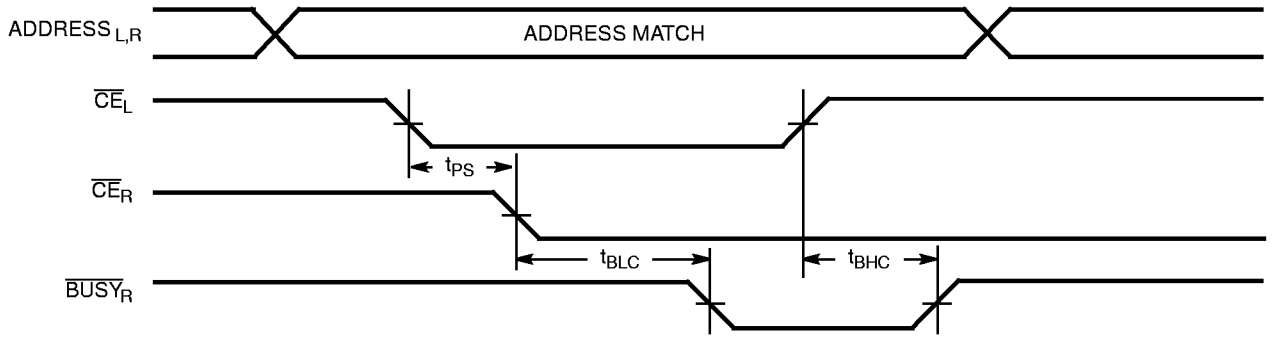

### Write Timing with Busy Input (M/$\overline{S}$=LOW)



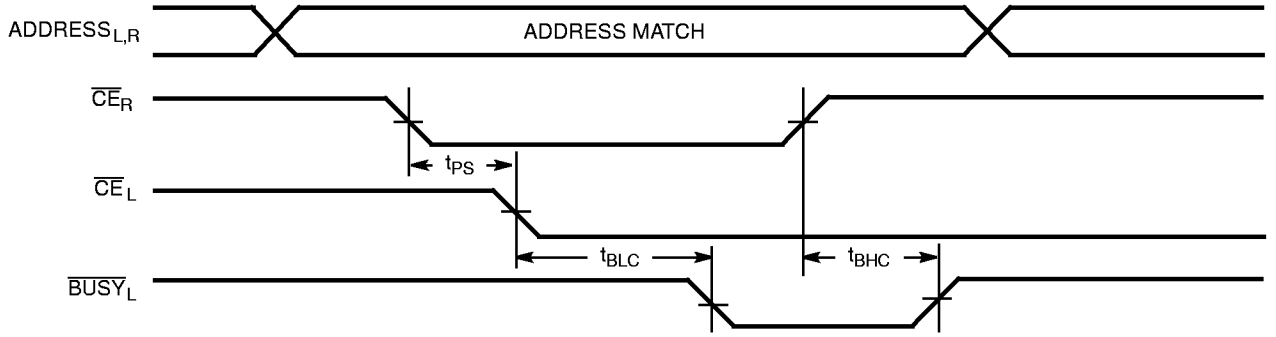

**Note:**
40. $\overline{CE}_L = \overline{CE}_R$ = LOW.

## Switching Waveforms (continued)

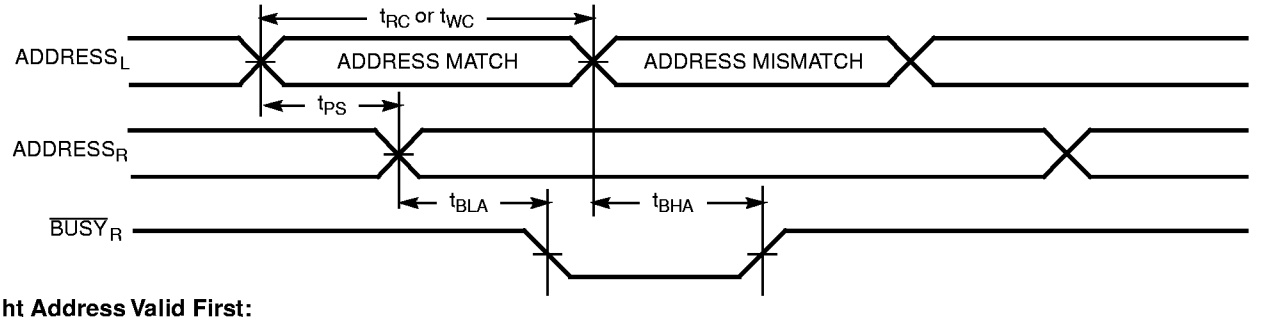
**Busy Timing Diagram No.1 ($\overline{CE}$ Arbitration)**[41]
**$\overline{CE}_L$ Valid First:**



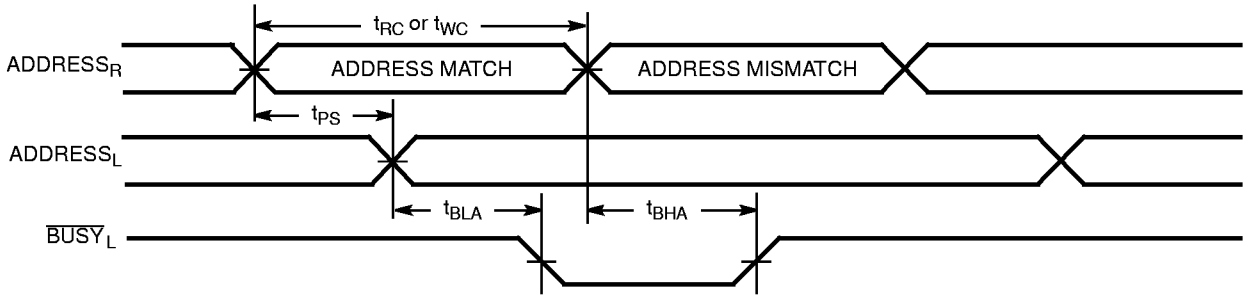

**$CE_R$ Valid First:**




**Busy Timing Diagram No.2 (Address Arbitration)**[41]
**Left Address Valid First**




**Right Address Valid First:**

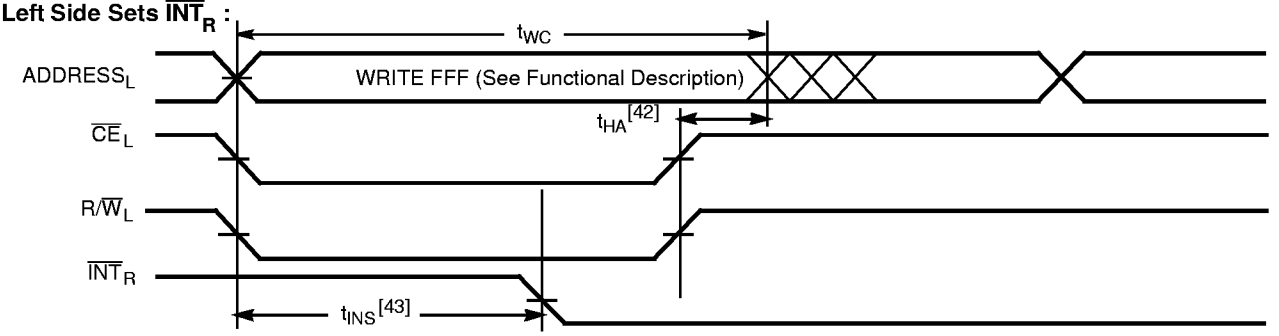



**Note:**
41. If $t_{PS}$ is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

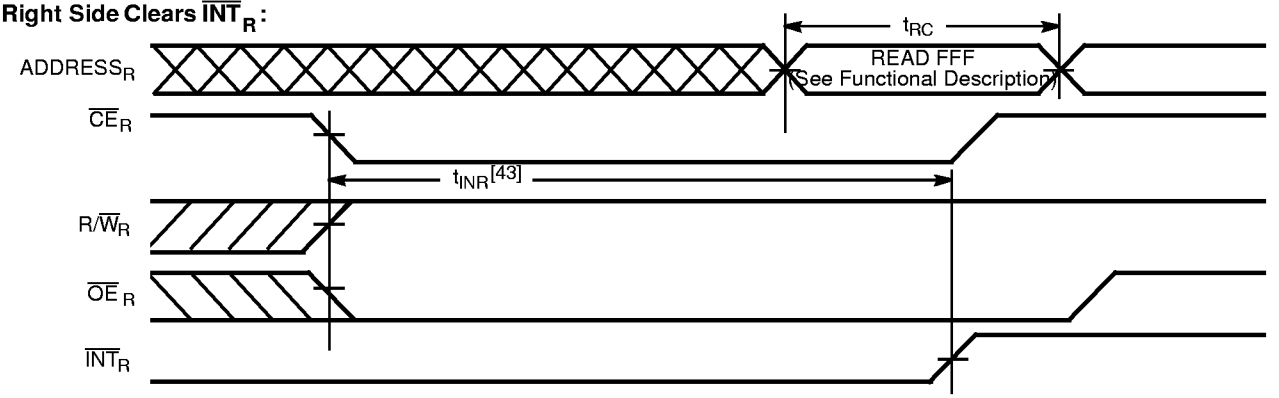
## Switching Waveforms (continued)

### Interrupt Timing Diagrams

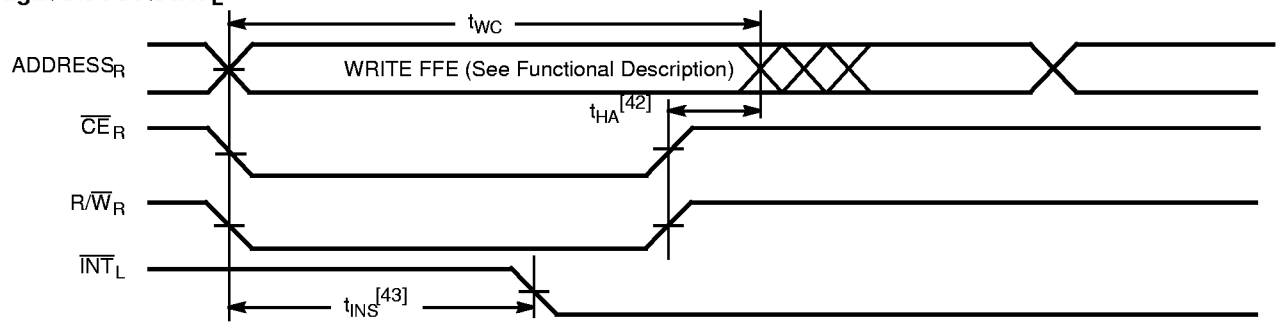
**Left Side Sets $\overline{INT}_R$ :**



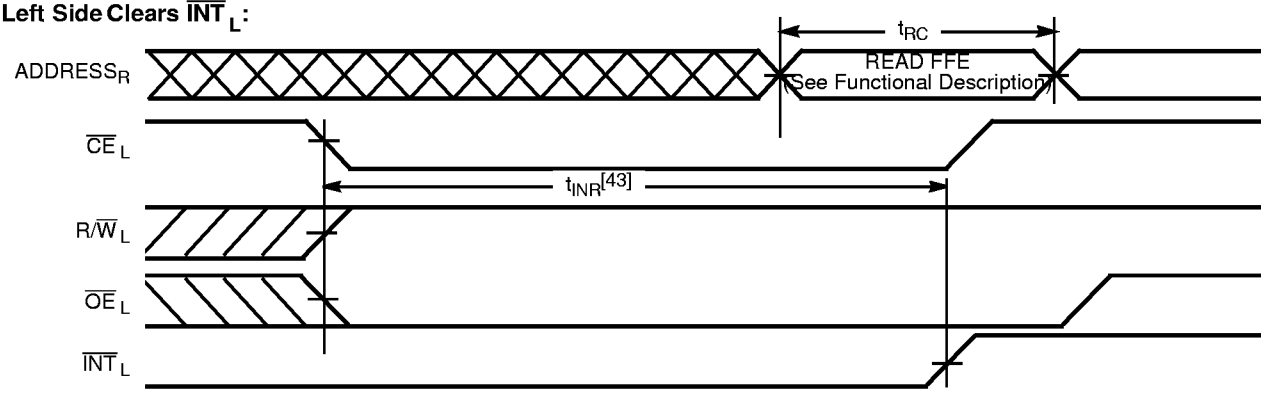

**Right Side Clears $\overline{INT}_R$ :**




**Right Side Sets $\overline{INT}_L$ :**




**Left Side Clears $\overline{INT}_L$ :**




**Notes:**

42. $t_{HA}$ depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
43. $t_{INS}$ or $t_{INR}$ depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

## Architecture

The CY7C138V/144V/006V/007V and CY7C139V/145V/016V/017V consist of an array of 4K, 8K, 16K, and 32K words of 8 and 9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two Interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two Semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the devices can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The devices also have an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

## Functional Description

### Write Operation

Data must be set up for a duration of $t_{SD}$ before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the R/$\overline{W}$ pin (see Write Cycle No. 1 waveform) or the $\overline{CE}$ pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port $t_{DDD}$ after the data is presented on the other port.

### Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available $t_{ACE}$ after $\overline{CE}$ or $t_{DOE}$ after $\overline{OE}$ is asserted. If the user wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

### Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CY7C138V/9V, 1FFF for the CY7C144V/5V, 3FFF for the CY7C006V/16V, 7FFF for the CY7C007V/17V) is the mailbox for the right port and the second-highest memory location (FFE for the CY7C138V/9V, 1FFE for the CY7C144V/5V, 3FFE for the CY7C006V/16V, 7FFE for the CY7C007V/17V) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user-defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it. If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin. The operation of the interrupts and their interaction with Busy are summarized in *Table 2.*

### Busy

The CY7C138V/144V/006V/007V and CY7139V/145V/016V/017V provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within $t_{PS}$ of each other, the busy logic will determine which port has access. If $t_{PS}$ is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. $\overline{BUSY}$ will be asserted $t_{BLA}$ after an address match or $t_{BLC}$ after $\overline{CE}$ is taken LOW.

### Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled ($t_{BLC}$ or $t_{BLA}$), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

### Semaphore Operation

The CY7C138V/144V/006V/007V and CY7C139V/145V/016V/017V provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for $t_{SOP}$ before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). $A_{0-2}$ represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only $I/O_0$ is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within $t_{SPS}$ of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

**Table 1. Non-Contending Read/Write**

| Inputs | | | | Outputs | Operation |
|---|---|---|---|---|---|
| $\overline{CE}$ | R/$\overline{W}$ | $\overline{OE}$ | $\overline{SEM}$ | $I/O_0$–$I/O_8$ | |
| H | X | X | H | High Z | Deselected: Power-Down |
| H | H | L | L | Data Out | Read Data in Semaphore Flag |
| X | X | H | X | High Z | I/O Lines Disabled |
| H | ⎍ | X | L | Data In | Write into Semaphore Flag |
| L | H | L | H | Data Out | Read |
| L | L | X | H | Data In | Write |
| L | X | X | L | | Not Allowed |

**Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)**

| | Left Port | | | | | Right Port | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | R/$\overline{W}_L$ | $\overline{CE}_L$ | $\overline{OE}_L$ | $A_{0L–14L}$ | $\overline{INT}_L$ | R/$\overline{W}_R$ | $\overline{CE}_R$ | $\overline{OE}_R$ | $A_{0R–14R}$ | $\overline{INT}_R$ |
| Set Right $\overline{INT}_R$ Flag | L | L | X | FFF[46] | X | X | X | X | X | L[45] |
| Reset Right $\overline{INT}_R$ Flag | X | X | X | X | X | X | L | L | FFF[46] | H[44] |
| Set Left $\overline{INT}_L$ Flag | X | X | X | X | L[44] | L | L | X | 1FFE[46] | X |
| Reset Left $\overline{INT}_L$ Flag | X | L | L | 1FFE[46] | H[45] | X | X | X | X | X |

**Table 3. Semaphore Operation Example**

| Function | $I/O_0$–$I/O_8$ Left | $I/O_0$–$I/O_8$ Right | Status |
|---|---|---|---|
| No action | 1 | 1 | Semaphore free |
| Left port writes 0 to semaphore | 0 | 1 | Left Port has semaphore token |
| Right port writes 0 to semaphore | 0 | 1 | No change. Right side has no write access to semaphore |
| Left port writes 1 to semaphore | 1 | 0 | Right port obtains semaphore token |
| Left port writes 0 to semaphore | 1 | 0 | No change. Left port has no write access to semaphore |
| Right port writes 1 to semaphore | 0 | 1 | Left port obtains semaphore token |
| Left port writes 1 to semaphore | 1 | 1 | Semaphore free |
| Right port writes 0 to semaphore | 1 | 0 | Right port has semaphore token |
| Right port writes 1 to semaphore | 1 | 1 | Semaphore free |
| Left port writes 0 to semaphore | 0 | 1 | Left port has semaphore token |
| Left port writes 1 to semaphore | 1 | 1 | Semaphore free |

**Note:**
44. If $\overline{BUSY}_R$ = L, then no change.
45. If $\overline{BUSY}_L$ = L, then no change.
46. See Functional Description for specific addresses by device part number.

## Ordering Information

### Package Availability Guide

| Device | Organization | 68-Pin PLCC | 64-Pin TQFP |
|---|---|---|---|
| CY7C138V | 4K x 8 | X | |
| CY7C139V | 4K x 9 | X | |
| CY7C144V | 8K x 8 | X | X |
| CY7C145V | 8K x 9 | X | |
| CY7C006V | 16K x 8 | X | X |
| CY7C016V | 16K x 9 | X | |
| CY7C007V | 32K x 8 | X | |
| CY7C017V | 32K x 9 | X | |

### 4K x8 3.3V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15[1] | CY7C138V-15JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| 20 | CY7C138V–20JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C138V–20JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |
| 25 | CY7C138V–25JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C138V–25JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |

Shaded areas contain advance information.

### 4K x9 3.3V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15[1] | CY7C139V-15JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| 20 | CY7C139V–20JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C139V–20JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |
| 25 | CY7C139V–25JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C139V–25JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |

Shaded areas contain advance information.

### 8K x8 3.3V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15[1] | CY7C144V-15AC | A65 | 64-Pin Thin Quad Flat Pack | Commercial |
| | CY7C144V-15JC | J81 | 68-Pin Plastic Leaded Chip Carrier | |
| 20 | CY7C144V–20AC | A65 | 64-Pin Thin Quad Flat Pack | Commercial |
| | CY7C144V–20JC | J81 | 68-Pin Plastic Leaded Chip Carrier | |
| | CY7C144V–20AI | A65 | 64-Pin Thin Quad Flat Pack | Industrial |
| | CY7C144V–20JI | J81 | 68-Pin Plastic Leaded Chip Carrier | |
| 25 | CY7C144V–25AC | A65 | 64-Pin Thin Quad Flat Pack | Commercial |
| | CY7C144V–25JC | J81 | 68-Pin Plastic Leaded Chip Carrier | |
| | CY7C144V–25AI | A65 | 64-Pin Thin Quad Flat Pack | Industrial |
| | CY7C144V–25JI | J81 | 68-Pin Plastic Leaded Chip Carrier | |

Shaded areas contain advance information.

## Ordering Information (continued)

### 8K x9 3.3V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15[1] | CY7C145V-15JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| 20 | CY7C145V–20JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C145V–20JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |
| 25 | CY7C145V–25JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C145V–25JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |

Shaded areas contain advance information.

### 16K x8 3.3V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15[1] | CY7C006V-15AC | A65 | 64-Pin Thin Quad Flat Pack | Commercial |
| | CY7C006V-15JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| 20 | CY7C006V–20AC | A65 | 64-Pin Thin Quad Flat Pack | Commercial |
| | CY7C006V–20JC | J81 | 68-Pin Plastic Leaded Chip Carrier | |
| | CY7C006V–20AI | A65 | 64-Pin Thin Quad Flat Pack | Industrial |
| | CY7C006V–20JI | J81 | 68-Pin Plastic Leaded Chip Carrier | |
| 25 | CY7C006V–25AC | A65 | 64-Pin Thin Quad Flat Pack | Commercial |
| | CY7C006V–25JC | J81 | 68-Pin Plastic Leaded Chip Carrier | |
| | CY7C006V–25AI | A65 | 64-Pin Thin Quad Flat Pack | Industrial |
| | CY7C006V–25JI | J81 | 68-Pin Plastic Leaded Chip Carrier | |

Shaded areas contain advance information.

### 16K x9 3.3V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15[1] | CY7C016V-15JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| 20 | CY7C016V–20JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C016V–20JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |
| 25 | CY7C016V–25JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C016V–25JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |

Shaded areas contain advance information.

### 32K x8 3.3V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15[1] | CY7C007V-15JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| 20 | CY7C007V–20JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C007V–20JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |
| 25 | CY7C007V–25JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C007V–25JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |

Shaded areas contain advance information.

## Ordering Information (continued)

**32K x9 3.3V Asynchronous Dual-Port SRAM**

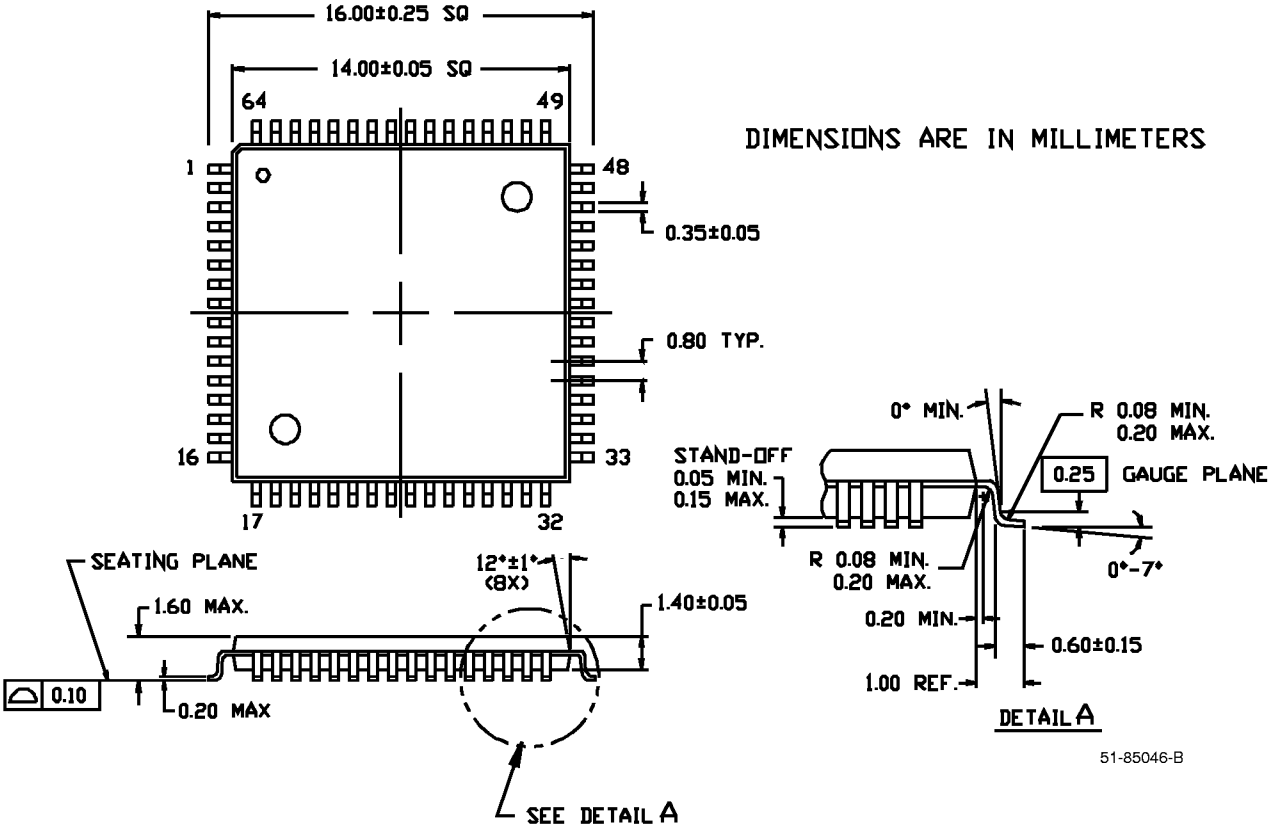
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15[1] | CY7C017V-15JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| 20 | CY7C017V–20JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C017V–20JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |
| 25 | CY7C017V–25JC | J81 | 68-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C017V–25JI | J81 | 68-Pin Plastic Leaded Chip Carrier | Industrial |

Shaded areas contain advance information.

Document #: 38–00677–B

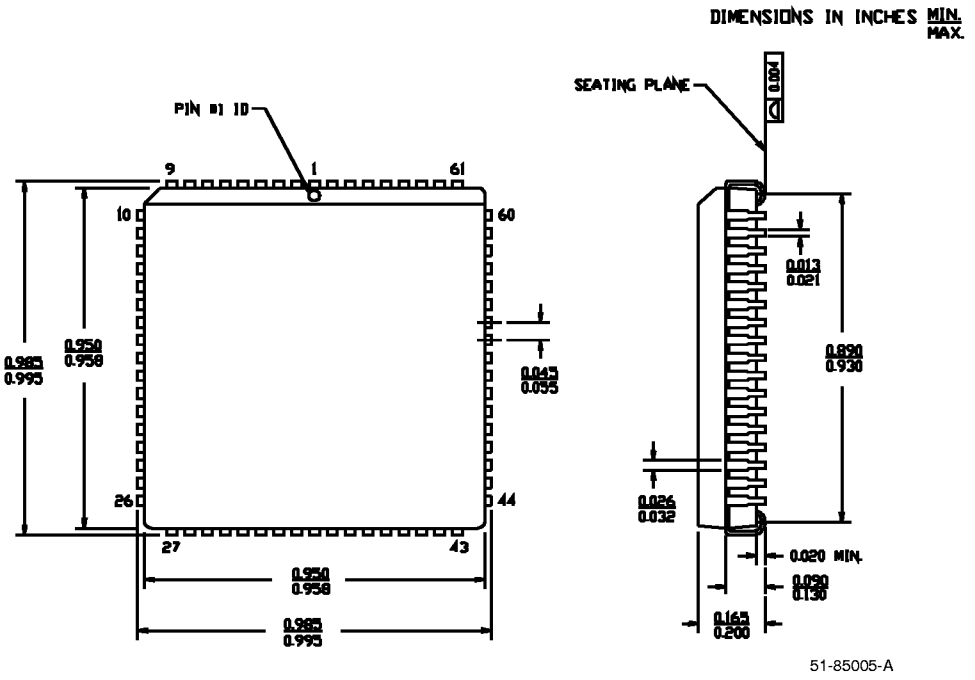
## Package Diagrams

**64-Lead Thin Plastic Quad Flat Pack (14 x 14 x 1.4 mm) A65**



## Package Diagrams (continued)

**68-Lead Plastic Leaded Chip Carrier J81**




51-85005-A

## CY7C036 Dual Port Design Consideration – Data Sheet Addendum

This design consideration applies to the Internal Power-On-Reset (POR) circuit used on the CY7C036 and its derivatives listed below.

Power supply ramp—The devices will function properly and meet all data sheet specifications if the power supply ramp rate is greater than 100 ns. If ramp is less than 100 ns, you may see a non-destructive failure in which the device will not respond to changes in address or clock, but the I/Os will respond to the output enable.

Applications consideration—If the power supply ramps in less than 100 ns, a small resistor (20–50Ω), a large capacitor, or an RC network can be connected at the output of the power supply to ground. The addition of a resistor will help clean up the power lines, while the capacitor will slow down the ramp rate without the loss of any power. Contact your local Cypress FAE for assistance as needed.

Troubleshooting—If a problem occurs with the part, power down the device to ground and then power up again at slower ramp rate (greater than 100 ns) in order to confirm that the problem might be due to the POR circuit. If the dual-port functions properly once the ramp rate is slowed to 100 ns or greater, then the POR circuit is at fault.

Applicable devices—All speed/package/temperature combinations of the following:

- CY7C138V
- CY7C139V
- CY7C144V
- CY7C145V
- CY7C006V
- CY7C016V
- CY7C007V
- CY7C017V

Cypress design change—Cypress design team has identified the root cause. A permanent circuit change and die revision will be available beginning in October and will be identified by the letter “A” in the part number.