# POLYFET RF DEVICES

F1202

7.39.09

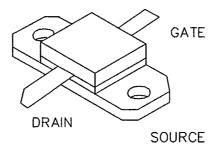
## **General Description**

Silicon vertical DMOS designed specifically for RF applications. Immune to forward and reverse bias secondary breakdown. "POLYFET" process features gold metal for greatly extended lifetime. Low output capacitance and high  $F_t$  enhance broad band performance.



20 WATTS TO 500 MHZ

Single Ended Package Style AP



# ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C)

Total Device Dissipation	Junction to Case Thermal Resistance	Maximum Junction Temperature	Storage Temperature	DC Drain Current	Drain to Gate Voltage	Drain to Source Voltage	Gate to Source Voltage
80 Watts	2.10 °C/W	200 °C	-65 °C to 150 °C	4 A	45 V	45 V	40 V

### RF CHARACTERISTICS (20 WATTS OUTPUT)

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
G <sub>ps</sub>	Common Source Power Gain	10			dВ	$I_{DQ} = 0.8A, V_{DS} = 12.5V, F = 500 MHz$
η	Drain Efficiency		60		%	I <sub>DQ</sub> =0.8A, V <sub>DS</sub> = 12.5V, F = 500 MHz
VSWR	Load Mismatch Tolerance			20 : 1	Relative	I <sub>DQ</sub> =0.8A, V <sub>DS</sub> = 12.5V, F = 500 MHz

#### **ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS ,	CONDITIONS
BV <sub>DSS</sub>	Drain Breakdown Voltage	40			v	I <sub>D</sub> = 0.1A, V <sub>GS</sub> = 0V
loss	Zero Bias Drain Current			2	mA	V <sub>DS</sub> = 12.5V, V <sub>GS</sub> = 0V
l <sub>GSS</sub>	Gate Leakage Current			1	uA	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 40V
V <sub>GS</sub>	Gate Bias for Drain Current	1		7	V	$I_D = 0.2A$ , $V_{GS} = V_{DS}$
8M	Forward Transconductance		1.6		МНО	V <sub>DS</sub> = 12.5V, I <sub>D</sub> =2.0A F=120 Htz
C <sub>iss</sub>	Common Source Input Capacitance		80		pFD	V <sub>DS</sub> = 12.5V, V <sub>GS</sub> = 0V, F = 1 MHz
C <sub>res</sub>	Common Source Feedback Capacitance		12		pFD	V <sub>DS</sub> = 12.5V, V <sub>GS</sub> = 0V, F = 1 MHz
Coss	Common Source Output Capacitance	t:	60		pFD	$V_{DS} = 12.5V$ , $V_{GS} = 0V$ , $F = 1$ MHz

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