MICRONAS

May 1992

T-51-09-12

MAS 1A212

PRELIMINARY

Dual 12-bit Voltage-out DAC

FEATURES

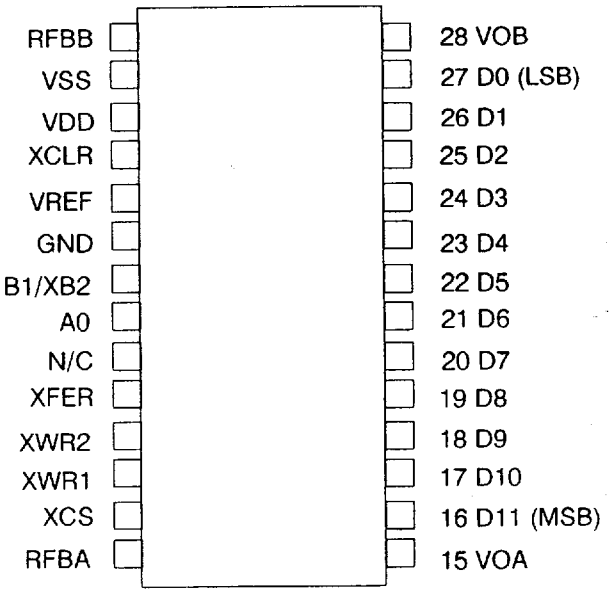
- Two 12-bit DAC's on a Single Monolithic Chip
- Bipolar Voltage Out
- Low Power (600 mW max.)
- Double-Buffered Inputs

GENERAL DESCRIPTION

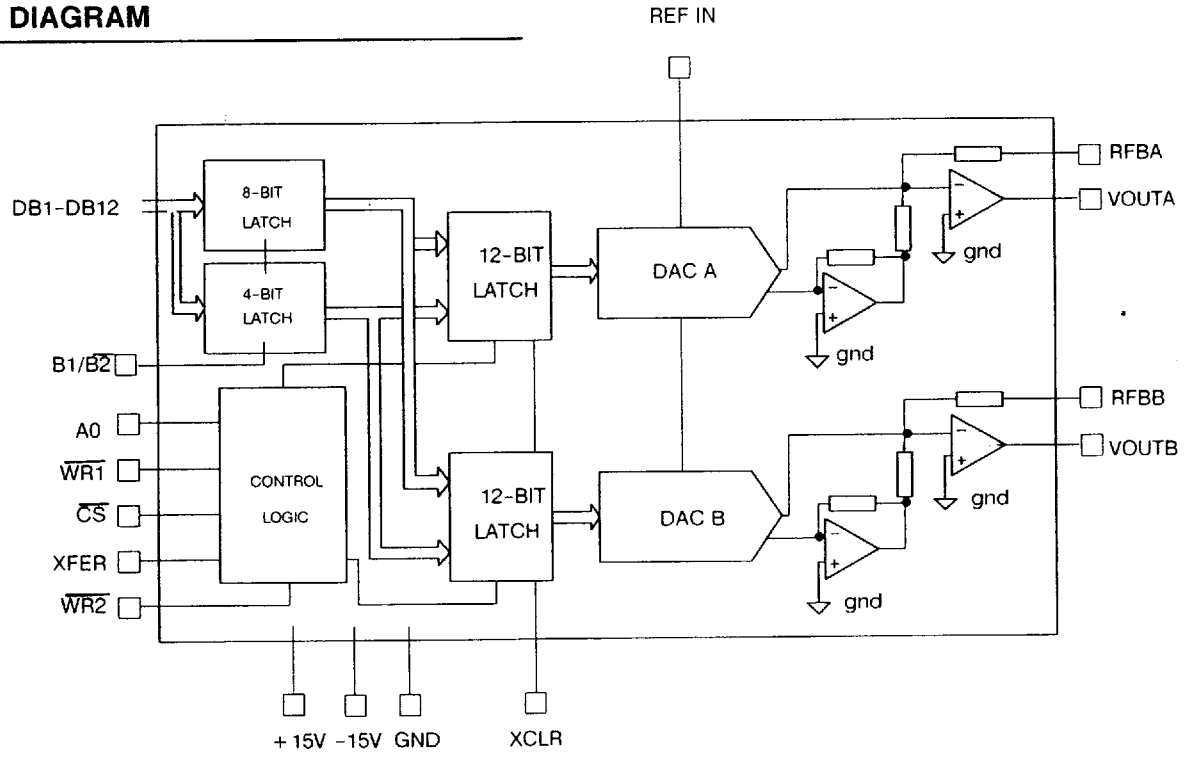
The MAS 1A212 is a dual 12-bit digital-to-analog converter with a bipolar voltage outpurt on a single monolithic IC. The MAS 1A212 features a double buffered input structure for each DAC allowing easy microprocessor interface. Both DAC's may be simultaneously updated using a single XFER command and they can be cleared to bipolar zero by asserting the asynchronous XCLR input.

The device is offered in a 28 pin Side Brazed DIP package.

PIN CONFIGURATION



BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

VDD = +15V, VSS = -15V, VREF = -10V, GND = 0V

Parameter	Symbol	Version	MIN	Ta = +25°C TYP	MAX	Tmin-Tmax Limits	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution	N	All	12			12	Bits	
Integral Nonlinearity	INL	All		+/-1/2	+/-1		LSB	Note 1. Relative Accuracy 11 bit
Differential Nonlinearity	DNL	All		+/-1/2	+/-1		LSB	Note 2. Monotonic to 12 bits
Gain error	GFE	All		+/-4	+/-8		LSB	Measured Using Internal Rfb's
Bipolar offset	BOF	All		+/-20	+/-40		mV	Digital inputs 100000000000
TEMPERATURE STABILITY								
Gain error TC	TCGFE	All		+/-15			ppm/°C	
Bipolar zero TC	TCBOF	All		+/-15			ppm/°C	
INL TC	TCINL	All		+/-1			ppm/°C	
DNL TC	TCDNL	All		+/-1			ppm/°C	
REFERENCE INPUT								
Input Resistance	Rref	All	2.5	5.0	7.5		kΩ	Input resistance per DAC 10kΩ typ.
DIGITAL INPUTS								
Input High Voltage	VIH	All	2.4		VDD	2.4	V	
Input Low Voltage	VIL	All	-0.3		0.8	0.8	V	
Input Current	Iin	All			+/-1	+/-10	µA	Note 4.
Input Capacitance	Cin	All			7	7	pF	Note 3.
SWITCHING CHARACTERISTICS								
Write Pulse Width		All		120			ns	
Data Setup Time		All		125			ns	
Data Hold Time		All		TBD			ns	
POWER SUPPLY								
VDD Range	VDD	All	13.5	15	16.5		V	
VSS range	VDD	All	-13.5	-15	-16.5		V	
Supply Current	IDD	All		15	20.0		mA	All Dig. Inputs 0V or 5V to VDD
	ISS	All		15	20.0		mA	All Dig. Inputs 0V or 5V to VDD
TEMPERATURE RANGE		C	0		+70		°C	
		I	-25		+85		°C	

NOTES:
1. Integral Nonlinearity is measured as the arithemetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value of any given input combination.
2. Differential Nonlinearity DNL is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
3. Guaranteed by design but not production tested.
4. Logic inputs are MOS gates. Iin typical is less than 1 nA at 25°C.

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AC PERFORMANCE CHARACTERISTICS

These Characteristics are included for design guidiance only and are subject to sample testing only.
VDD = +15V, VSS = -15V, VREF = -10V, GND = AGND = 0V.

Parameter	Symbol	Version	Min	Ta = +25°C TYP	MAX	Tmin-Tmax Limits	Units	Test Conditions/Comments
SETTLING TIME Full Scale Transition	ts	All		10			us	
DIGITAL TO ANALOG GLITCH ENERGY	Q	All		TBD			nVs	VREF = 0V: DAC register alternatel loaded with all 0's and all 1's Iout load = 100 Ohm. Cext = 13 p
MULTIPLYING FEEDTHROUGH ERROR AT IO1	FT IO1	All		TBD			mVpp	VREF = 20Vpp: f = 10kHz sine wave DAC register loaded with all 0's
POWER SUPPLY REJECTION RATIO	PSRR	All		TBD			%/%	VDD = 14-16V

ORDERING INFORMATION

Bipolar Offset	Gain Error	TEMPERATURE RANGE AND PACKAGE	
		COMMERCIAL	INDUSTRIAL
Ta = 25°C	Ta = 25°C	0°C to +70°C	-25°C to +85°C
		Side Braze	Side Braze
+/-40 mV	+/-8 LSB	MAS1A212-1CD	MAS1A212-1ID

MAS 1A212 CONTROL INPUTS

A0	$\overline{CS}$	$\overline{WR1}$	B1/$\overline{B2}$	$\overline{WR2}$	$\overline{XFER}$	MAS 1A212 OPERATION DESCRIPTION
0	0	0	1	1	1	Address DAC A register and loads data (register only)
1	0	0	1	1	1	Address DAC B register and loads data (register only)
X	X	X	X	0	0	Transfer data from first registers to all DAC's
X	1	X	X	X	X	No updated information
X	X	1	X	X	X	No updated information

MAS 1A212 Truth table 12-bit parallel load

MAS 1A212 CONTROL INPUTS

A0	$\overline{CS}$	$\overline{WR1}$	B1/$\overline{B2}$	$\overline{WR2}$	$\overline{XFER}$	MAS 1A212 OPERATION DESCRIPTION
0	0	0	1	1	1	Address DAC A register and loads data (register only)
0	0	0	0	1	1	Address DAC A register and updates lower 4 bits
1	0	0	1	1	1	Address DAC B register and loads data (register only)
1	0	0	0	1	1	Address DAC B register and updates lower 4 bits
X	X	X	X	0	0	Transfer data from first registers to all DAC's
X	1	X	X	X	X	No updated information
X	X	1	X	X	X	No updated information

MAS 1A212 Truth table 8-bit parallel load

CONTROL FUNCTIONS

PIN	FUNCTION
A0	Address for DAC selection
$\overline{CS}$	Enables DAC input and A0 (along with $\overline{WR1}$) for writing (Active low)
$\overline{WR1}$	Enables A0 (along with $\overline{CS}$) active low, gated with $\overline{CS}$
B1/$\overline{B2}$	Selects high and low bytes. In 12-bit mode, B1/$\overline{B2}$ tied high; In 8-bit mode, a 12-bit word is loaded into first register when B1/$\overline{B2}$ is high, and a 4-bit word is updated to the lower bits when B1/$\overline{B2}$ is low
$\overline{WR2}$	Gated with $\overline{XFER}$, used to load all DAC's simultaneously (Active low)
$\overline{XFER}$	Gated with $\overline{WR2}$, used to load all DAC's simultaneously (Active low)
$\overline{CLR}$	All registers reset to bipolar zero (Active low)

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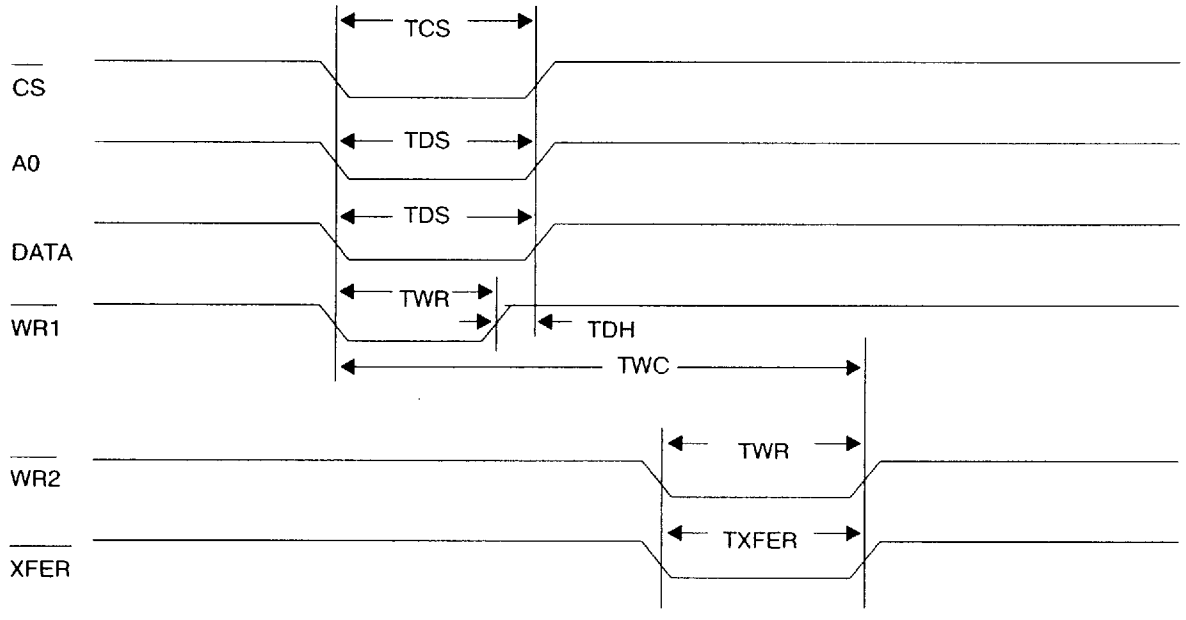
TIMING CHARACTERISTICS

PARAMETER	TYP AT TA = +25°C	LIMIT AT -25°C to +85°C	UNITS	
TDS	100 min	TBD	ns	Data set up time (to rising edge of $\overline{WR1}$ command)
TDH	0 min	TBD	ns	Data hold time
TWR	100 min	TBd	ns	Write pulse width
TCS	100 min	TBD	ns	Chip select width
TXFER	100 min	TBD	ns	Transfer pulse width
TWC	200 min	TBD	ns	Total write command

TIMING DIAGRAM



LEVEL TRIGGERED DEVICE

WRITE CYCLE TIMING DIAGRAM