

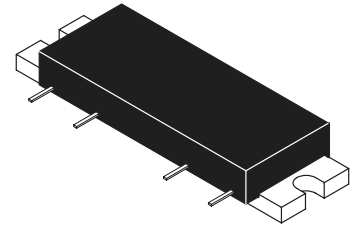
# The RF Line 3G Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the 3G frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital CDMA modulation systems.

- Third Order Intercept: 45 dBm Typ
- Power Gain: 31 dB Typ (@ f = 2140 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

**MHL21336**

**2110–2170 MHz  
3.0 W, 31 dB  
RF LINEAR LDMOS AMPLIFIER**



CASE 301AP-02, STYLE 1

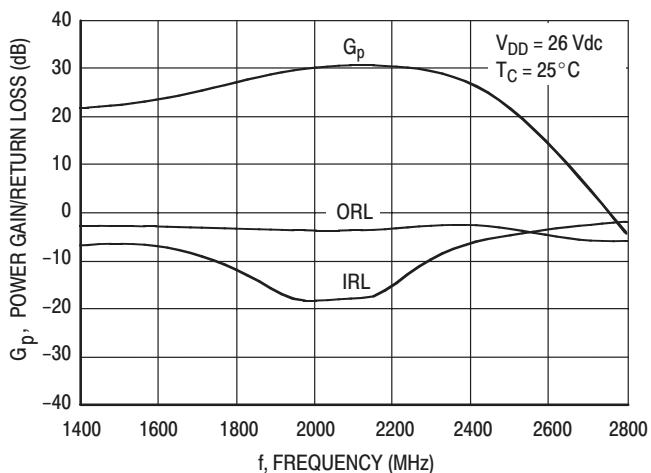
## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V <sub>DD</sub>	30	Vdc
RF Input Power	P <sub>in</sub>	+5	dBm
Storage Temperature Range	T <sub>stg</sub>	-40 to +100	°C
Operating Case Temperature Range	T <sub>C</sub>	-20 to +100	°C

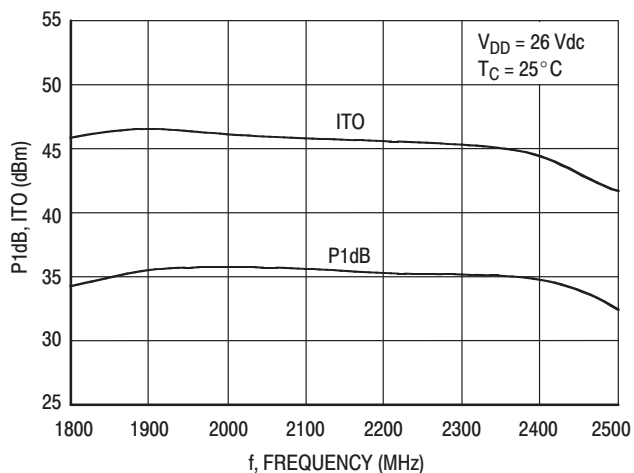
## ELECTRICAL CHARACTERISTICS (V<sub>DD</sub> = 26 Vdc, T<sub>C</sub> = 25°C; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I <sub>DD</sub>	—	500	525	mA
Power Gain (f = 2140 MHz)	G <sub>p</sub>	30	31	32	dB
Gain Flatness (f = 2110–2170 MHz)	G <sub>F</sub>	—	0.15	0.4	dB
Power Output @ 1 dB Comp. (f = 2140 MHz)	P <sub>out 1 dB</sub>	34	35	—	dBm
Input VSWR (f = 2110–2170 MHz)	VSWR <sub>in</sub>	—	1.2:1	1.5:1	
Third Order Intercept (f <sub>1</sub> = 2137 MHz, f <sub>2</sub> = 2142 MHz)	ITO	44	45	—	dBm
Noise Figure (f = 2170 MHz)	NF	—	4.5	5	dB

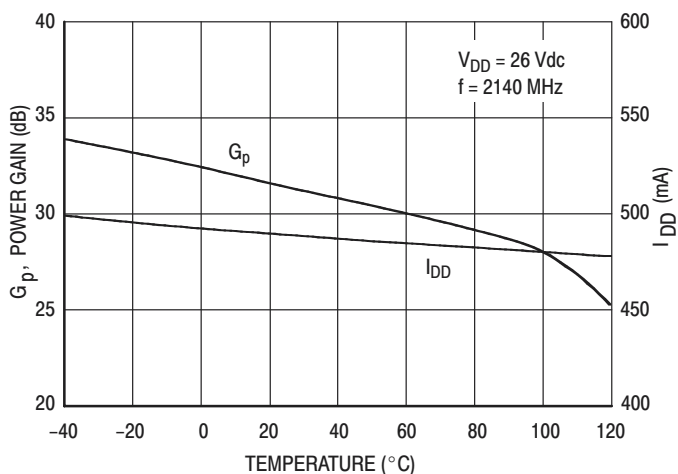
## TYPICAL CHARACTERISTICS



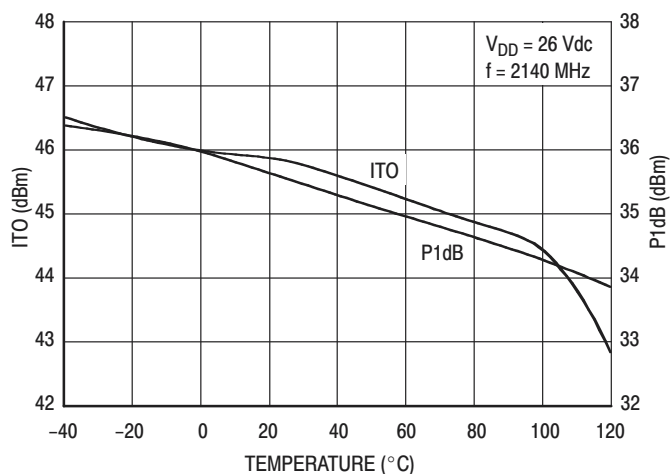
**Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency**



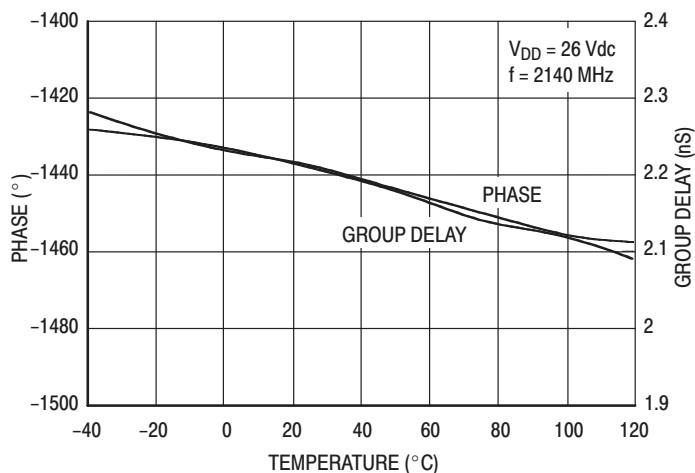
**Figure 2. P1dB, ITO versus Frequency**



**Figure 3. Power Gain,  $I_{DD}$  versus Temperature**

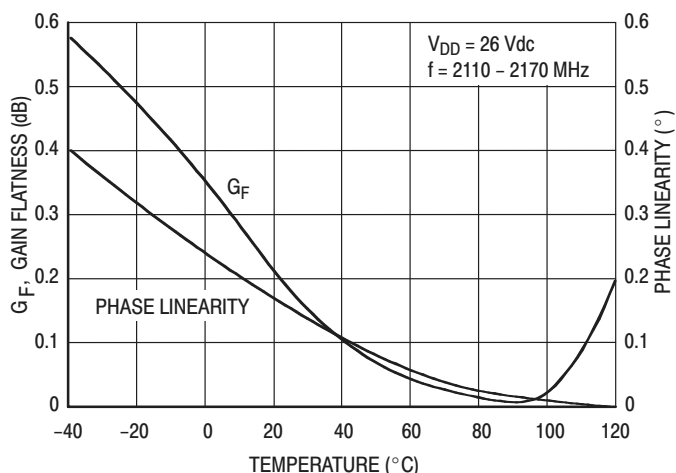


**Figure 4. ITO, P1dB versus Temperature**



**Figure 5. Phase<sup>(1)</sup>, Group Delay<sup>(1)</sup> versus Temperature**

<sup>(1)</sup>In Production Test Fixture



**Figure 6. Gain Flatness, Phase Linearity versus Temperature**

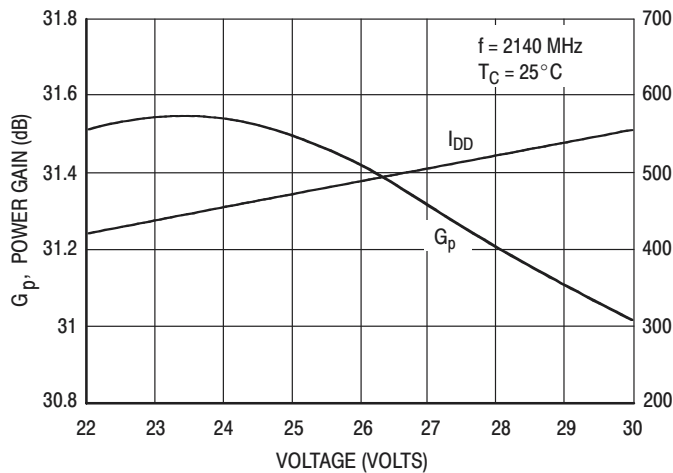


Figure 7. Power Gain,  $I_{DD}$  versus Voltage

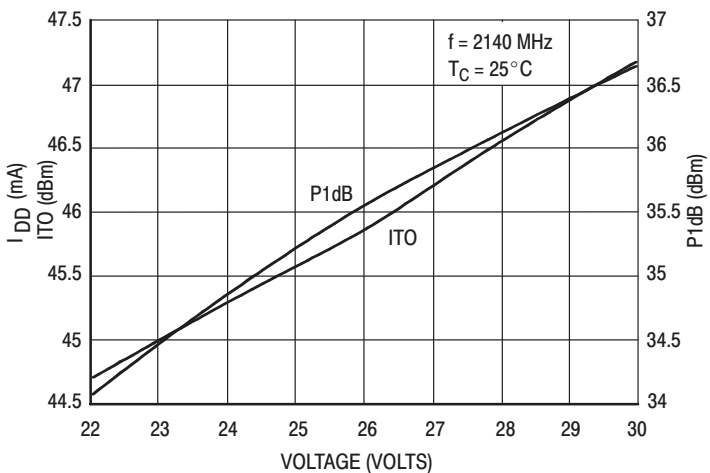


Figure 8. ITO, P1dB versus Voltage

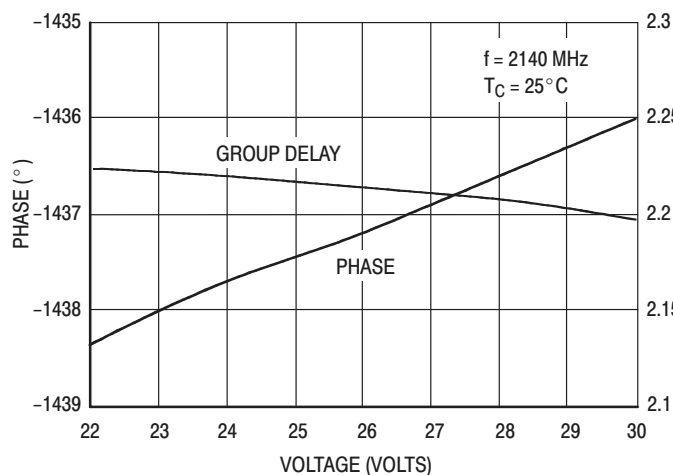


Figure 9. Phase<sup>(1)</sup>, Group Delay<sup>(1)</sup> versus Voltage

<sup>(1)</sup>In Production Test Fixture

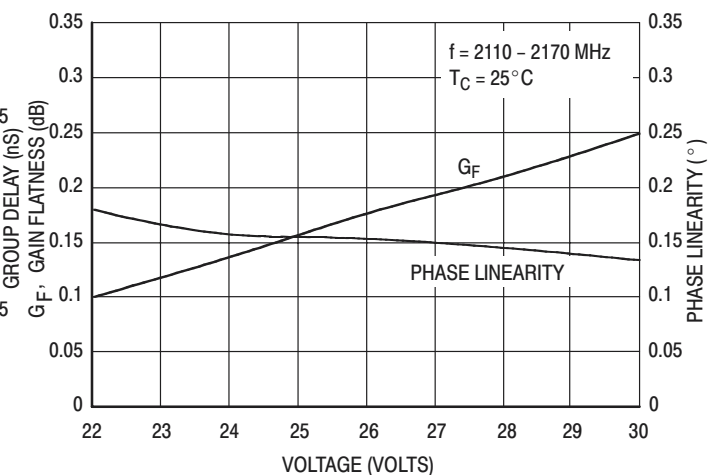
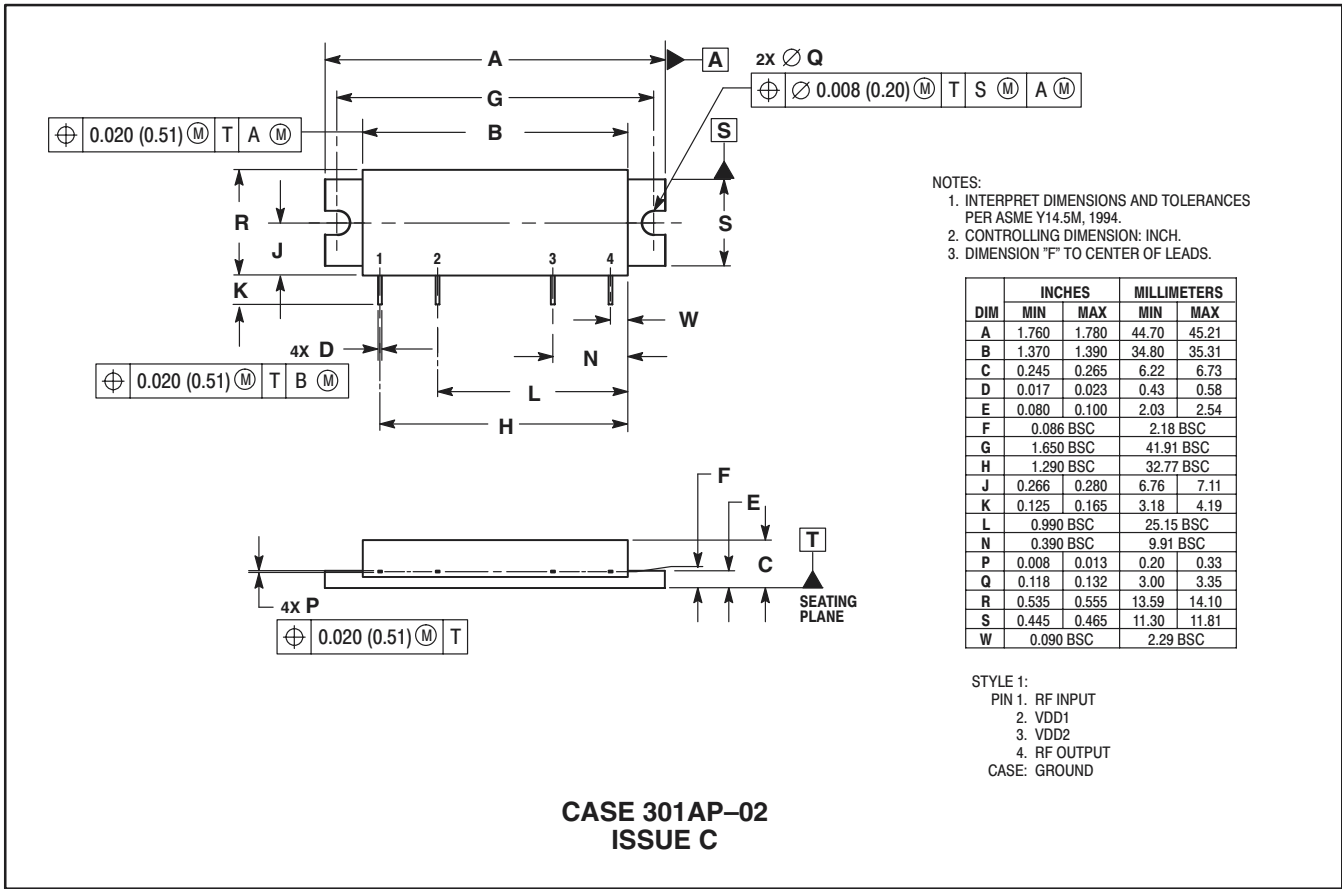


Figure 10. Phase Linearity, Gain Flatness versus Voltage

## PACKAGE DIMENSIONS



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