# SIEMENS

Signal Processing Codec Filter (SICOFI®)

PEB 2060

Features

- Single chip codec and filter
- Band limitation according to all CCITT and AT & T recommendations
- Digital Signal Processing techniques
- Digital voice transmission
  - PCM encoded (A-law or µ-law)
  - linear (16 bit 2's complement)
- Programmable digital filters for
  - impedance matching
  - transhybrid balancing
  - gain
  - frequency response correction
- Configurable three pin serial interface
  - 512-kHz-SLD-Bus (e.g. to PEB 2050/52)
  - burst mode with bit rates up to 4 Mbit/s
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities
  - three digital loop back modes
  - two analog loop back modes
  - on chip tone generation
- No trimming or adjustments
- No external components
- Variable clock selection
- Signaling expansion possible
- Prepared for three-party conferencing
- Advanced low power 2µCMOS technology
- Power supply + / − 5 V
- Meets or exceeds CCITT and LSSGR recommendations

VPL 05018

P-LCC-28-R

VPD 05053
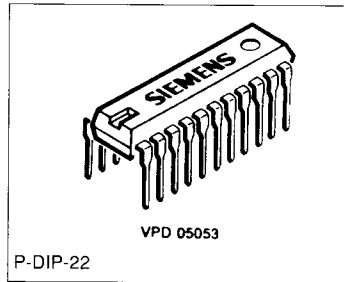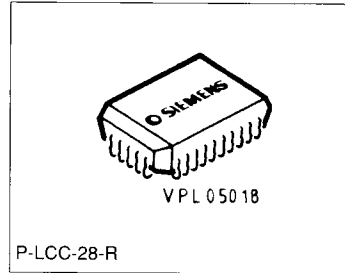
P-DIP-22

| Type	Version	Ordering Code	Package
PEB 2060-N	V 4.4	Q67100-H8393	P-LCC-28-R (SMD)
PEB 2060-P	V 4.4	Q67100-Z170	P-DIP-22

03.92

General Description

The Signal Processing Codec Filter (SICOFI) PEB 2060 is a fully integrated PCM codec (coder/decoder) and transmit/receive filter fabricated in advanced CMOS technology for applications in digital telecommunication systems. Based on a digital filter concept, the PEB 2060 provides improved transmission performance and high flexibility. The digital signal processing approach supports software controlled adjustment of the analog behavior, including attractive features such as programmable transhybrid balancing, impedance matching, gain and frequency response correction.
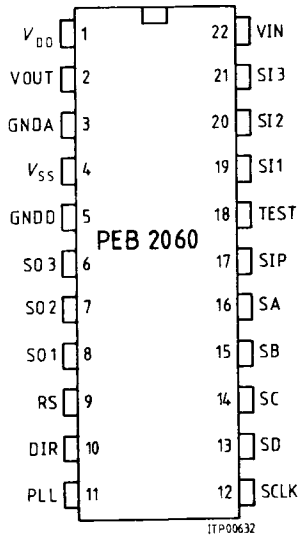
Pin Configuration

(top view)

P-LCC-28-R
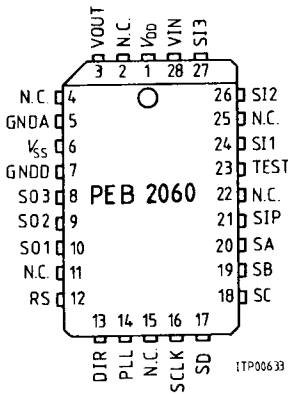
P-DIP-22

Pin Definitions and Functions

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-28-R	**P-DIP-22**			
1	1	V_{DD}	I	+ 5 V power supply
6	4	V_{SS}	I	– 5 V power supply
5	3	GNDA	I	Ground analog, not internally connected to GNDD. All analog signals are referred to this pin
7	5	GNDD	I	Ground digital, not internally connected to GNDA. All digital signals are referred to this pin
28	22	VIN	I	Analog voice input to transmit path
3	2	VOUT	O	Analog voice output of the received digital voice
16	12	SCLK	I	Slave clock
13	10	DIR	I	Frame synchronisation signal (direction signal)
21	17	SIP	I/O	Serial interface port, bidirectional serial data port
12	9	RS		Reset input, RS forces the SICOFI to power down mode and initializes the configuration registers
23	18	TEST	I	Test input, normally connected to GNDD
14	11	PLL	I	Clock selection (see Appendix A)
24	19	SI1	I	Signaling inputs. Data present at SI is sampled and transmitted via the serial interface
26	20	SI2	I	
27	21	SI3	I	
10	8	SO1	O	Signaling outputs. Data received via the serial interface is latched and fed to these outputs
9	7	SO2	O	
8	6	SO3	O	
20	16	SA	I/O	Programmable I/O signaling pins. Each of these pins may be declared input individually with adequate SICOFI status settings. If 2 SICOFIs are connected to 1 serial interface, pin SA (high/low) assigns voice, control and signaling bytes
19	15	SB	I/O	
18	14	SC	I/O	
17	13	SD	I/O	

SICOFI® Principles

The SICOFI codec filter solution is a highly digital approach utilizing the advantages of digital signal processing such as excellent performance, high flexibility, easy testing, no sensitivity to fabrication and temperature variations, no problems with crosstalk and power supply rejection.

SICOFI® Signal Flow Graph
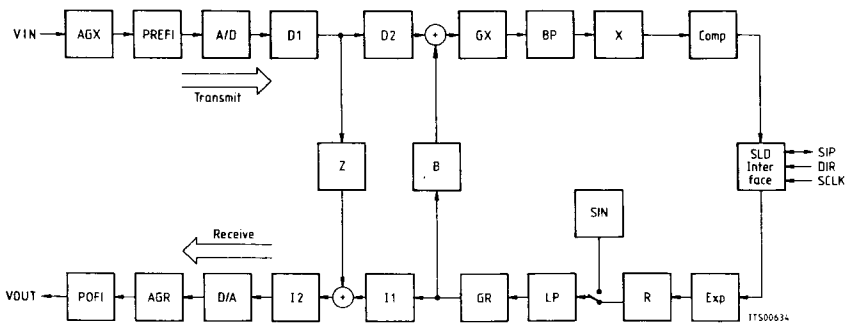
Transmit Direction

The analog input signal is A/D converted, digitally filtered and transmitted either PCM-encoded or linear. Antialiasing is done with a 2nd order Sallen-Key prefilter (PREFI). The A/D Converter (ADC) is a modified slopeadaptive interpolative sigmadelta modulator with a sampling rate of 128 kHz. Digital downsampling to 8 kHz is done by subsequent decimation filters D1 and D2 together with the PCM bandpass filter (BP).
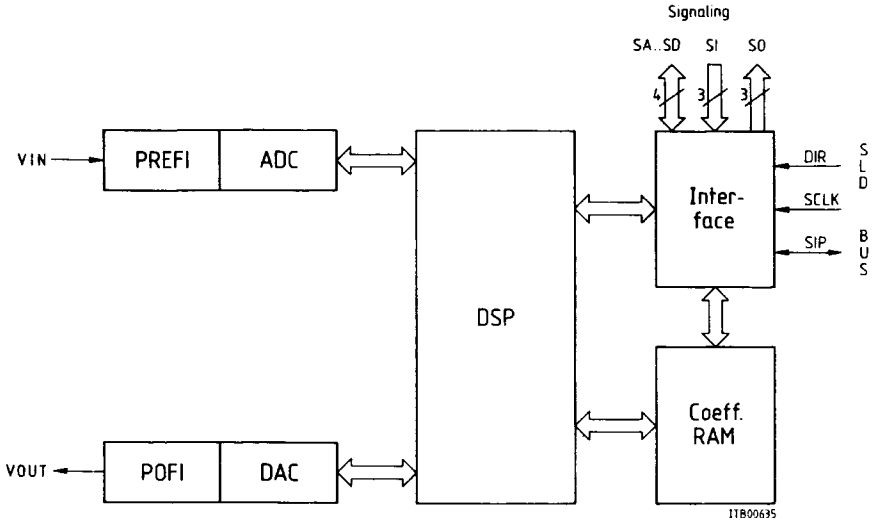
Receive Direction

The digital input signal is received PCM-encoded or linear, digitally filtered and D/A converted to generate the analog output signal. Digital interpolation up to 128 kHz is done by the PCM lowpass filter (LP) and the interpolation filters I1 and I2. The D/A Converter (DAC) output is fed to the 2nd order Sallen-Key postfilter (POFI).

Programmable Functions

The high flexibility of the SICOFI is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.

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SICOFI® Block Diagram

Signaling

SA..SD   SI   SO

4   3   3

VIN → | PREFI | ADC | ⇔

| Inter-face | DIR S L D
              SCLK
              SIP B U S

DSP

VOUT ← | POFI | DAC | ⇔

| Coeff. RAM |

ITB00635

The SICOFI bridges the gap between analog and digital voice signal transmission in modern telecommunication systems. High performance oversampling Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) provide the conversion accuracy required. An analog antialiasing prefilter (PREFI) and smoothing postfilter (POFI) is included. The dedicated on chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The three pin serial SLD-Bus interface handles digital voice transmission and SICOFI feature control. Specific filter programming is done by downloading coefficients to the coefficient ram (CRAM).

The ten pin parallel Signaling Interface provides for a powerful per line SLIC control.

Serial Line Data Interface (SLD Interface)

The exchange of data on the SLD-Bus is based on a bidirectional, bitserial interface consisting of three pins: SIP, DIR and SCLK.
Data is written or read out on the Serial Interface Port SIP under control of the frame synchronization signal DIR with a period of 125 μs [*]. The interface clock frequency supplied at the Slave CLock pin SCLK is 512 kHz [*]. The rate of the serial data stream on the SIP pin is 512 kbit/s, that is 64 bits per each 8 kHz frame [*].

Starting with the rising edge of DIR, four bytes of information are transferred on the SLD-Bus to the SICOFI, followed by four bytes from the SICOFI to the SLD-Bus. Bit 7 (MSB) is the first bit transferred and bit 0 (LSB) is the last one of each byte.

Byte Sequence and Timing at Serial Interface Port SIP
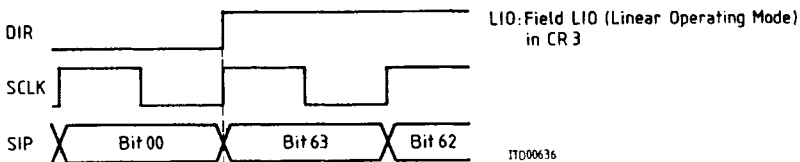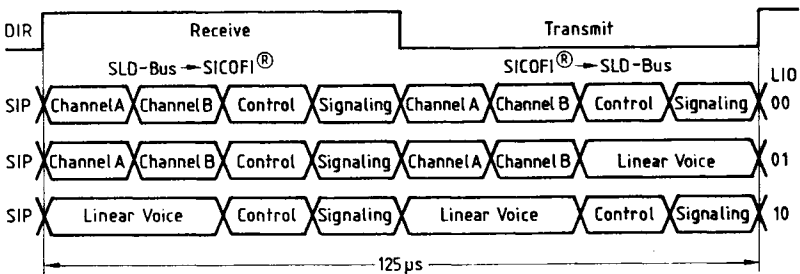
[*] for applications with other clock rates see Appendix A

Programming

A message-orientated byte transfer is used, due to the fact that the SICOFI needs extended control information. One control byte per frame and direction is transferred. With the appropriate received commands, data can be written to the SICOFI or read from the SICOFI onto the SLD-bus.

Data transfer to the SICOFI starts with a write command, followed by up to 8 bytes of data. The SICOFI responds to a read command with the requested information, starting at the next transmission period. If no status modification or data exchange is required a NOP byte is transferred (**see Programming Procedure**).

Control Bytes

The 8-bit control bytes consist of either commands, status information or data. There are three different classes of SICOFI commands:

NOP   NO OPERATION:
      no status modification or data exchange

SOP   STATUS OPERATION:
      SICOFI status setting/monitoring

COP   COEFFICIENT OPERATION:
      filter coefficient setting/monitoring

The class of command is selected by Bit 2 and 3 of the control byte as shown below. Due to the extended SICOFI feature control facilities, SOP- and COP-commands contain additional information.

BIT	7	6	5	4	3	2	1	0
NOP	1	1	1	1	1	1	1	1
SOP					0	1		
COP					X	0		

X ... don't care

NOP Command

If no status modification of the SICOFI or control data exchange is required, a No Operation Byte NOP is transferred.

BIT	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	1	1

SOP Command

To modify or evaluate the SICOFI status, the contents of up to four configuration registers CR1, CR2, CR3 and CR4 may be transferred to or from the SICOFI. This is done by a SOP-Command (Status Operation Command).

BIT	7	6	5	4	3	2	1	0
	AD	R/W	PU	TR	0	1	LSEL	

AD   Address   AD = 0   A-SICOFI addressed
   Information   AD = 1   B-SICOFI addressed
   This bit is evaluated if two SICOFIs are
   connected to one SLD-port.
   A SICOFI is accessed, if AD is
   consistent with the level at pin SA
   (**see Signaling Byte, Programming Procedure**).

R/W   Read/Write   R/W = 0   Write to SICOFI
   Information   R/W = 1   Read from SICOFI
   Enables reading from the SICOFI
   or writing information to the SICOFI.

PU   Power Up/   PU = 1   sets the SICOFI to power-up mode (operating)
   Power Down   PU = 0   resets the SICOFI to power-down (standby mode)
   (**see also CR3**)

TR   Three Party   TR = 1   The received voice bytes of channel A
   Conference   and channel B are added (A + B).
   The result is filtered, D/A converted and
   transferred to analog output VOUT (**see also CR3**).

LSEL   Length Select Information, identifies the number of subsequent data bytes
   (**see also Programming Procedure**)
   LSEL = 0 0   no byte following
   LSEL = 1 1   CR1 is following
   LSEL = 1 0   CR2 and CR1 are following
   LSEL = 0 1   CR4, CR3, CR2 and CR1 are following
   in this case the PU and TR bits are not overwritten.

CR1 Configuration Register 1

This configuration register is used for enabling/disabling the programmable digital filters (DB ... RG) and for accessing testmodes (TM1).

BIT	7	6	5	4	3	2	1	0
	DB	RZ	RX	RR	RG		TM1	

DB	Disable B-Filter	DB = 0	B-Filter enabled
		DB = 1	B-Filter disabled
RZ	Restore Z-Filter	RZ = 0	Z-Filter disabled
		RZ = 1	Z-Filter enabled
RX	Restore X-Filter	RX = 0	X-Filter disabled
		RX = 1	X-Filter enabled
RR	Restore R-Filter	RR = 0	R-Filter disabled
		RR = 1	R-Filter enabled
RG	Restore	RG = 0	GX-GR-Filter disabled
	GX-GR-Filter	RG = 1	GX-GR-Filter enabled

TM1			TEST MODES
0	0	0	No test mode
0	0	1	Analog loop back via Z-filter (H (Z) = 1) [1]
0	1	0	Disable highpass filter (part of bandpass BP)
0	1	1	Cut off receive path
1	0	0	Initialize data ram with 0x0000
1	1	0	Digital loop back via B-filter (H (B) = 1) [2]
1	1	1	Digital loop back via PCM-register [3]

Other codes are reserved for future use.

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[1] Output of the interpolation filter I1 is set to 0.
  Value of transfer function of the Z-filter is 1 (not programmable).
[2] Output of the low pass decimation filter D2 is set to 0.
  Value of transfer function of the B-filter is 1 (not programmable).
[3] PCM in = PCM out. This testmode is also available in standby mode.

CR2 Configuration Register 2

BIT	7	6	5	4	3	2	1	0
	D	C	B	A	EL	AM	μ/A	PCS

The first four bits D ... A in this register, program the four bidirectional signaling pins SD ... SA. With two SICOFIs on one SLD-port only pin SD can be used, pin SA is always input in this case and indicates the address of the SICOFI.

SA = 0 : A-SICOFI, SA = 1 : B-SICOFI (**see also bit AD in SOP-command**).

D	Signaling	D = 0	SD is output
	Pin SD	D = 1	SD is input

C	Signaling	C = 0	SC is output
	Pin SC	C = 1	SC is input

B	Signaling	B = 0	SB is output
	Pin SB	B = 1	SB is input

A	Signaling	A = 0	SA is output
	Pin SA	A = 1	SA is input

EL	Signaling	EL = 0	No expansion logic
	Expansion Logic	EL = 1	Expansion logic provided

Signaling expansion logic is only possible with one SICOFI on port (**see also Signaling Byte**)

AM	Address Mode	AM = 0	Two SICOFIs on SLD port
		AM = 1	One SICOFI on SLD port

The SICOFI access to the SLD-Bus voice channel is controlled by AM and TR.

		Receive (SLD-Bus ⇒ SICOFI)		**Transmit (SICOFI ⇒ SLD-Bus)**	
AM	**TR**	**SICOFI A**	**SICOFI B**	**SICOFI A**	**SICOFI B**
0	0	channel A	channel B	channel A	channel B
0	1	channel B	channel A	channel B	channel A
1	0	channel A	------	channel A, B [1]	------
1	1	channel A + B [2]	------	channel A, B [1]	------

μ/A	PCM-law	μ/A = 0	A-law
		μ/A = 1	μ-law (μ255 PCM)

PCS	B-Filter	PCS = 0	Programmed coefficients
	Coefficients	PCS = 1	Fixed coefficients

[1] The SICOFI transmits the same byte in channel A and B.
[2] Three Party Conference.

CR3 Configuration Register 3

BIT	7	6	5	4	3	2	1	0
	AGX		AGR		PU	TR	LIO	

AGX Analog Gain Control Transmit-Path

AGX = 0 0	0 dB
AGX = 0 1	6.03 dB amplification
AGX = 1 0	12.06 dB amplification
AGX = 1 1	14 dB amplification

AGR Analog Gain Control Receive-Path

AGR = 0 0	0 dB
AGR = 0 1	6.03 dB attenuation
AGR = 1 0	12.06 dB attenuation
AGR = 1 1	14 dB attenuation

PU Power Up / Power Down [1]

PU = 0	Power Down (standby)
PU = 1	Power Up (operating)

TR Three Party Conference/Reverse Operating Mode (**see CR2**) [1]

LIO Linear Operating Mode (**see Serial Interface**)

LIO = 0 0	PCM mode
LIO = 0 1	Linear mode 1 [2]
LIO = 1 0	Linear mode 2

(Change of linear mode becomes valid in the next DIR-cycle).

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[1] The bits PU and TR may also be overwritten by a SOP Command with LSEL ≠ 0 1 (PU and TR are part of the SOP Command).
With LSEL = 0 1, the bits PU and TR in the SOP Command are ignored.

[2] Subsequent to a SOP/COP-read Command the control and signaling information is transmitted instead of linear voice.

CR4 Configuration Register 4

BIT	7	6	5	4	3	2	1	0
		TM3		0	0		TM4	

TM3	TEST MODES
0 0 0	No test mode
0 0 1	Additional + 6 dB digital gain in transmit direction (GX)
0 1 1	Additional + 12 dB digital gain in transmit direction (GX)
1 0 0	Enable on chip tone generation [1]
1 1 0	Far analog loop back [2]

TM4	TEST MODES
0 0 0	No test mode
1 0 0	Digital loop back via analog port (VIN = VOUT)

Other codes are reserved for future use.

[1] With the R-filter disabled a 2 kHz, 0 dBm0 sinusoidal signal is fed to the input of the receive Lowpass Filter LP (other frequencies see Appendix B).
[2] The output of the X-filter is fed to the input of the R-filter (8 kHz, 16 bit linear).

COP Command

BIT	7	6	5	4	3	2	1	0

AD	R/W			CODE			

With a COP Command coefficients for the programmable filters can be written to the SICOFI coefficient ram or transmitted on the SLD-bus for verification.

AD   Address   AD = 0   A-SICOFI addressed
Information   AD = 1   B-SICOFI addressed
This bit is evaluated with two SICOFIs on one SLD-port only.
With two SICOFIs on port, a SICOFI is identified, if AD is consistent
with the level at pin SA (**see Signaling Byte, Programming Procedure**).

R/W   Read/Write   R/W = 0   Write to SICOFI
Information   R/W = 1   Read from SICOFI
This bit indicates whether filter coefficients are written to the SICOFI
or read from the SICOFI.

CODE							
0	0	0	0	1	1	B-Filter coefficients part 1	followed by 8 bytes of data
0	0	1	0	1	1	B-Filter coefficients part 2	followed by 8 bytes of data
0	1	0	0	1	1	Z-Filter coefficients	followed by 8 bytes of data
0	1	1	0	0	0	B-Filter delay coefficients	followed by 4 bytes of data
1	0	0	0	1	1	X-Filter coefficients	followed by 8 bytes of data
1	0	1	0	1	1	R-Filter coefficients	followed by 8 bytes of data
1	1	0	0	0	0	GX- and GR-Filter coefficients *)	followed by 4 bytes of data

Other codes are reserved for future use.

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*) In the range – 8 dB to 8 dB gain adjustment is possible in steps $\leq$ 0.25 dB

Signaling Byte

The signaling interface of the SICOFI consists of 10 pins.
3 transmit signaling inputs: SI1, SI2 and SI3
3 receive signaling outputs: SO1, SO2 and SO3
4 bidirectional programmable signaling pins: SA, SB, SC and SD

Data present at SI1 ... SI3 and possibly at some or all of SA ... SD (if programmed as inputs) are sampled and transferred serially on SIP onto the SLD-bus. Data received serially on SIP from the SLD-Bus are latched and fed to SO1 ... SO3 and possibly to some of SA ... SD if programmed as output.

The signaling field format is generally:

in receive direction:

BIT	7	6	5	4	3	2	1	0
	SO1	SO2	SO3	SD	SC	SB	SA	SEL

in transmit direction:

BIT	7	6	5	4	3	2	1	0
	SI1	SI2	SI3	SD	SC	SB	SA	SEL

where SEL is the signaling expansion bit if EL = 1 in CR2.

For the different cases possible, the signaling byte format at SIP is

Bit Case	Receive Signaling Byte								Transmit Signaling Byte							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	SC	SB	SA	0
2	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	SC	SB	SA	Z
3	SO1	SO2	SO3	SD	SC	SB	SA	X	SI1	SI2	SI3	0	0	0	0	0
4	SO1	SO2	SO3	SD	SC	SB	SA	X	SI1	SI2	SI3	Z	Z	Z	Z	Z
5 A-SIC	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	Z	Z	Z	Z
B-SIC	X	X	X	X	SO1	SO2	SO3	X	Z	Z	Z	Z	SI1	SI2	SI3	SD
6 A-SIC	SO1	SO2	SO3	SD	X	X	X	X	SI1	SI2	SI3	0	Z	Z	Z	Z
B-SIC	X	X	X	X	SO1	SO2	SO3	SD	Z	Z	Z	Z	SI1	SI2	SI3	0

Z ... high impedance, X ... don't care

Cases

1   One SICOFI is connected to one SLD port, EL = 0 (no signaling expansion logic provided); SA … SD are programmed as transmit signaling inputs.

2   One SICOFI connected to one SLD port, EL = 1 (signaling expansion logic provided); SA … SD are programmed as transmit signaling inputs.

3   One SICOFI is connected to one SLD port; EL = 0 (no signaling expansion logic provided); SA … SD are programmed as receive signaling outputs.

4   One SICOFI is connected to one SLD port; EL = 1 (signaling expansion logic provided); SA … SD are programmed as receive signaling outputs.

If a signaling expansion logic is provided (see case 2 and 4), the signaling bits SA … SD which are programmed as signaling inputs or outputs can be used as additional expansion bits in receive or transmit direction, respectively. As far as SICOFI is concerned, SIP is in a high-impedance (Z) state or "dont care" (Y) state while these bits are transferred.

5   Two SICOFIs are connected to one SLD port; SD is programmed as transmit signaling input.

6   Two SICOFIs are connected to one SLD port; SD is programmed as receive signaling output.

If two SICOFIs are connected to one SLD port, no signaling expansion logic is possible. SA is programmed as input automatically, and defines the addressed SICOFI:

SA = 0 : A-SICOFI
SA = 1 : B-SICOFI.

SB and SC are not usable with two SICOFIs on one SLD port.

Programming Procedure

The following table shows some control byte sequences. If the SICOFI has to be configured completely during initialization, up to 60 bytes will be transferred.

DIR | Receive | Transmit | Receive | Transmit | Receive | Transmit | Receive | Transmit | Receive | Transmit | Receive

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DIR

No Operation

|NOP |NOP |NOP |NOP |NOP |NOP |NOP |NOP |NOP |NOP |

SOP Write

LSEL = 00	SOP	NOP								
LSEL = 11	SOP	NOP	CR1	NOP						
LSEL = 10	SOP	NOP	CR2	NOP	CR1	NOP				
LSEL = 01	SOP	NOP	CR4	NOP	CR3	NOP	CR2	NOP	CR1	NOP

SOP Read

LSEL = 00	SOP	NOP						
LSEL = 11	SOP	CR1						
LSEL = 10	SOP	CR2	X	CR1				
LSEL = 01	SOP	CR4	X	CR3	X	CR2	X	CR1

COP Write

4 Bytes	COP	NOP	DB4	NOP	DB3	NOP	DB2	NOP	DB1	NOP
8 Bytes	COP	NOP	DB8	NOP	DB7			NOP	DB1	NOP

COP Read

4 Bytes	COP	DB4	X	DB3		DB1	X	CR2	X	CR1
8 Bytes	COP	DB8	X	DB7		DB1	X	CR2	X	CR1

X … don't care   DB1, DB2 … DB8 … coefficient Data Byte 1 … 8

Operating Modes

Basic Setting

Upon initial application of V_{DD} or reseting pin RS to "1" while operating, the SICOFI enters a basic setting mode. Basic setting means, that the SICOFI configuration registers CR1 ... CR4 are initialized. All CR1 bits are set to "0" (all programmable filters are disabled except the B-Filter where fixed coefficients are used, no test mode); CR2 is set to "1" (SA ... SD are inputs, signaling expansion logic is provided, one SICOFI on SLD-port, μ-law chosen and fixed B-Filter coefficients used). All CR3 and CR4 bits are reset to "0" (no additional amplification or attenuation, no linear mode, power down, no test mode). Receive signaling registers are cleared. SIP is in high-impedance state, the analog output VOUT and the receive signaling outputs SO1 ... SO3 are forced to ground.

The serial interface is active to receive commands starting with the next 8-kHz SLD-Bus frame. The serial interface port SIP remains in high-impedance state until CR2 has been defined.

If two SICOFIs are connected to one SLD port, both SICOFI's get the same SOP and CR2 information during initialization. The subsequent CR1 byte is assigned to the addressed SICOFI only. If the two SICOFI's need different CR2 information, the SOP-CR2 sequence has to be provided once again (each SICOFI knows its address now).

If any voltage is applied to any input before initial application of V_{DD}, the SICOFI may not enter the Basic Setting Mode. In this case it is necessary either to reset the SICOFI via the RS Pin or to initialize the configuration registers CR1, CR2, CR3, CR4.

Standby Mode

Upon reception of a SOP command to load CR2 from the basic setting, the SICOFI enters the standby mode (basic setting replaced by individual CR2). Being in the operating mode, the SICOFI is reset to standby mode with a Power-Up bit PU = 0 (in CR3 or in the SOP-command directly). The serial interface is active to receive and transmit new commands and data.

Operating Mode

From the standby mode, the operating mode is entered upon recognition of a Power-Up bit PU = 1 (in CR3 or in the SOP-command directly).

Transmission Characteristics

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing: B; impedance matching: Z; frequency-response correction: X, R) needs a complete knowledge of the SICOFIs analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test condition below.

T_A = 0 ˚C to 70 ˚C; V_{DD} = 5 V ± 5 %; V_{SS} = – 5 V ± 5 %; GNDA = GNDD = 0 V

R_L > 10 kΩ; C_L < 50 pF; H(Z) = H(B) = 0; H(X) = H(R) = 1;

GX = 0 to 8 dB; GR = 0 to – 8 dB; AGX = 0, 6.03, 12.06, 14 dB;

AGR = 0, – 6.03, – 12.06, – 14 dB;

f = 1000 Hz; 0 dBm0; A-law or μ-law;

A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms. A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V (A-law, [μ-law]).

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain (either value) [1]					
Gain absolute (AGR = AGX = 0)	G				
T_A = 25 ˚C, V_{DD} = 5 V, V_{SS} = – 5 V		– 0.2	± 0.06	0.2	dB
T_A = 0–70 ˚C; V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%		– 0.3		0.3	dB
Gain absolute (AGR = 0 to 14 dB, AGX = 0 to 14 dB)	G				
T_A = 0–70 ˚C; V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%		– 0.4	± 0.10	0.4	dB
Total harmonic distortion, 0 dBm0; f = 300 Hz to 3400 Hz	*THD*		– 50	– 44	dB
Intermodulation $2f1 - f2$ [2]	*IMD*			– 42	dB
$2f1 - f2$ [3]				– 56	dB
Crosstalk 0 dBm0; f = 300 Hz to 3400 Hz					
Transmit to receive	CT_{XR}		– 85	– 80	dB
Receive to transmit	CT_{RX}		– 85	– 80	dB
Idle channel noise,					
transmit, psophometric, A-law VIN = 0 V	N_{TP}			– 67.4	dBm0p
transmit, C-message, μ-law VIN = 0 V	N_{TC}			17.5	dBrnc
receive, psophometric, A-law idle code + 0	N_{RP}		– 82	– 78	dBm0p
receive, C-message, μ-law idle code + 0	N_{RC}		8	12	dBrnc

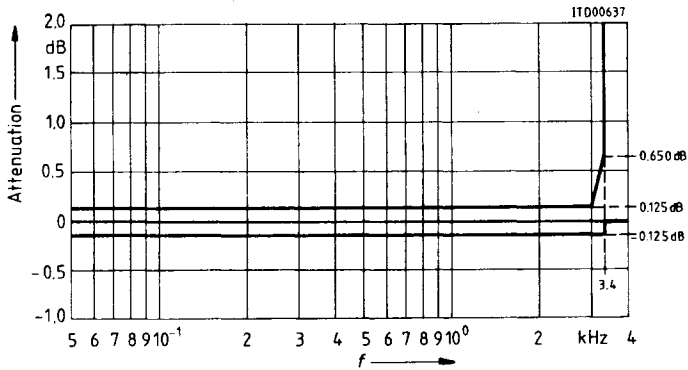[1] R_L = 300 Ω causes an additional attenuation in the range between – 0.1 to 0 dB.

[2] Equal input levels in the range between – 4 dBm0 and – 21 dBm0; different frequencies in the range between 300 Hz and 3400 Hz.

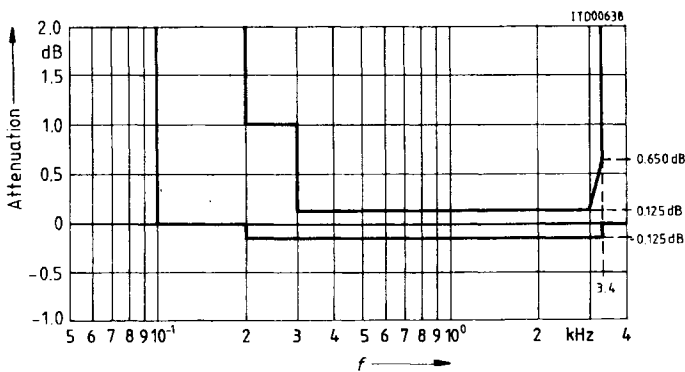[3] Input level – 9 dBm0, frequency range 300 Hz to 3400 Hz and – 23 dBm0, 50 Hz.

Attenuation Distortion

Attenuation deviations stay within the limits in the figures below.

Receive: Reference frequency 1 kHz, input signal level 0 dBm0

ITD00637

2.0 dB
1.5
1.0
0.5
0
−0.5
−1.0

0.650 dB
0.125 dB
0.125 dB
3.4

5 6 7 8 910⁻¹   2   3   4   5 6 7 8 910⁰   2   kHz   4

$f \longrightarrow$

Attenuation

Transmit: Reference frequency 1 kHz, input signal level 0 dBm0

ITD00638

2.0 dB
1.5
1.0
0.5
0
−0.5
−1.0

0.650 dB
0.125 dB
0.125 dB
3.4

5 6 7 8 910⁻¹   2   3   4   5 6 7 8 910⁰   2   kHz   4

$f \longrightarrow$

Attenuation

Group Delay

Maximum delays for operating the SICOFI with $H(B) = H(Z) = 0$ and $H(R) = H(X) = 1$, including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group delay deviations stay within the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Transmit Delay	D_{XA}			300	μs	$f = 1.4$ kHz
Receive Delay	D_{RA}			240	μs	$f = 300$ Hz

Group Delay Distortion: Input signal level 0 dBm0, reference frequency = 1.4 kHz
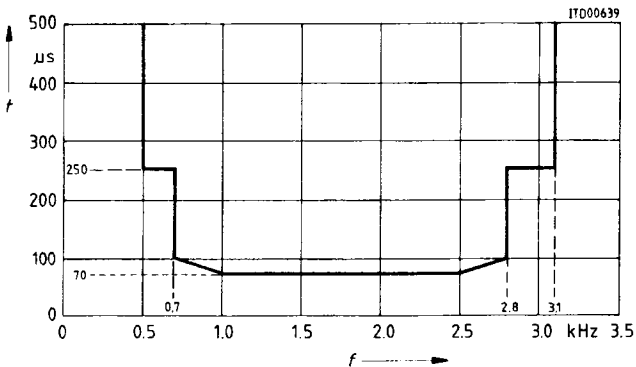
Out-of-Band Signals at Analog Input

With an out-of-band sine wave signal with frequency f and level A applied to the analog inpu
the level of any resulting frequency component at the digital output will stay at least X dB belov
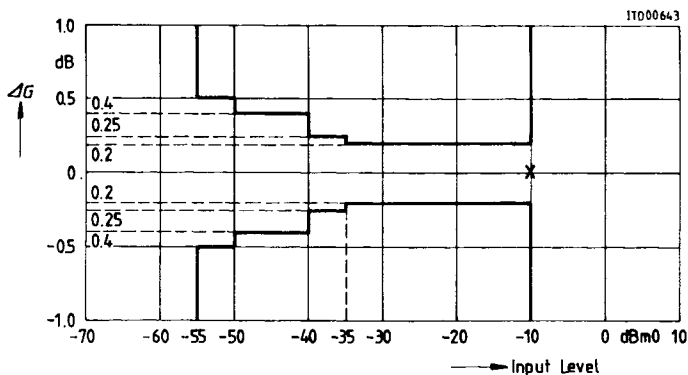level A.

Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave of frequency f applied to the digital input, the level of any resulting ou
of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wav
reference signal at the analog output.

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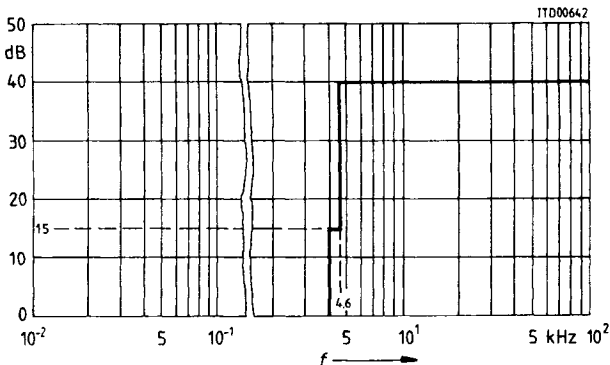
Gain Tracking (Receive and Transmit)

The gain deviations stay within the limits in the figures below

Gain Tracking: Measured with noise signal according to CCITT recommendations, reference level is − 10 dBm0, AGX = AGR = 0

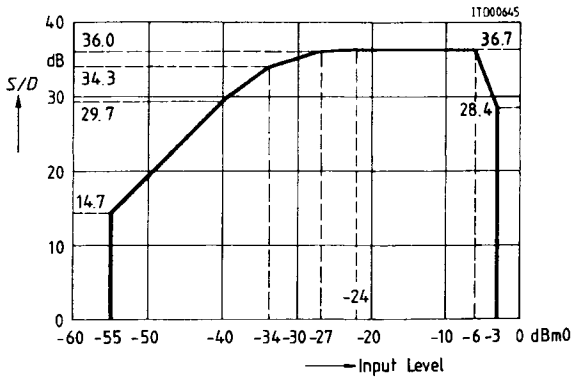**Gain Tracking:** Measured with sine wave in the range 700 to 1100 Hz, reference level is − 10 dBm0, AGX = AGR = 0
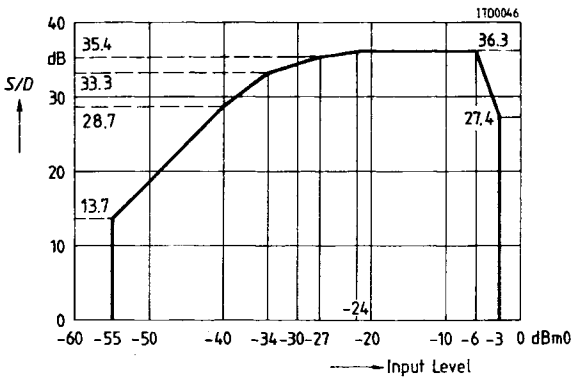

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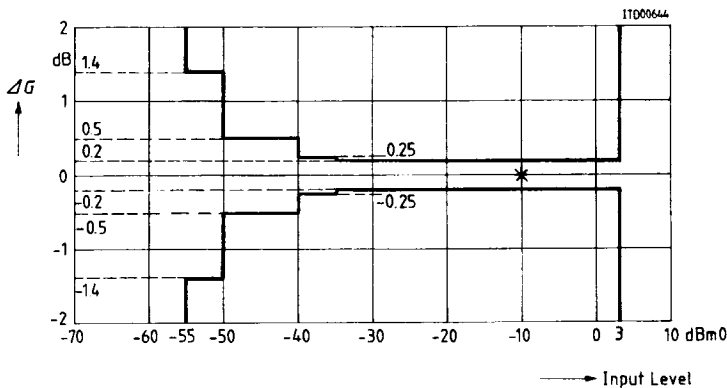
Total Distortion

The signal-to-distortion ratio exceeds the limits in the following figures.

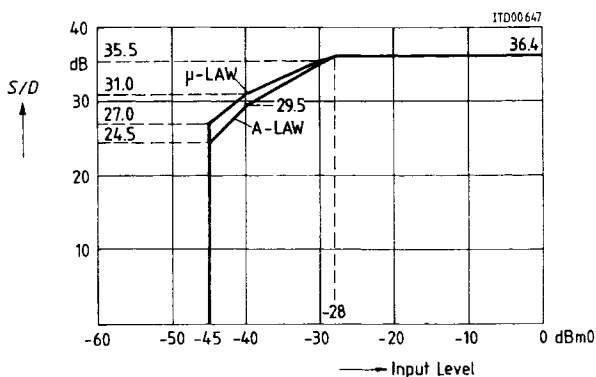**Receive:** Measured with noise signal according to CCITT recommendations

Transmit: Measured with noise signal according to CCITT recommendations

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The signal to distortion ratio exceeds the limits in the following figures.

Receive & Transmit: Measured with sine wave in the range 700 to 1100 Hz excluding submultiples of 8 kHz

Signal to Total Distortion CCITT Noise Signal Digital-Digital (A-law and μ-law)

Parameter			Total Distortion	
	Input Level	Unit	min.	Unit
Digital Loop Back via B-Filter or Digital Loop Back via Analog port	0	dBm0	31	dB
	– 30	dBm0	31	dB
	– 40	dBm0	25	dB
	– 45	dBm0	20	dB

Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay – deviations inherent to the SICOFI A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP's etc.)

The SICOFI transhybrid loss is measured in the following way: A sine wave signal with level 0 dBm0 and a frequency in the range of 300 – 3400 Hz is applied to the digital input. The resulting analog output signal at pin VOUT is directly connected to VIN, e.g. with the SICOFI testmode "Digital Loop Back via Analog Port" (**see CR4**). The programmable filters R, GR, X, GX and Z are disabled, the balancing filter B is enabled with coefficients optimized for this configuration ($V_{OUT} = V_{IN}$).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below.

B-filter coefficients recommended for transhybrid loss measurement with $V_{OUT} = V_{IN}$

	COP-Write	Coefficients						
B-filter part 1	(83)	FD	29	FB	38	A1	A0	3C	42
B-filter part 2	(8B)	00	AF	62	2B	CF	D1	CA	A4
B-filter delay	(98)	19	19	11	19				

Parameter	Symbol	Limit Values min.	Limit Values typ.	Unit	Test Condition
Transhybrid loss at 500 Hz	THL_{500}	33	45	dB	$T_A = 25\,°C$,
Transhybrid loss at 2500 Hz	THL_{2500}	29	40	dB	$V_{DD} = 5\,V$, $V_{SS} = -5\,V$,
Transhybrid loss at 3000 Hz	THL_{3000}	27	35	dB	AGR = AGX = 0 dB
Transhybrid loss at 500 Hz	THL_{500}	29	40	dB	$T_A = 0$ to $70\,°C$,
Transhybrid loss at 2500 Hz	THL_{2500}	27	35	dB	$V_{DD} = 5\,V \pm 5\,\%$,
Transhybrid loss at 3000 Hz	THL_{3000}	25	30	dB	$V_{SS} = 5\,V \pm 5\,\%$,
					AGR = AGX = 0 dB
Transhybrid loss at 500 Hz	THL_{500}	27	40	dB	$T_A = 0$ to $70\,°C$,
Transhybrid loss at 2500 Hz	THL_{2500}	25	35	dB	$V_{DD} = 5\,V \pm 5\,\%$,
Transhybrid loss at 3000 Hz	THL_{3000}	23	30	dB	$V_{SS} = -5\,V \pm 5\,\%$,
					AGR = AGX = 6.03,
					12.06,
					14.00 dB

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{DD} referred to GNDD		– 0.3	5.5	V
V_{SS} referred to GNDD		– 5.5	0.3	V
GNDA to GNDD		– 0.6	0.6	V
Analog input and output voltage				
referred to $V_{DD} = 5$ V, $V_{SS} = - 5$ V	V_{IN}	– 10.3	0.3	V
referred to $V_{SS} = - 5$ V, $V_{DD} = 5$ V	V_{IN}	– 0.3	10.3	V
All digital input voltages				
referred to GNDD = 0 V, $V_{DD} = 5$ V	V_{IN}	– 0.3	5.3	V
referred to $V_{DD} = 5$ V, GNDD = 0 V	V_{IN}	– 5.3	0.3	V
DC input and output current at any input or output pin	I_{DC}		10	mA
Storage temperature	T_{stg}	– 60	125	°C
Ambient temperature under bias	T_A	– 10	80	°C
Power dissipation	P_D		1	W

Operating Range

$T_A = 0$ to 70 °C; $V_{DD} = 5$ V $\pm$ 5%; $V_{SS} = - 5$ V $\pm$ 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current	I_{DD}					
stand by			2.1	4	mA	
operating			8	12	mA	
V_{SS} supply current	I_{SS}					
stand by			1.7	3	mA	
operating			5	8	mA	
Power supply rejection (of either supply/direction)	*PSRR*	30	44		dB	1 kHz 80 mVrms ripple
Power dissipation stand by	P_{Ds}		20	37	mW	
Power dissipation operating	P_{Do}		70	105	mW	

Electrical Characteristics

Digital Interface

T_A = 0 to 70 ˚C; V_{DD} = 5 V ± 5 %; V_{SS} = − 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	− 0.3	0.8	V	
H-input voltage	V_{IH}	2.0		V	
L-output voltage	V_{OL}		0.45	V	I_0 = − 2 mA
H-output voltage	V_{OH}	2.4		V	I_0 = 400 μA
Input leakage current	I_{IL}		± 1	μA	− 0.3 ≤ V_{IN} ≤ V_{DD}

Analog Interface

T_A = 0 to 70 ˚C; V_{DD} = 5 V ± 5%; V_{SS} = − 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input resistance	R_I	10		MΩ	
Analog output resistance	R_O		10	Ω	
Input offset voltage	V_{IO}		± 50	mV	
Output offset voltage	V_{OO}		± 50	mV	
Input voltage range	V_{IR}		± 3.2	V	
Output voltage range	V_{OR}	± 3.1		V	R_L ≥ 300 Ω; C_L ≤ 50 pF

SIP Interface Timing (SLD-Bus)
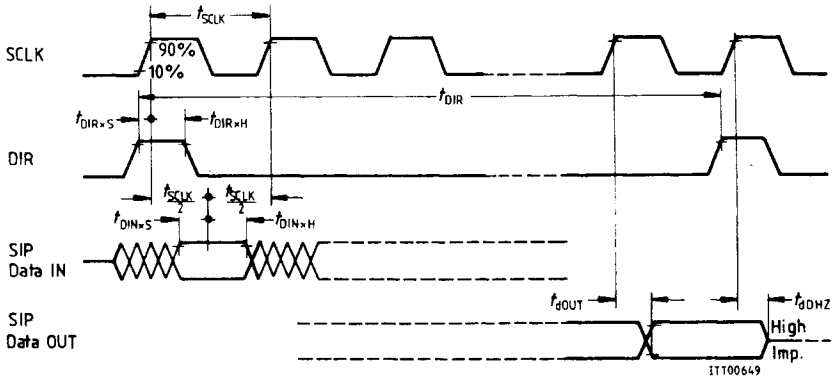
Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period SCLK	t_{SCLK}		1/512 kHz		
Duty cycle		20	50	80	%
Period DIR	t_{DIR}		125		µs
DIR setup time	$t_{DIR \times S}$	20	0	– 80	ns
DIR hold time	$t_{DIR \times H}$	250			ns
SIP data in setup time	$t_{DIN \times S}$	20			ns
SIP data in hold time	$t_{DIN \times H}$	100			ns
SIP data out delay	t_{dDOUT}		150	250	ns
SIP data out high impedance delay vs. SCLK	t_{dDHZ}		50	70	ns

Signaling Interface Timing

ITT02446
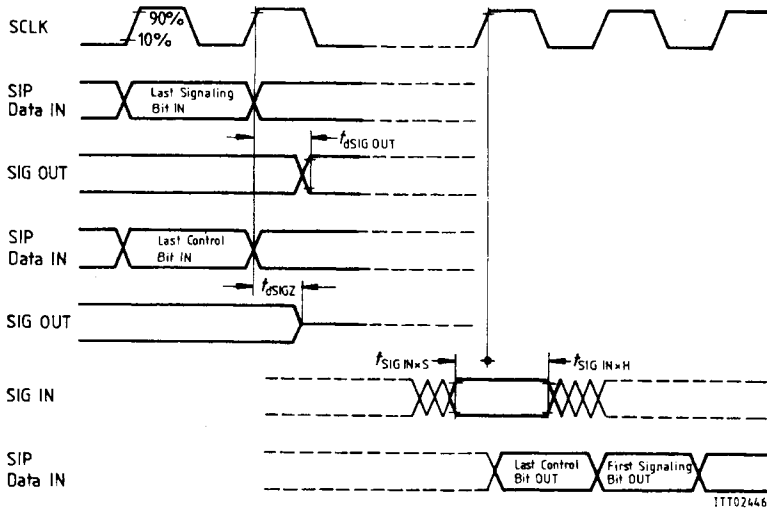
Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Delay signaling out vs. SCLK [1]	$t_{dSIGOUT}$		250	350	ns
Delay signaling high impedance vs. SCLK	t_{dSIGZ}		150	200	ns
SIG in setup time [2]	$t_{SIGIN \times S}$	50			ns
SIG in hold time [2]	$t_{SIGIN \times H}$	100			ns
Reset pulse width [3]	t_{RES}	500			ns

[1] Pins SO1 ... SO3; Pins SA ... SD as output
[2] Pins SI1 ... SI3; Pins SA ... SD as input
[3] SICOFI is ready to accept SOP/COP commands in the next DIR Cycle.
Spikes shorter than 244 ns will be ignored.
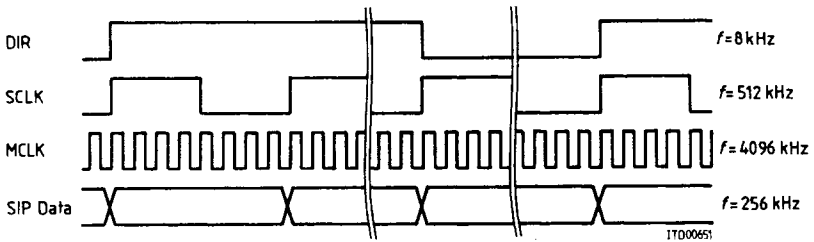
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Appendix A

Specific Interface Types

The SICOFI can be used with three different SLD-bus type interfaces. A specific interface type is selected with three pins: TEST, SI3 and PLL.
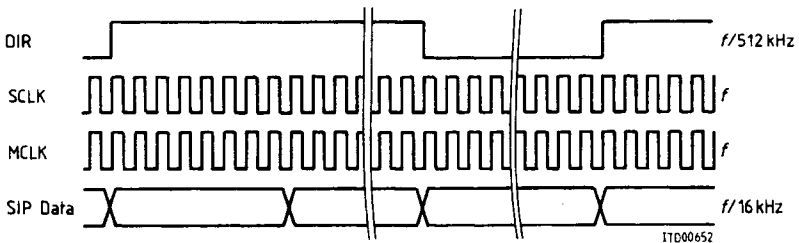
1) SLD-Bus Interface [1]

TEST	SI3	PLL
0	X	X

2) SLD-Bus Interface with Variable Clock Frequencies [2]

TEST	SI3[*]	PLL
1	0	0

[*] SI3 cannot be used as Signaling Pin

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[1] 4096-kHz Masterclock MCLK is generated from 512-kHz SCLK by on chip PLL
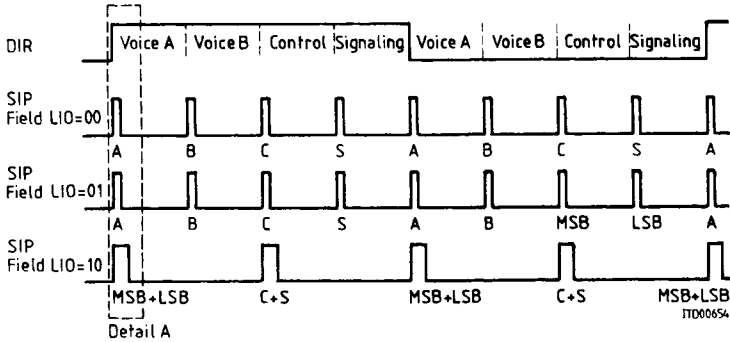[2] Maximum MCLK-frequency = 8 MHz

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3) Burst Mode Interface [1]

TEST	SI3[*]	PLL
1	0	1

[*] SI3 cannot be used
as Signaling Pin
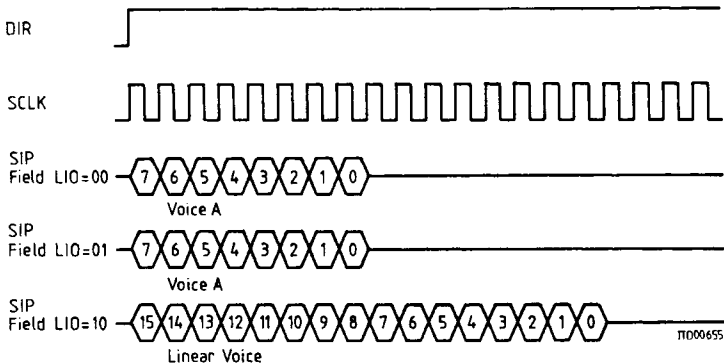
In burst-mode 8- or 16-bit bursts are received or transmitted, depending on the linear mode selected (**see** field LIO in **CR3**).

Detail A

Detail A

A ...   voice A   C ... control
B ...   voice B   S ... signaling
MSB ...   bit 15-8 of linear in- or output
LSB ...   bit 7-0 of linear in- or output

Appendix B

On Chip Tone Generation

By setting field TM3 in CR4 to '100' the on-chip tone generator is activated with a fixed frequency of 2 kHz. The frequency f_{TONE} may be programmed via the R-filter coefficients (R-filter enabled) in the range of 0 to 4 kHz. The gain may be adjusted with the programmable GR-filter.
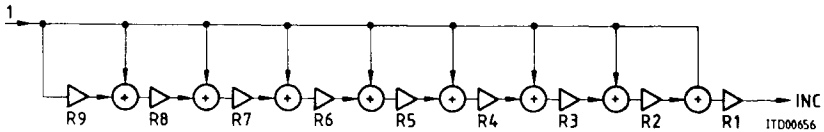
The trapezoidal tone generation algorithm used, provides for a harmonic distortion better than 27 dB.

Calculation of the R-filter Coefficients:

$f_{TONE} := 8192 \times INC/f_{MCLK}$ with f_{MCLK}, f_{TONE} [kHz]

$INC := S_{R1} \times 2^{-EXP R1} \times (1 + S_{R2} \times 2^{-EXP R2} \times (1 + S_{R3} \times 2^{-EXP R3} \times (...(...(1 + S_{R9} \times 2^{-EXP R9})...))$

S ... SIGN, EXP ... EXPONENT

$A_1 := INC$

FOR i := 1 TO 9 DO

    FIND S_i, EXP_i: FOR ($|A_i - S_i \times 2^{-EXP i}|$) = MIN; $S_i \in (-1, 1)$, $EXP_i \in (0 ... 7)$

    $A_{i+1} := (A_i / S_i \times 2^{-EXP i}) - 1$

    $R_i := [(-S_i + 1)/2), BIN(EXP_i)]$ (to be transferred to the SICOFI)

NEXT i

Programming Byte Sequence for Selected Frequencies

Coefficients		Frequency Hz										
		2000	1000	800	697	770	852	941	1209	1336	1477	1633
COP write *)		2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB	2B/AB
X	X	00	00	00	00	00	00	00	00	00	00	00
X	X	00	00	00	00	00	00	00	00	00	00	00
X	X	00	00	00	00	00	00	00	00	00	00	00
*R*1	X	00	10	10	20	10	10	10	10	10	10	00
*R*3	*R*2	8F	8F	AA	A1	CA	3B	CC	B2	22	D1	1B
*R*5	*R*4	8F	8F	AA	2B	32	C1	BB	22	A1	C1	5C
*R*7	*R*6	8F	8F	AA	4B	2D	BB	12	5F	5F	BB	CA
*R*9	*R*8	8F	8F	AA	B1	B3	12	DA	8F	1B	12	13

X don't care
*) 2B for SICOFI A, AB for SICOFI B.