T-46-23-12

CYPRESS SEMICONDUCTOR

CY7C182

8,192 x 9 Static R/W RAM

Features

- Fast access time
  - Commercial: 25/35/45 ns (max.)
  - Military: 35/45/55 ns (max.)
- Low power consumption
  - Active: 770 mW (max.)
- 300-mil-width package
- Low standby power
  - 193 mW
- TTL-compatible inputs and outputs
- Asynchronous
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C182 is a high-speed CMOS static RAM organized as 8,192 by 9 bits and it is manufactured using Cypress's high-performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 770 mW.

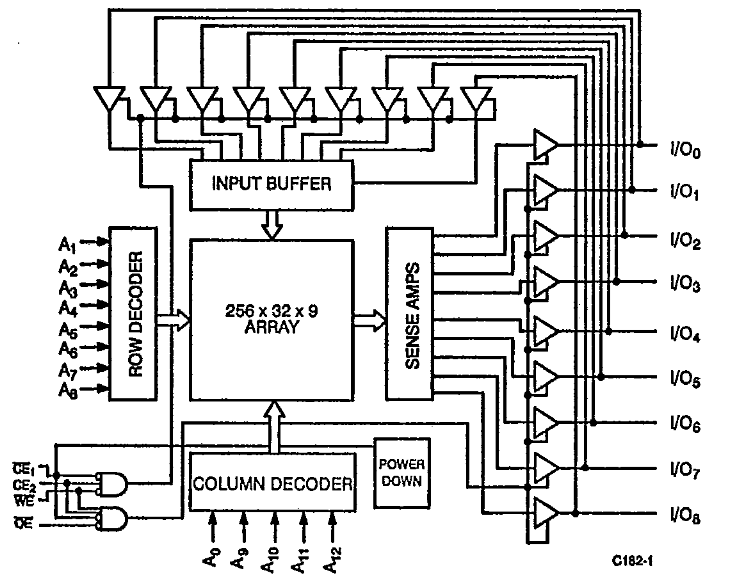
The CY7C182, which is oriented toward cache memory applications, features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by more than 70% when the circuit is deselected. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE_1}$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, data on the nine data input/output pins (I/O_0 through I/O_8) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, ($\overline{CE_1}$ and $\overline{OE}$ active LOW and CE_2 active HIGH), while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the nine data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

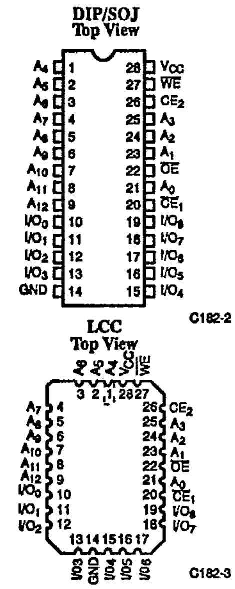
A die coat is used to insure alpha immunity.

Logic Block Diagram



C182-1

Pin Configurations



Selection Guide

		7C182-12	7C182-15	7C182-20	7C182-25	7C182-35	7C182-45	7C182-55
Maximum Access Time (ns)		12	15	20	25	35	45	55
Maximum Operating Current (mA)	Com'l	170	160	150	140	140	140	140
	Mil	180	170	160				
Maximum Standby Current (mA)		40	35	35	35	35	35	35

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to +150°C

Ambient Temperature with Power Applied .... – 55°C to +125°C

Supply Voltage to Ground Potential[1] .... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] .... – 0.5V to +7.0V

DC Input Voltage[1] .... – 0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015.2)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C182–12 Min.	7C182–12 Max.	7C182–15 Min.	7C182–15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} Min., I_{OH} = – 4.0 mA.		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}, GND < V_{OUT} < V_{CC}, Output Disabled		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND		–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			–350		–350	mA
I_{CC}	V_{CC} Operating Circuit Current	V_{CC} Max., Output Current = 0 mA, f = Max., V_{IN} = V_{CC} or GND	Com'l		170		160	mA
			Mil		180		170	
I_{SB1}	Automatic Power-Down Current — TTL Inputs	Max V_{CC}, $\overline{CE_1}$ ≥ V_{IH}, CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		35	mA
I_{SB2}	Automatic Power-Down Current — CMOS Inputs	Max V_{CC}, $\overline{CE_1}$ ≥ V_{CC} – 0.3V, CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0			20		20	mA

Shaded area contains advanced information.

Notes:

1. $V_{IL\,(min.)}$ = – 3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Duration of the short circuit should not exceed 30 seconds. Not more than one output should be shorted at one time.

Electrical Characteristics Over the Operating Range (continued)

Parameters	Description	Test Conditions		7C182−20 Min.	7C182−20 Max.	7C182−25, 35, 45, 55 Min.	7C182−25, 35, 45, 55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} Min., I_{OH} = − 4.0 mA.		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}, GND < V_{OUT} < V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−300	mA
I_{CC}	V_{CC} Operating Circuit Current	V_{CC} Max., Output Current = 0 mA, f = Max., V_{IN} = V_{CC} or GND	Com'l		150		140	mA
			Mil		160		150	
I_{SB1}	Automatic Power-Down Current — TTL Inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			35		35	mA
I_{SB2}	Automatic Power-Down Current — CMOS Inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			20		20	mA

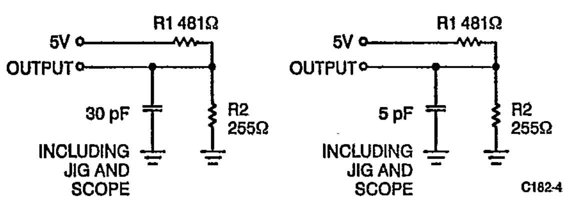
Shaded area contains advanced information.

Capacitance[4]

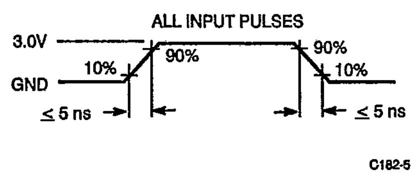
Parameters	Description	Test Conditions	Max.	Units
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{IN}	Input Capacitance		10	pF

Note:
4. Tested initially and after any design or process changes that may affect these parameters.

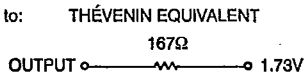
AC Test Loads and Waveforms



(a) (b)



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameters	Description	7C182−12		7C182−15		7C182−20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE[5]								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Address Valid to Low Z	3		3		5		ns
t_{ACE1}	$\overline{CE}_1$ Access Time		12		15		20	ns
t_{ACE2}	CE_2 Access Time		12		15		20	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z	3		3		3		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		ns
t_{HZCE1}	$\overline{CE}_1$ HIGH to High Z[6]		7		8		8	ns
t_{HZCE2}	CE_2 LOW to High Z[6]		7		8		8	
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		12		15		20	ns
t_{DOE}	$\overline{OE}$ Access Time		6		7		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		7		8		8	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SA}	Address Set-Up Time	0		0		0		ns
t_{AW}	Address Valid to End of Write	9		10		15		ns
t_{SD}	Data Set-Up Time	6		7		10		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	8		10		15		ns
t_{SCE2}	CE_2 HIGH to Write End	8		10		15		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		15		ns
t_{HA}	Address Hold from End of Write	0		0		0		ns
t_{HD}	Data Hold Time	0		0		0		ns
t_{LZWE}	Write HIGH to Low Z[8]	3		3		5		ns
t_{HZWE}	Write LOW to High Z[6,8,9]		6		7		7	ns

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Notes:

5. $\overline{WE}$ is HIGH for read cycle.
6. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF. Transition is measured ± 500 mV from steady state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. At any given temperature and voltage condition, t_{LZWE} is less than t_{HZWE} for any given device. These parameters are sampled and not 100% tested.
9. Address valid prior to or coincident with $\overline{CE}$ transition LOW and CE_2 transition HIGH.

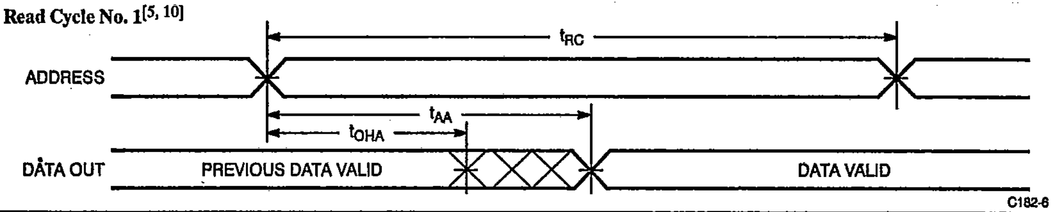
Switching Characteristics Over the Operating Range (continued)

Parameters	Description	7C182-25 Min.	7C182-25 Max.	7C182-35 Min.	7C182-35 Max.	7C182-45 Min.	7C182-45 Max.	7C182-55 Min.	7C182-55 Max.	Units
READ CYCLE[5]										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Address Valid to Low Z	3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ Access Time		25		35		45		55	ns
t_{ACE2}	CE_2 Access Time		25		25		45		55	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z	5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	5		5		5		5		ns
t_{HZCE1}	$\overline{CE}_1$ HIGH to High Z[6]		20		20		25		25	ns
t_{HZCE2}	CE_2 LOW to High Z[6]		20		20		25		25	
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		25		25	ns
t_{DOE}	$\overline{OE}$ Access Time		20		20		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		20		20		25		30	ns
WRITE CYCLE[7]										
t_{WC}	Write Cycle Time	25		35		45		50		ns
t_{SA}	Address Set-Up Time	0		0		0		0		ns
t_{AW}	Address Valid to End of Write	20		30		40		50		ns
t_{SD}	Data Set-Up Time	18		20		25		30		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	20		30		40		50		ns
t_{SCE2}	CE_2 HIGH to Write End	20		30		40		50		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		35		ns
t_{HA}	Address Hold from End of Write	5		5		5		5		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{LZWE}	Write HIGH to Low Z[8]	3		3		3		3		ns
t_{HZWE}	Write LOW to High Z[6, 8, 9]		13		15		20		25	ns

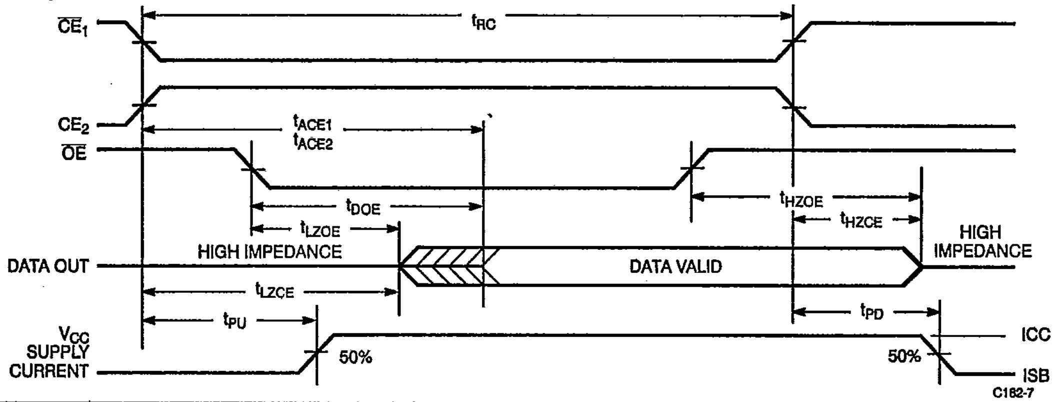
SRAMs 2

Switching Waveforms

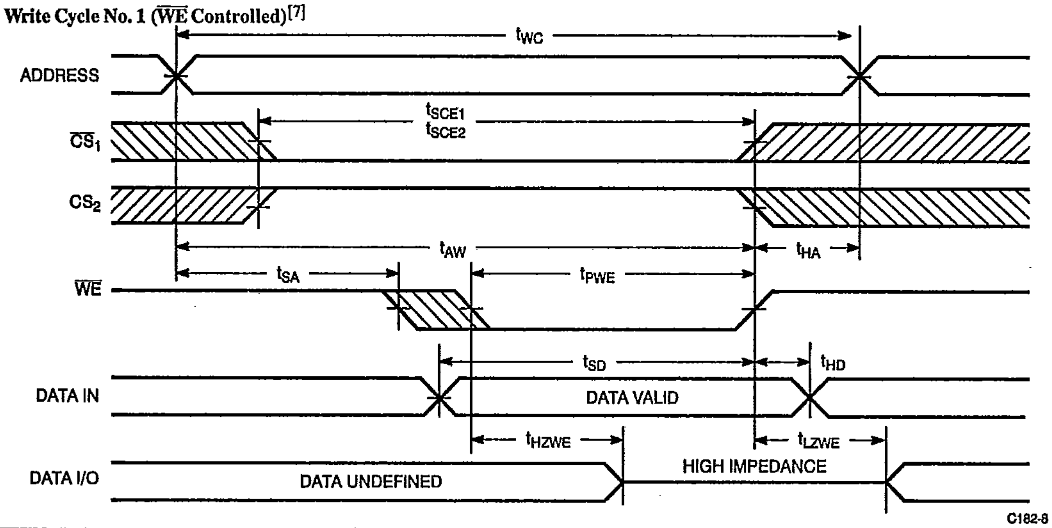
Read Cycle No. 1[5, 10]



Read Cycle No. 2[5, 11]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]

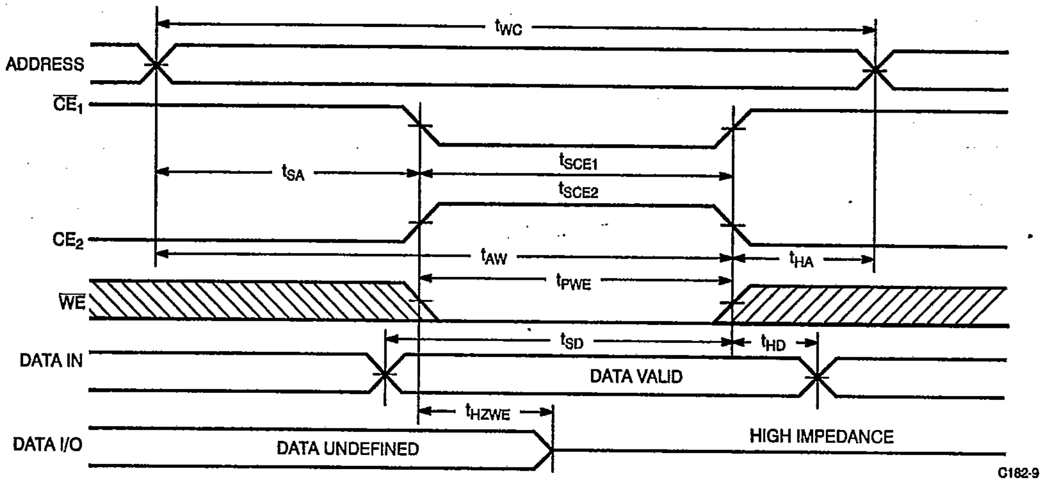


Notes:

10. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}. CE_2 = V_{IH}.
11. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[7, 11]



Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	Data-In	Data-Out	Mode
H	X	X	X	Z	Z	Deselect/Power-Down
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output Disable
X	L	X	X	Z	Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C182−12DC	D22	Commercial
	CY7C182−12PC	P21	
	CY7C182−12VC	V21	
	CY7C182−12DMB	D22	Military
	CY7C182−12LMB	L54	
15	CY7C182−15DC	D22	Commercial
	CY7C182−15PC	P21	
	CY7C182−15VC	V21	
	CY7C182−15DMB	D22	Military
	CY7C182−15LMB	L54	
20	CY7C182−20DC	D22	Commercial
	CY7C182−20PC	P21	
	CY7C182−20VC	V21	
	CY7C182−20DMB	D22	Military
	CY7C182−20LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C182−25DC	D22	Commercial
	CY7C182−25PC	P21	
	CY7C182−25VC	V21	
35	CY7C182−35DC	D22	Commercial
	CY7C182−35PC	P21	
	CY7C182−35VC	V21	
45	CY7C182−45DC	D22	Commercial
	CY7C182−45PC	P21	
	CY7C182−45VC	V21	

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