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1. General Description

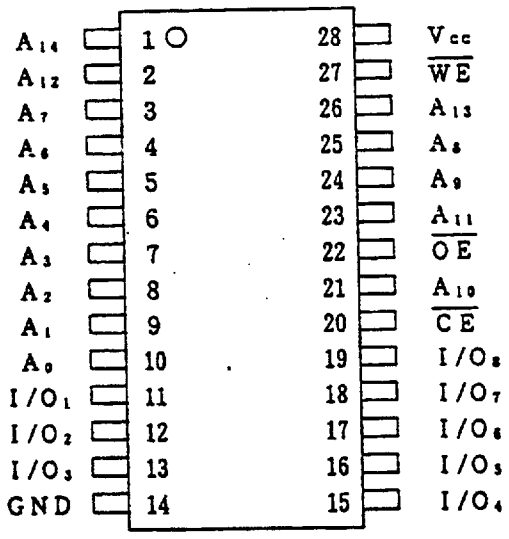
LH52B256HN-90LL is a static RAM organized as 32,768words×8bits fabricated with a CMOS silicon gate process.

Features

○Access time		90ns (Max.)
○Current Consumption Operating		70mA (Max.)
		15mA (t_{RC}, t_{WC}=1μs; typ.)
	Standby	40μA (Max.)
	Data retention	1μA (V_{CCDR}=3V, Ta=25℃)
○Single 5V power supply		5V±10%

○Fully static operation
○All inputs/outputs TTL compatible
○Three-state output
○Not designed or rated as radiation hardened
○28pin SOP (SOP28-P-450) plastic package
○N-type bulk silicon
○Operating temperature is −40℃ to +85℃

2. Pin Configuration



(Top View)

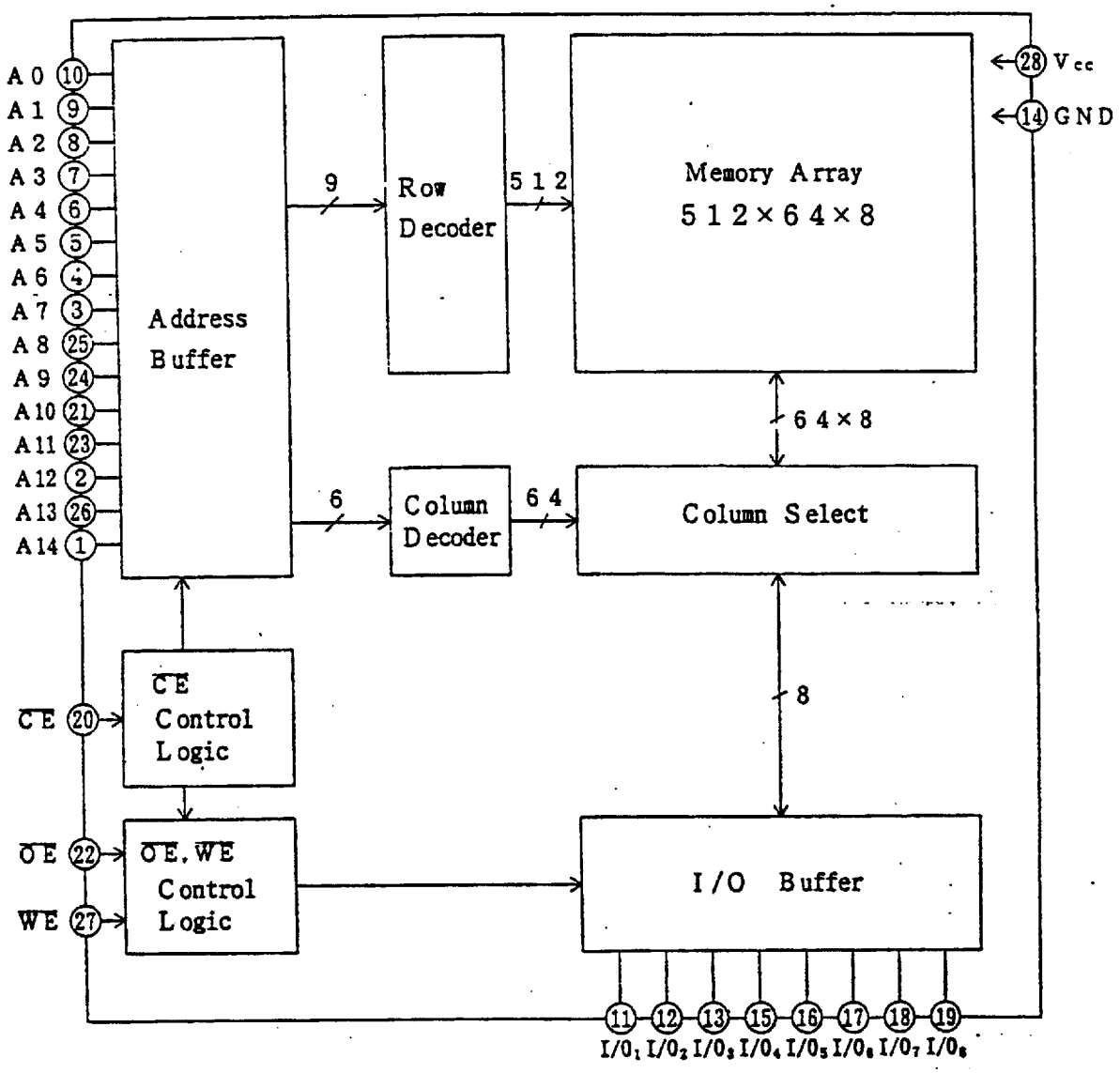
Pin Name	Signal
A_0 to A_{14}	Address inputs
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
I/O_1 to I/O_8	Data inputs/outputs
V_{CC}	Power supply
GND	Ground

3. Operating Mode

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O_1 to I/O_8	Supply current
H	*	*	Standby	High impedance	Standby (I_{SB})
L	L	*	Write	D_{IN}	Operating (I_{CC})
L	H	L	Read	D_{OUT}	Operating (I_{CC})
L	H	H	Output disable	High impedance	Operating (I_{CC})

(* = H or L)

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage(*1)	V_{CC}	−0.5 to +7.0	V
Input voltage (*1)	V_{IN}	−0.5(*2) to V_{CC}+0.5	V
Operating temperature	Topr	−40 to +85	℃
Storage temperature	Tstg	−65 to +150	℃

Note) * 1. Maximum applicable voltage on any pin with respect to GND.
* 2. -3.0V for pulse width≦50ns.

6. Recommended DC Operating Conditions

(Ta=-40℃ to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC}+0.5	V
	V_{IL}	−0.5(*3)		0.8	V

Note) * 3. -3.0V for pulse width≦50ns.

7. DC Electrical Characteristics

(Ta=-40℃ to +85℃, V_{CC}=5V±10%)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	−1		1	μA
Output leakage Current	I_{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=0V to V_{CC}	−1		1	μA
Operating Supply Current	I_{CC}	Minimum Cycle $V_{IN}=V_{IL}$ or V_{IH} $I_{I/O}$=0mA, $\overline{CE}=V_{IL}$			70	mA
		t_{RC}, t_{WC}=1μs $V_{IN}=V_{IL}$ or V_{IH} $I_{I/O}$=0mA, $\overline{CE}=V_{IL}$		15	30	mA
Standby Supply Current	I_{SB}	$\overline{CE}\geqq V_{CC}-0.2V$			40	μA
	I_{SB1}	$\overline{CE}=V_{IH}$			3.0	mA
Output voltage	V_{OL}	I_{OL}=2.1mA			0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4			V

8. Test Conditions of AC Characteristics

Input pulse levels	0.6 to 2.4V
Input rise/fall times	10 ns
Input/output reference levels	1.5V
Output load	1TTL+C_L (100pF) (Including scope and jig capacitance)

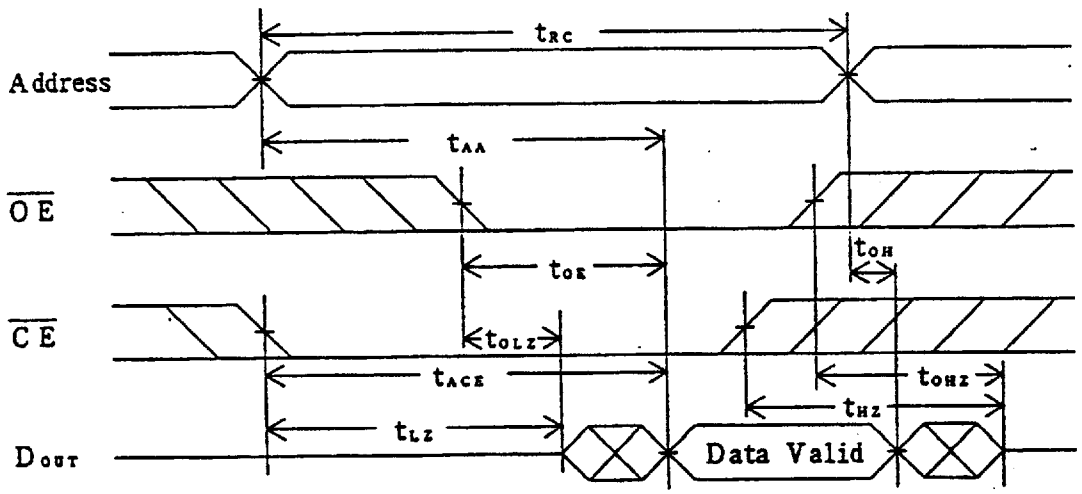
9. AC Characteristics

Read Cycle

(T_a=-40℃ to +85℃, V_{CC}=5V±10%)

Parameter	Symbol	Min.	Max.	Unit	
Read cycle time	t_{RC}	90		ns	
Address access time	t_{AA}		90	ns	
Chip enable access time	t_{ACE}		90	ns	
Output enable access time	t_{OE}		50	ns	
Output hold time	t_{OH}	10		ns	
$\overline{CE}$ Low to output in Low impedance	t_{LZ}	10		ns	*4
$\overline{OE}$ Low to output in Low impedance	t_{OLZ}	5		ns	*4
$\overline{CE}$ High to output in High impedance	t_{HZ}	0	40	ns	*4
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	40	ns	*4

Timing Chart (*5)



Note) *4. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

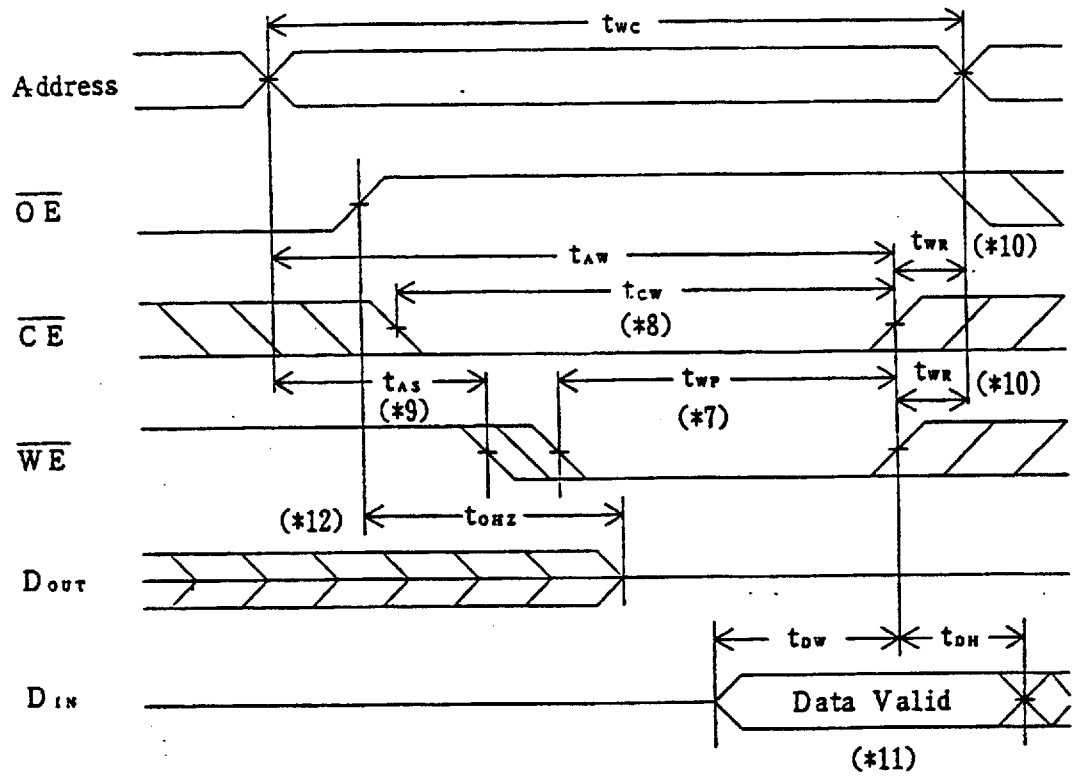
*5. $\overline{WE}$ is 'High' level during the read cycle.

Write Cycle

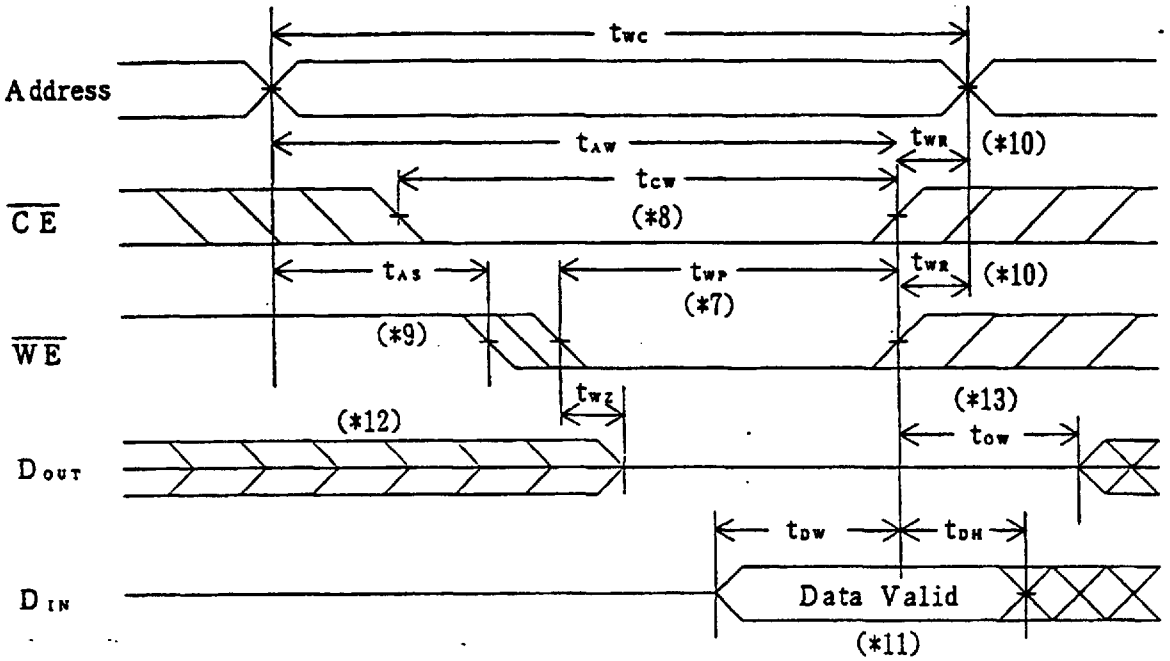
(Ta=-40℃ to +85℃, V_{CC}=5V±10%)

Parameter	Symbol	Min.	Max.	Unit	
Write cycle time	t_{WC}	90		ns	
CE Low to end of write	t_{CW}	70		ns	
Address valid to end of write	t_{AW}	70		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	65		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	35		ns	
Input data hold time	t_{DH}	0		ns	
WE High to output in Low impedance	t_{OW}	5		ns	*6
WE Low to output in High impedance	t_{WZ}	0	40	ns	*6
OE High to output in High impedance	t_{OHZ}	0	40	ns	*6

Timing Chart ($\overline{OE}$ Controlled)



Timing Chart ($\overline{OE}$ Low fixed)



Note) * 6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

* 7. The writing occurs during a overlapping period of $\overline{CE}$ = 'Low', and $\overline{WE}$ = 'Low' (t_{WP}).

* 8. t_{CW} is defined as the time from $\overline{CE}$ Low transition to the end of writing.

* 9. t_{AS} is defined as the time from address change to the start of writing.

*10. t_{WR} is defined as the time from the end of writing to address change.

*11. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

*12. If $\overline{CE}$ Low transition occurs at the same time or after $\overline{WE}$ Low transition, the outputs will remain High impedance.

*13. If $\overline{CE}$ High transition occurs at the same time or before $\overline{WE}$ High transition, the outputs will remain High impedance.

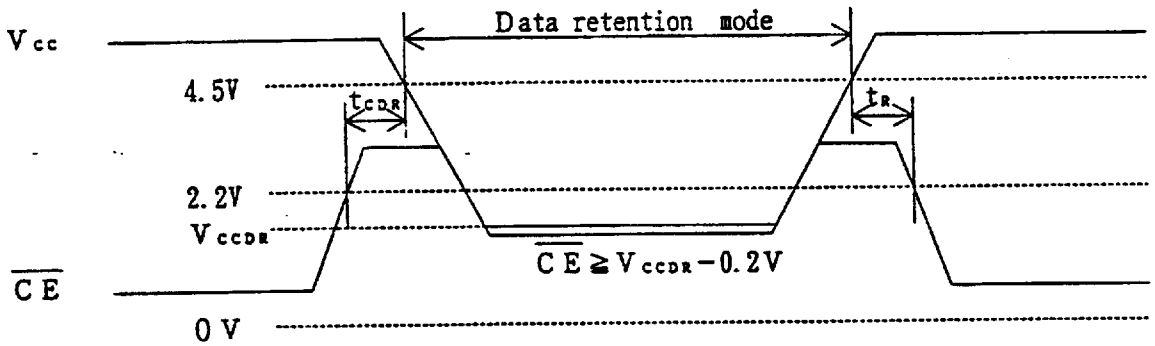
10. Low Voltage Data Retention Characteristics

(Ta=-40℃ to +85℃)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	
Data retention supply voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR} - 0.2V$		2		5.5	V	
Data retention supply current	I_{CCDR}	$V_{CCDR} = 3.0V$	Ta=25℃			1	μA	
			Ta=0℃~+40℃			3	μA	
		$\overline{CE} \geq V_{CCDR} - 0.2V$				20	μA	
Chip enable setup time	t_{CDR}			0			ns	
Chip enable hold time	t_R			(*14) t_{RC}			ns	

Note) *14. Read cycle time.

Timing Chart



11. Pin Capacitance

(Ta=25℃, f=1MHz)

Parameter	Symbol	Conditio n	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	$V_{IN} = 0V$			9	pF	*15
I/0 capacitance	$C_{I/O}$	$V_{I/O} = 0V$			10	pF	*15

Note) *15. This parameter is sampled and not 100% tested.

12 Package and packing specification

1. Package Outline Specification

Refer to drawing No. AA931

2. Markings

2－1. Marking contents

(1) Product name : LH52B256HN－90LL

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×××

- YY → Denotes the production year. (Lower two digits of the year.)
- WW → Denotes the production week. (01,02,03,・・・・・52,53)
- ××× → Denotes the production ref.code (1~3)

Indicates the product was manufactured in the WWth week of 19YY.

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer to drawing No. AA931

(This layout do not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip,lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3－1. Packing Materials

Material Name	Material Specificaiton	Purpose
Magazine	Anti-static treated plastic (25devices/magazine)	Packing of device
Stopper	Plastic or rubber	Fixing of device
Cap	Plastic (2caps/bag)	Fixing of Magazine
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
Inner case	Card board (1000devices/case)	Packaging of device
Label	Paper	Indicates part number,quantity and date of manufacture
Outer case	Card board	Outer packing of Magazine

(Devices shall be inserted into a magazine (sleeve) in the same direction.)

ISSUE DATE	'94.08.25	T. Maeda	Y. Tohdo	M. Uchida	(NOTE)
ISSUE NUMBER	H40825-09				(DOCUMENT No. 931-SDE)
S/C NUMBER	LH52B5HN				

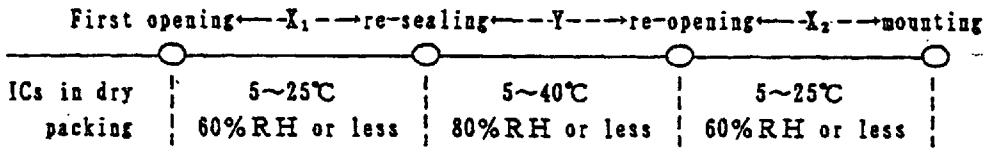
3－2. Outline dimension of magazine (sleeve)
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The magazine has been treated to be conductive or anti-static. If the device is transferred to another magazine, use a equivalent magazine.
(3) A stopper is included with the magazine. Before storage, make sure the stopper is inserted.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 4 days after opening dry packing.
(2) To re-store the ICs for an extended period of time within 4 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whoes indicater is blue), and store in an environment with a temperature of 5～40℃ and a relative humidity of 80% or less, and mount ICs within 2 weeks.
(3) Total period of storage after first opening and re-opening is within 4 days, and store the ICs in the same environment as section 4-3.(1).



$X_1 + X_2$: within 4 days
Y : within 2 weeks

4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16～24 hours at 120℃ or 5～10 hours at 150℃. Note that the standard magazine can not be baked. Use the heat resistant magazine.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 4-3.(1).

5. Surface Mount Conditions

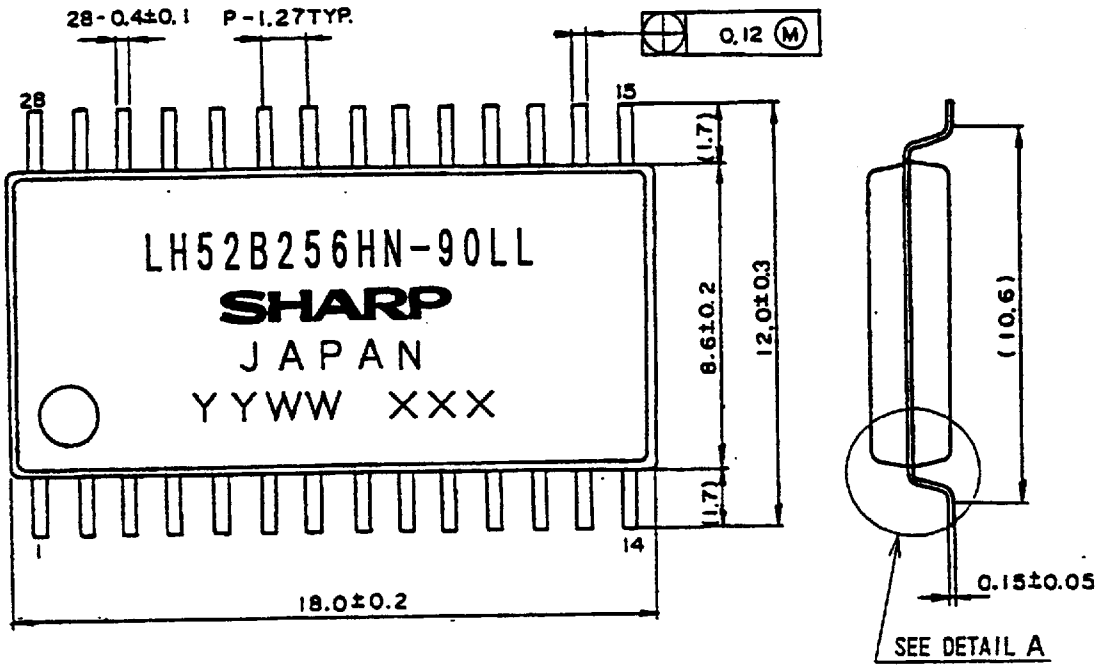
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

5－1. Soldering conditions (The following conditions are valid only for one time soldering.)

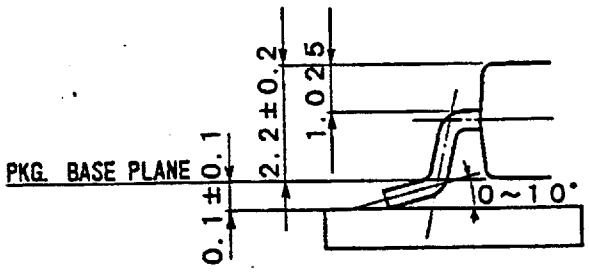
Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 240℃, duration less than 15 seconds above 230℃, temperature increase rate of 1～4℃/second	IC surface
Solder dipping	245℃ or less, duration less than 3 seconds/dip, total of 5 seconds	Solder bath
Vapor phase solderring	215℃ or less, duration less than 40 seconds above 200℃	Steam
Manual soldering (soldering iron)	260℃ or less, duration less than 10 seconds	IC outer lead surface

5－2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃

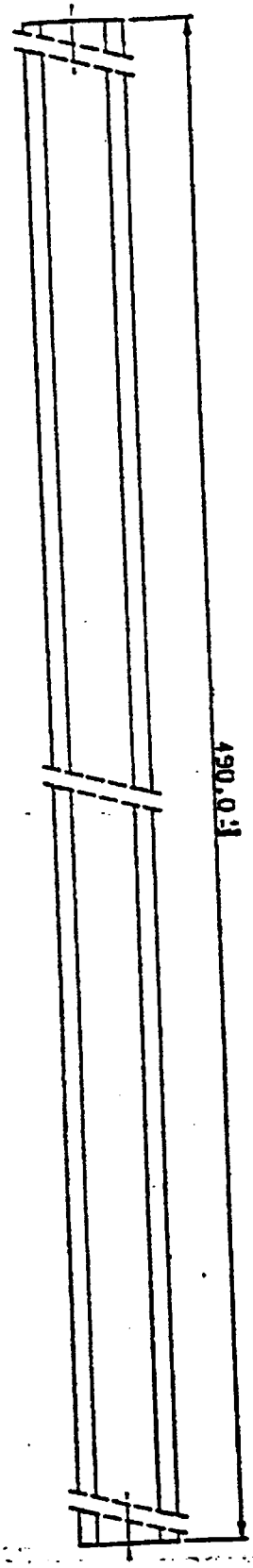


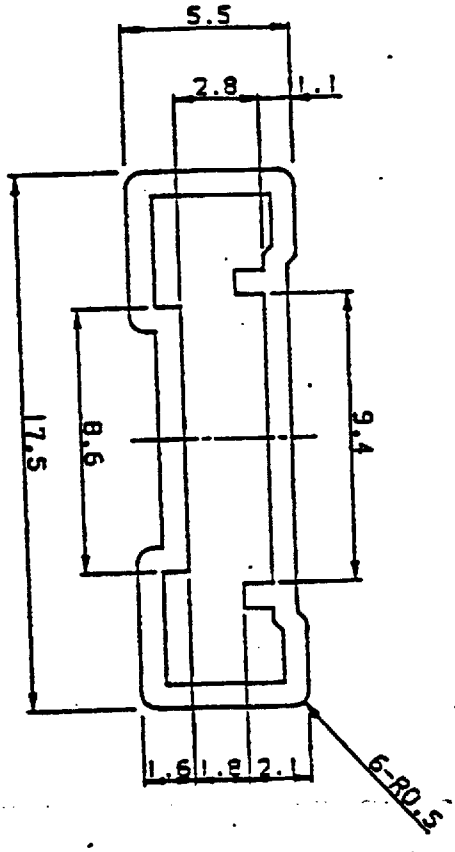
DETAIL A



名称 NAME	SOP28-P-450	リード仕上 LEAD FINISH	TIN-LEAD PLATING	単位 UNIT	mm
シャープ株式会社 SHARP CORP.	IC事業本部 IC GROUP		DRAWING NO.	AA931	

備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。
NOTE Plastic body dimensions do not include burr of resin.





注記 ：マガジン(スリーブ)両側のストッパーは、ゴムストッパーとする。
指示無き寸法公差は全て±０．４ｍｍとする。

NOTES : Stopper which is set at the both ends of magazine (sleeve) is made of rubber.
All tolerances are ±0.4mm unless otherwise specified.

名称 NAME	SOP28SPN-A2	単位 UNIT	mm
シャープ株式会社 IC事業本部 SHARP CORP. IC GROUP		DRAWING NO.	CV607
備考 NOTE			