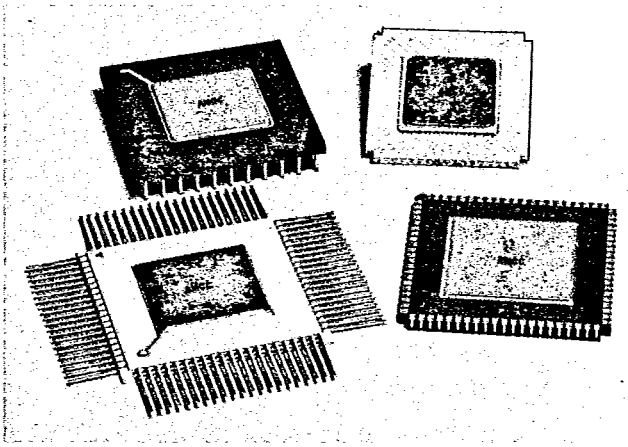
DEVICE SPECIFICATION

APPLIED MICRO CIRCUITS CORPORATION

Q1500 SERIES LOGIC ARRAYS



FEATURES

TWO ARRAY SIZES
1500 and 1700 equivalent gate densities are available in the Q1500A and QH1500A respectively.

UP TO 120 I/O CAPABILITY
The QH1500A supports up to 60 inputs and 60 I/Os. The Q1500A supports up to 46 inputs and 38 outputs.

VERY HIGH SPEED
0.5 to 0.9 ns average gate delay for complex circuits.

ECL & TTL COMPATIBLE
The Q1500 series logic arrays are compatible with ECL, TTL or simultaneous ECL/TTL systems, in both single and multiple power supply configurations. This flexible I/O structure eliminates the need for ECL/TTL and TTL/ECL translation logic in high performance applications.

MODERATE POWER
The Q1500 series devices offer the advantage of low power ECL coupled with a very flexible I/O structure.

FULL MILITARY AVAILABILITY
These logic arrays are available for applications requiring MIL-STD-883C class B screening including burn-in, and will operate over the military temperature range of −55° to +125°C.

RADIATION HARD TECHNOLOGY
This series features a washed emitter ECL process which is one of the most radiation tolerant technologies in production.

DESCRIPTION

The AMCC Q1500 Series consists of the Q1500A and QH1500A logic arrays providing equivalent densities of up to 1500 and 1700 gates respectively. The series is optimized to provide a system approach to high performance semicustom applications. High speed ECL logic and proven reliability are combined with an advanced, interactive CAD system to provide a quick and cost-effective solution to discrete I.C. replacement.

Each device shares a common Internal Logic and MSI macro library. The Q1500 series arrays utilize advanced series gating techniques providing both density and speed improvements over gate oriented and other macro-oriented designs.

The Q1500 logic arrays offer a wide range of standard packages and support both 84 and 120 I/O signal requirements.

PERFORMANCE SUMMARY	
PARAMETER	**VALUE**
Equivalent gate delay* (typical)	0.5 to 0.9 ns
Maximum input frequency	125 MHZ
Maximum output frequency	100 MHZ
TTL output drive	20 mA
ECL output driver load	50 Ω
Average cell utilization	95%
*Based on complex macro functions	

TABLE 1

RESOURCE SUMMARY		
DESCRIPTION	**Q1500A**	**QH1500A**
Equivalent gate complexity	1500	1700
Internal logic cells	128	136
Input cells	46	60
Output cells	38	—
I/O cells	—	60
Typical power dissipation per internal cell in mW	5-12	5-12
Typical total circuit power dissipation in watts @ 95% utilization	2.6	2.9

TABLE 2

Q1500 SERIES DIE LAYOUTS

Q1500A – Die Size 269 mils x 257 mils

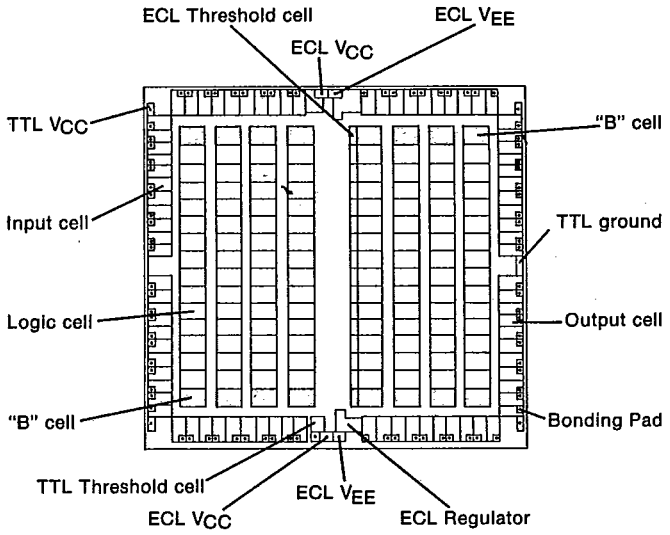


FIGURE 1

QH1500A – Die Size 312 mils x 300 mils

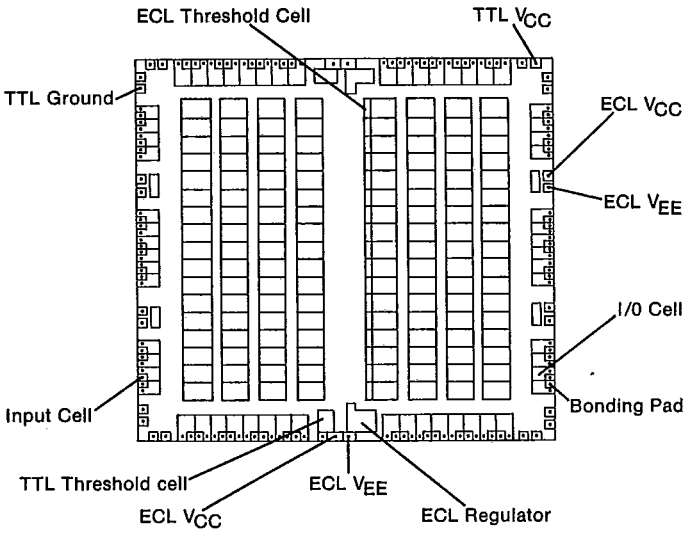


FIGURE 2

ARRAY ARCHITECTURE

The Q1500 series logic arrays have an internal structure comprised of configurable cells plus features, such as voltage references, bias generators and voltage regulators. The user configurable Q1500A cells consist of Internal Logic (L) and Buffered Logic (B) cells in the internal array, with Input (I) and Output (O) cells on the array perimeter. The QH1500A has Internal Logic (L) cells in the internal array, with Input (I) and Input/Output (I/O) cells on the array perimeter.

INTERNAL CELLS

There are 128 internal logic cell positions for the Q1500A and 136 cells for the QH1500A. B cells are used on the Q1500A only, and occupy the top and bottom rows in the internal array. Internal logic macros can be placed in either an L or B cell, while ECL output buffer macros can only be placed in a B cell. In the QH1500A, the ECL output buffers are placed in the I/O cells, providing additional logic capability in the internal array.

Macro placement is performed automatically by using the AMCC CAD software. If a circuit requires critical timing considerations, these macros may be preplaced through an interactive graphics terminal.

CIRCUIT I/O

The interface to the array is accomplished in the Input (I) cells and the Output (O) or Input/Output (I/O) cells. Input and output cells can be configured for input and output functions respectively, while I/O cells can be configured as either inputs, outputs, or bi-directional I/O. All output and bi-directional I/O functions on a QH1500A are performed in the I/O cells. Bi-directional I/O is obtained in a Q1500A by using one input cell and one output cell as an I/O pair.

Additionally, the I/O of the Q1500 series can be configured to provide ECL input, output or ECL I/O referenced either to a −5.2V or +5.0V power supply.

Table 4 lists the available I/O resources for the Q1500 series logic arrays. Each logic array requires different quantities of power supply connections depending on the mode of operation.

INTERNAL ARRAY CELL RESOURCE SUMMARY

	Q1500A	QH1500A
L Cells	112	136
B Cells	16	–
Total	128	136

TABLE 3

I/O RESOURCES

MODE	DESCRIPTION	Q1500A	QH1500A	
TTL SYSTEMS	Input Cells (Max)	46	60	MAX
	I/O Cells (Max)	–	60	MAX
	Output Cells (Max)	38	–	MAX
	V_{CC} (+5 V_{DC} nom.)	6	14	
	Ground	4	14	
ECL SYSTEMS	Input Cells (Max)	46	60	MAX
	I/O Cells (Max)	–	60	MAX
	Output Cells (Max)	38	–	MAX
	V_{EE} (−5.2 V_{DC} nom.)	2	6	
	Ground	8	22	
MIXED TTL/ECL SYSTEMS	Input Cells (Max ECL or TTL)	46	59	MAX
	I/O Cells (Max ECL or TTL)	–	60	MAX
	Output Cells (Max)	38	–	MAX
	V_{CC} (+5V V_{DC} nom.)	5	6	
	V_{EE} (−5.2 V_{DC} nom.)	2	6	
	Ground	4	16	
MIXED +5V SYSTEM	Input cells	46	60	MAX
	I/O cells	--	60	MAX
	Output cells	38	--	MAX
	V_{CC}	6	12	
	V_{EE}	--	--	
	Ground	4	16	

TABLE 4

INTERNAL LOGIC CELLS

INTERNAL LOGIC CELL CAPABILITIES

Each of the Q1500 series devices have similar internal logic cell structures.

These logic cells are positioned in uniform columns across the arrays and contain 60 uncommitted transistors and resistors. Each cell is individually configurable to provide a variety of logic functions through the use of the Q1500 series internal logic macro library. As shown in Figure 3, the internal logic macro library provides for both SSI and the more basic MSI functions. MSI functions are available for the more frequently used complex logic functions (adders, counters, shift registers, parity generators, etc.) These MSI logic macros uniquely interconnect a larger number of transistor and resistor components than contained in a single cell. This higher level of integration provides the advantages of higher speed, lower power, and higher circuit density over a standard macro implementation.

TYPICAL MACROS

Illustrated in Figures 4 and 5 are typical examples of macros found in the INTERNAL LOGIC macro library. Each of the INTERNAL LOGIC MACROS occupy up to one internal logic cell location and have the performance and power specified. AMCC provides a large variety of INTERNAL LOGIC MACROS in the library which are organized much like circuits in a TTL or ECL logic catalog. Additionally, the MSI LOGIC MACROS are available for frequently required high level logic functions.

HIGH SPEED MACROS

A high speed option is available on many of the macros in the Q1500 series library. These high speed macros can be used to decrease the propagation delay of critical logic paths; yielding a higher performance circuit with only a minimal increase in overall power consumption.

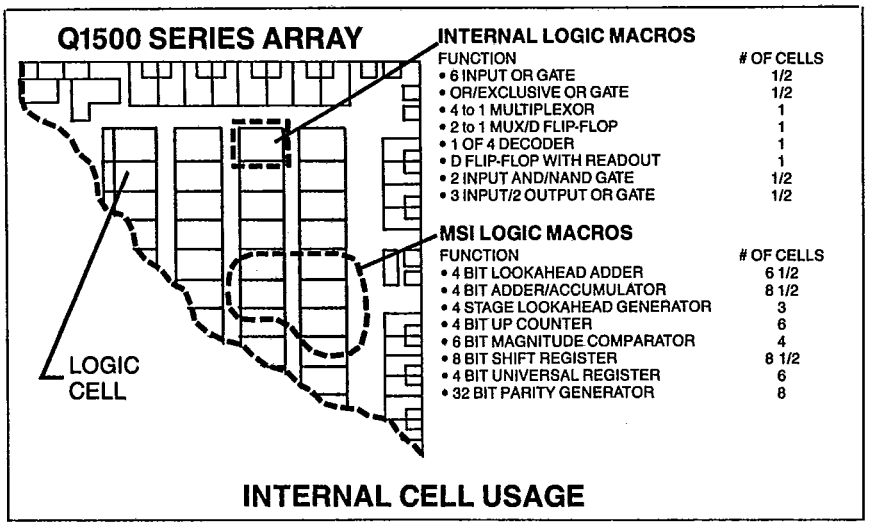


FIGURE 3

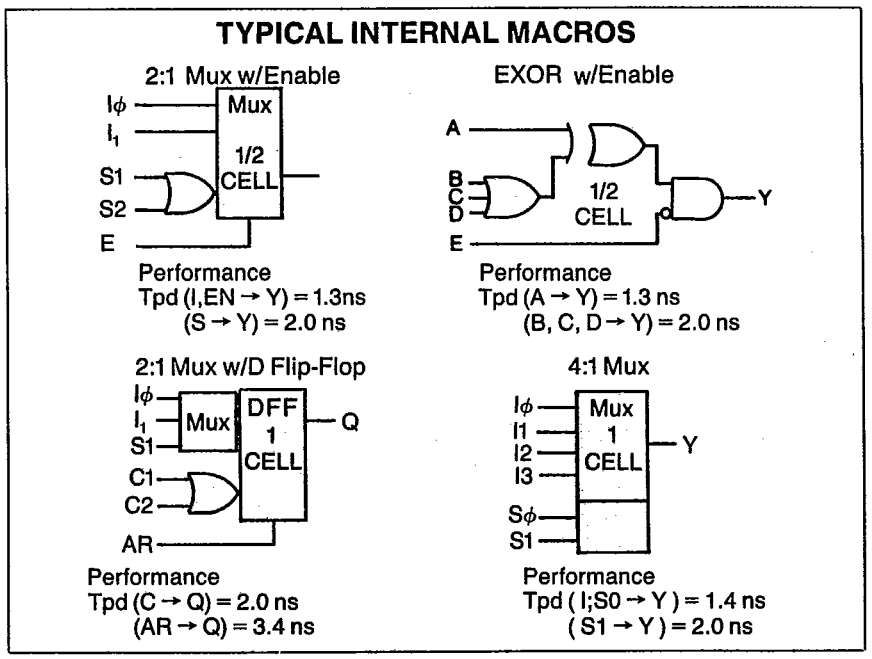


FIGURE 4

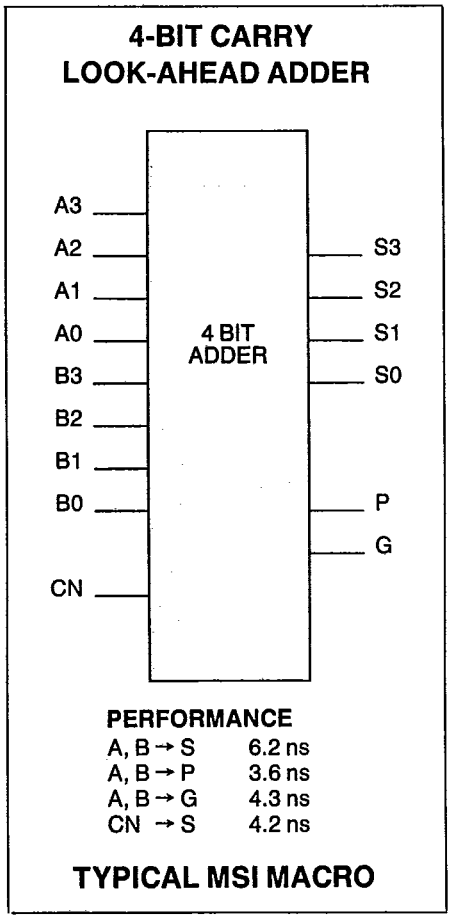


FIGURE 5

INPUT CELLS – Q1500A/QH1500A

Input (I) cells are individually configurable and provide for TTL and ECL inputs. The Q1500A supports ECL 10K I/O, while the QH1500A supports both ECL 10K and ECL 100K I/O.

The following input configurations are supported:

TTL
ECL 10K
ECL 100K (QH1500A only)
TTL 3-state enable driver

OUTPUT CELLS – Q1500A ONLY

Output (O) cells are individually configurable and provide for inputs and 3-state enable drivers as well as TTL and ECL 10K outputs. Output cells configured as 3-state enable drivers can be used with either internal or external control signals and can drive up to eight 3-state enable loads.

The following output cell configurations are supported:

TTL totem pole
TTL 3-state
TTL open collector
TTL 3-state enable driver
ECL 10K (50,100 or 200 ohm drive)

INPUT/OUTPUT CELLS – QH1500A ONLY

The QH1500A output structure provides additional flexibility by replacing the O cells with Input/Output (I/O) cells. Each I/O cell is individually configurable as TTL, ECL 10K, or ECL 100K, and provides for inputs, outputs or bi-directional I/O.

The following I/O cell configurations are supported:

INPUT
TTL
ECL 10K
ECL 100K
TTL 3-state enable driver

OUTPUT
TTL totem pole
TTL 3-state
TTL open collector
ECL 10K
ECL 100K

BI-DIRECTIONAL
TTL transceiver
ECL 10K transceiver
ECL 100K transceiver

HIGH PERFORMANCE INTERFACE OPTIONS

The Q1500 series offers the following high performance interface options:

High speed options on TTL interface
Differential ECL I/O
10124/10125 ECL/TTL translation capability
+5V only ECL and ECL/TTL

The mixed ECL/TTL capabilities allow the use of both technologies in a single design without the use of external translators.

The +5V only ECL allows partitioning of a high speed TTL design into multiple AMCC devices using a single +5V supply, while providing high speed ECL I/O between arrays, and full system TTL compatibility.

DESIGN INTERFACE

The AMCC design interface has been structured to be highly flexible with respect to the customer's level of involvement. AMCC has developed a comprehensive set of CAD tools providing an easy to understand, user-friendly interface.

AMCC CAD TOOLS

- Schematic capture
- Logic simulation
- Test vector generation with optional fault grading
- Auto place and route
- Timing verifier
- Design rule and interconnect verifier

These CAD tools provide the logic designer with the required support to design and develop a logic array from schematic diagrams through complete layout.

AMCC PROVIDED SERVICES

In addition to providing the required CAD capability to allow customer design of arrays, AMCC provides a number of services to support customer design.

- Logic conversion to AMCC macros
- Logic simulation with customer provided simulation vectors
- Custom macro development
- High-level engineering support
- Comprehensive training courses

PACKAGING

The Q1500 series logic arrays can be packaged in a variety of dual in-line, leaded and leadless chip carriers, and pin grid packages.

PACKAGES

Pin Count	Type	Q1500A	QH1500A
48	SDIP	●	
68	LCC	●	
84	LDCC	●	●
	PGA	●	●
100	LDCC	●	●
	PGA	●	●
148	LDCC		●
	PGA		●

TABLE 5

LDCC—Leaded Chip Carrier PGA—Pin Grid Array
LCC—Leadless Chip Carrier SDIP–Side Brazed DIP

Q1500 SERIES ECL MODE OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage (V_{EE}) V_{CC} = 0	−4.7	−5.2	−5.7	V
Input Signal Rise/Fall Time		2.0	2.2	nS
Junction Temperature T_J Military Commercial			 150 130	 °C °C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{EE}) V_{CC} = 0	−8.0 V DC
Input Voltage V_{CC} = 0	GND to V_{EE}
Output Source Current Continuous	−50 mA DC
Operating Temperature	−55°C (Ambient) to +125°C (Case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	−65°C to +150°C

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS V_{EE} = −5.2V[1]

	$T_{ambient}$				T_{case}	
	−55°C	0°C	25°C	75°C	125°C	UNIT
$V_{OH\,max}$	V_{CC}–850	V_{CC}–770	V_{CC}–730	V_{CC}–650	V_{CC}–575	mV
$V_{IH\,max}$	V_{CC}–800	V_{CC}–720	V_{CC}–680	V_{CC}–600	V_{CC}–525	mV
$V_{OH\,min}$	V_{CC}–1080	V_{CC}–1000	V_{CC}–980	V_{CC}–920	V_{CC}–850	mV
$V_{IH\,min}$	V_{CC}–1255	V_{CC}–1145	V_{CC}–1105	V_{CC}–1045	V_{CC}–1000	mV
$V_{IL\,max}$	V_{CC}–1510	V_{CC}–1490	V_{CC}–1475	V_{CC}–1450	V_{CC}–1400	mV
$V_{OL\,max}$	V_{CC}–1655	V_{CC}–1625	V_{CC}–1620	V_{CC}–1585	V_{CC}–1545	mV
$V_{OL\,min}$	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	mV
$V_{IL\,min}$	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	mV
I_{in} H max[2]	30	30	30	30	30	µA
I_{in} L min[2]	.5	.5	.5	.5	.5	µA

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS V_{EE} = -4.5V[3]

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM -0°/+70°C			MIL-55°/+125°C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output Voltage HIGH	Loading is 50Ohms to -2V	V_{CC}-1035		V_{CC}-850	V_{CC}-1080		V_{CC}-835	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to -2V	V_{CC}-1830		V_{CC}-1605	V_{CC}-1880		V_{CC}-1595	mV
$V_{IH\,min}$	Input Voltage HIGH	Maximum input voltage HIGH	V_{CC}-1145		V_{CC}-800	V_{CC}-1145		V_{CC}-800	mV
$V_{IL\,max}$	Input Voltage LOW	Maximum input voltage LOW	V_{CC}-1950		V_{CC}-1475	V_{CC}-1950		V_{CC}-1475	mV
I_{INL}[2]	Input Current	V_{IN} = I_{LMIN}	0.5			0.5			µA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	COMM 0°C/+70°C			MIL-55° C/+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{IPD}	Input Propagation Delay				0.3			0.3		nS
t_{OPD}	Output Propagation Delay, Including Buffer		5 pf, 50Ω to −2V		2.1			2.1		nS
t_{FPD}	Internal Equivalent Gate Delay 5	Standard			0.9			0.9		nS
		High Speed			0.8			0.8		nS

NOTES:
1 Data measured at thermal equilibrium. For +5V ref. ECL, V_{CC} = +5.0V
2 Per fan-in
3 For military temperature range applications V_{EE} minimum is −4.5V. For +5V ref. ECL, V_{CC} = +5.0V
4 Logic cell delays are for each gating level of a more complex logic function (i.e. D flip/flop, 4 to 1 mux, etc.)
5 Package selection will determine the maximum input frequency. Consult AMCC
6 Propagation delays will vary with application. Consult AMCC Q1500 Series Design Guide

Q1500 SERIES TTL MODE OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC})				
Military	4.5	5.0	5.5	V
Commercial	4.75	5.0	5.25	V
Output Current Low (IOL)				
Military			20	mA
Commercial			20	mA
Operating Temperature				
Military	-55 (ambient)		+125 (case)	°C
Commercial	0 (ambient)		70 (ambient)	°C
Junction Temperature T_J				
Military			150	°C
Commercial			130	°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	7.0V
Input Voltage	5.5V
Operating Temperature	−55°C (Ambient) to +125°C (Case)
Junction Temperature (Operating)	150°C
Storage Temperature	−65°C to +150°C

INPUT/OUTPUT DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMM 0°/+70°C			MIL-55°/+125°C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}[2]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			2.0			V
V_{IL}[2]	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = −18mA		−.65	−1.2		−.65	−1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = −1mA	2.7	3.4		2.4	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 4mA			0.4			0.4	V
		V_{CC} = Min, I_{OL} = 20 mA			0.5			0.5	V
I_{OZH}	Output "off" current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V	-50		50	-50		50	μA
I_{OZL}	Output "off" current LOW (3-state)	V_{CC} = Max, V_{OUT} = 0.4V	-50		50	-50		50	μA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V			50			50	μA
I_I	Input HIGH current at Max input voltage	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
I_{IL}	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V			−0.4			−0.4	mA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = OV	−25		−100	−25		−100	mA
I_{CC}[3]	Supply current Q1500 A	V_{CC} = Max, 95% utilization		525			525		mA
	Supply current QH1500 A	V_{CC} = Max, 95% utilization		585			585		mA

NOTES

1 Typical limits are at 25°C, V_{CC} = 5.0V

2a These input levels provide zero noise immunity and should only be tested in a static, noise-free environment

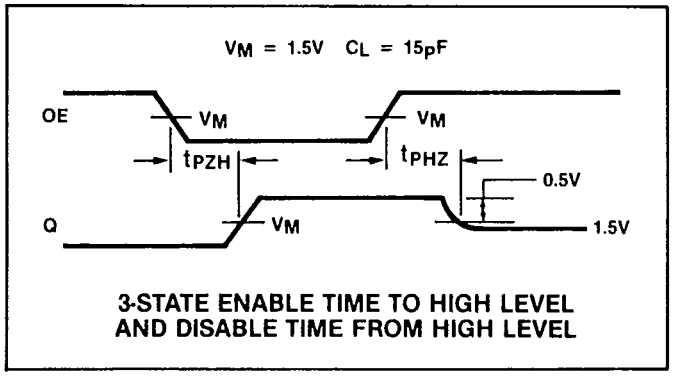
2b Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests

3. Maximum power supply currents vary with each circuit design implemented and can only be determined after macro level circuit designs are complete

Q1500 SERIES TTL MODE OPERATING CONDITIONS

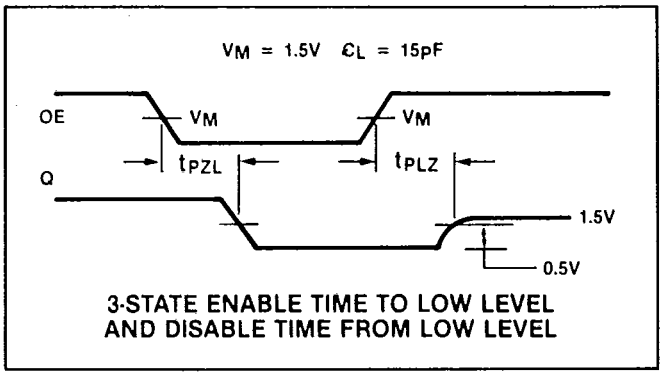
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	COMM 0°/+70°C			MIL 55°/+125°C			UNIT
				Min	Typ	Max	Min	Typ	Max	
t_{IPD}	Input propagation delay through input buffer	Standard	Low to high transition		2.9			2.9		nS
		High Speed	Low to high transition		2.3			2.3		nS
t_{IPD}	Input propagation delay through input buffer	Standard	High to low transition		1.8			1.8		nS
		High Speed	High to low transition		1.7			1.7		nS
t_{OPD}	Output Propagation delay (O cell)	Standard	R_L = 280Ω, C_L = 15 pF		6.6			6.6		nS
		High Speed	Load[2]		4.5			4.5		nS
t_{FPD}[1]	Internal Equivalent Gate Delay	Standard			0.9			0.9		nS
		High Speed			0.8			0.8		nS
t_{PZH}	Enable time to high level		Figure 3 3-state output		7.0			7.0		nS
t_{PZL}	Enable time to low level		Figure 2 3-state output		10.0			10.0		nS
t_{PHZ}	Disable time from high level		Figure 2 3-state output		8.0			8.0		nS
t_{PLZ}	Disable time from low level		Figure 3 3-state output		11.0			11.0		nS



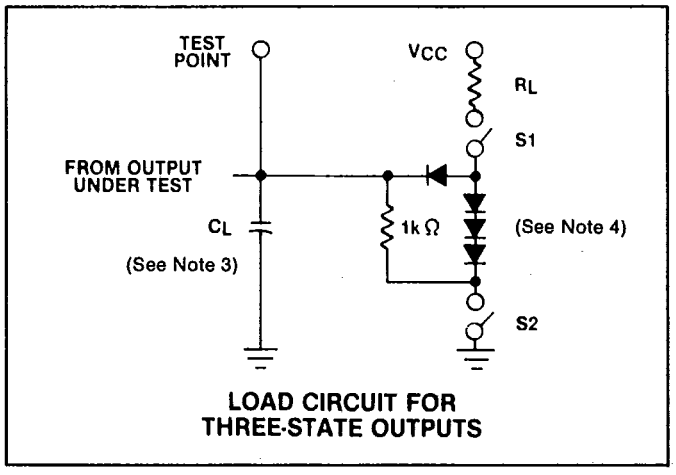
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL

FIGURE 2



3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

FIGURE 3



LOAD CIRCUIT FOR THREE-STATE OUTPUTS

FIGURE 4

TEST CIRCUIT SWITCH TABLE

TEST FUNCTIONS	S1	S2
tp_{ZH}	Open	Closed
tp_{ZL}	Closed	Open
tp_{HZ}	Closed	Closed
tp_{LZ}	Closed	Closed

NOTES:

1. Logic cell delays are for each gate level of a more complex logic function (i.e. D flip/flop, 4 to 1 mux, etc.)
2. Standard TTL load circuit used, see Figure 4 (S1 & S2 closed)
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or 1N3064.
5. Propagation delays will vary with application, consult AMCC Q1500 Series Design Guide.

REPRESENTED BY:

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