F2732
32K (4K x 8)
UV Erasable PROM

MOS Memory Products

Description

The F2732 is a 32,768-bit ultraviolet light Erasable and electrically Programmable Read Only Memory (EPROM) manufactured using the Isoplanar n-channel silicon gate technology. Organized 4096 X 8, the F2732 is ideally suited for non-volatile data storage in applications such as 8-bit microprocessor systems, where reprogrammability, high bit-density, maximum performance, and simple interfacing are essential parameters. All inputs and outputs are TTL-compatible. The 3-state outputs become high impedance when the F2732 is deselected, allowing a direct interface capability which is useful in many computer bus structures.

The F2732 operates from a single standard +5 V power supply during reading, making it compatible with the latest generations of microprocessors.

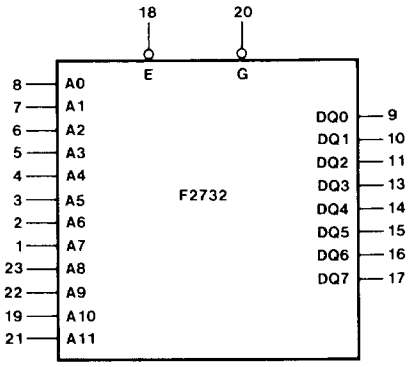
The F2732 programming technique is the simplest available. All data and address inputs are at TTL levels during programming. A +25 V power supply is connected to the $\overline{G}$/VPP pin and only those addresses to be programmed need be selected; therefore total programming time is short and field corrections straight forward. The technique is compatible with board-level programming making large systems simple to program.

- **4096 x 8-BIT ORGANIZATION**
- **FAST ACCESS TIME—450 ns MAX**
- **TTL-COMPATIBLE INPUTS AND OUTPUTS**
- **3-STATE OUTPUTS FOR WIRED-OR CAPABILITY**
- **SINGLE +5 V POWER SUPPLY FOR READ OPERATION**
- **REDUCED POWER STANDBY MODE**
- **SIMPLEST, FASTEST EPROM PROGRAMMING TECHNIQUE AVAILABLE**
- **OUTPUT ENABLE CONTROL FOR MEMORY EXPANSION**
- **STATIC OPERATION**
- **PIN COMPATIBLE WITH 32K AND 64K ROMs FOR LOW COST PRODUCTION**
- **LOW POWER DURING PROGRAMMING**
- **CONTENTS ERASABLE WITH ULTRAVIOLET LIGHT**

Pin Names

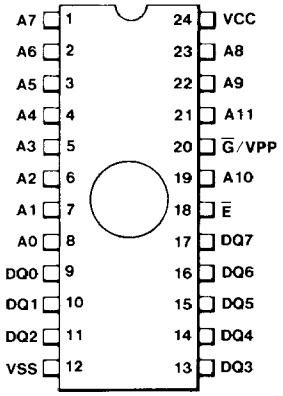
A0-A11	Address Inputs
$\overline{E}$	Chip Enable (Power Down) Input
$\overline{G}$/VPP	Output Enable/+25 V Program Input
DQ0-DQ7	Data Output/Programming Inputs
VCC	+5 V Supply
VSS	Ground

Logic Symbol



VCC = Pin 24
VPP = Pin 20
VSS = Pin 12

Connection Diagram
24-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	7W	D

Absolute Maximum Ratings

VCC Supply Voltage	−0.3 V to +6 V
Any Input or Output	−0.3 V to +6 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−65°C to + 125°C

All voltages with respect to VSS.
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

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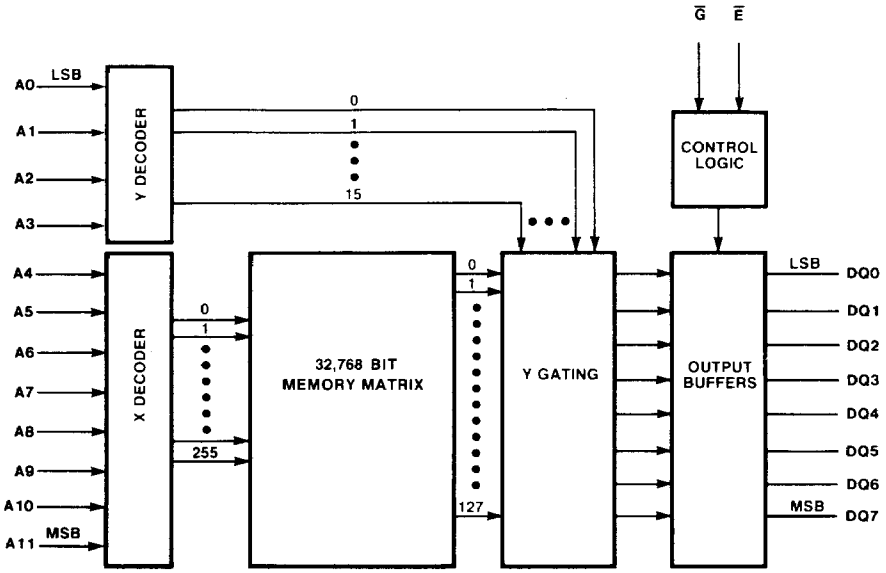
Block Diagram



Mode Selection All voltages referenced to ground

Mode	Outputs	Address Inputs	$\overline{E}$	$\overline{G}$/VPP	VCC	Note
Read	V_{OL} or V_{OH}	V_{IL} or V_{IH}	V_{IL}	V_{IL}	+5 V	1
Deselect/ Active	High Z	V_{IL} or V_{IH}	V_{IL}	V_{IH}	+5 V	1
Deselect/ Power Down	High Z	V_{IL} or V_{IH}	V_{IH}	V_{IH} or V_{IL}	+5 V	1
Program	V_{IH} or V_{IL}	V_{IL} or V_{IH}	Pulse V_{IH} to V_{IL}	V_{PP}	+5 V	1,2
Verify During Program	V_{OL} or V_{OH}	V_{IL} or V_{IH}	V_{IL}	V_{IL}	+5 V	1
Inhibit Program	High Z	V_{IL} or V_{IH}	V_{IH}	V_{PP}	+5 V	1

Read Mode dc Electrical Requirements
T_A = 0°C to 70°C unless otherwise indicated; all voltages referenced to ground

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input HIGH Voltage	2.0		V_{CC} + 1.0	V
V_{IL}	Input LOW Voltage	−0.1		0.8	V

Read Mode dc Electrical Characteristics Over full range of operating voltage and temperature unless otherwise indicated; typical values are for T_A = 25°C and nominal supply voltages

Symbol	Characteristic (Note 3)	Min	Typ	Max	Unit	Note
I_{CC}	Average V_{CC} Current Active		85	150	mA	4
	Average V_{CC} Current Power Down		15	30	mA	4
I_{IN1}	Input Leakage Current (Except $\overline{G}$/VPP)			10	μA	5
I_{IN2}	$\overline{G}$/VPP Input Leakage Current			10	μA	5
I_{OUT}	Output Leakage Current			10	μA	6
V_{OH}	Output HIGH Voltage I_{OH} = −400 μA	2.4			V	
V_{OL}	Output LOW Voltage I_{OL} = 2.1 mA			0.45	V	
C_{IN1}	Input Capacitance (Except $\overline{G}$/VPP)		4.0	6.0	pF	7
C_{IN2}	$\overline{G}$/VPP Input Capacitance			20	pF	7
C_{OUT}	Output Capacitance		8.0	12	pF	8

Notes on following page.

Read Mode ac Electrical Characteristics

Over full range of operating voltage and temperature unless otherwise indicated

Symbol	Characteristic	Min	Max	Unit	Note
t_{ACC}	Address to Output Delay Time		450	ns	9
t_{OE}	Output Enable to Output Delay Time		120	ns	9
t_{OFF}	Output Disable to Output High Impedance		100	ns	
t_{OH}	Address to Output Hold Time	0		ns	
t_{CE}	Power-up Delay from $\overline{E}$ to Outputs Active		450	ns	
t_{PD}	Power-down Delay from $\overline{E}$ to Outputs OFF		100	ns	

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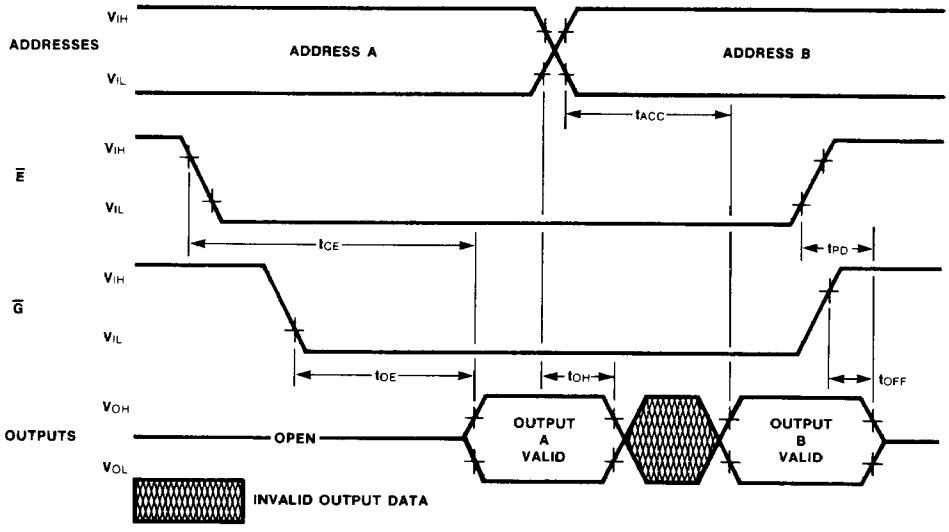
Notes

1. V_{IL} or V_{IH} should be selected on Address and Data inputs as desired.
2. Outputs are in the HIGH state allowing Data In to be applied with TTL drivers.
3. All voltage levels are referenced to VSS.
4. Worst case supply currents occur when all inputs are HIGH (including $\overline{G}$ = 5.0 V) and the ambient temperature is T_A = 0°C.
5. Measured both with V_{IN} = 5.25 V and V_{IN} = 0 V.
6. Measured both with V_{OUT} = 5.25 V and $\overline{G}$ = 5.0 V.
7. Measured with V_{IN} = 0 V, T_A = 25°C and f = 1.0 MHz.
8. Measured with V_{OUT} = 0 V, T_A = 25°C and f = 1.0 MHz.
9. Timing parameters are measured with input logic levels of $V_{IL(max)}$ = 0.8 V and $V_{IH(min)}$ = 2.2 V. Timing measurement reference levels are 1.0 V and 2.0 V for inputs and 0.8 V and 2 V for outputs. An output load of 1 TTL gate plus 100 pF is assumed.

Read Mode Timing Diagram



Erasing Instructions

The contents of the F2732 EPROM can be erased by exposure to high intensity short-wave ultraviolet (UV) light with a wavelength of 2537 Angstroms (Å). This can be accomplished with ultraviolet light EPROM erasure devices which are available from several U.S. manufacturers. These erasure devices contain a UV light source which is usually placed approximately one or two inches from the EPROM to illuminate the transparent window on top of the device. The minimum required integrated dose (intensity x exposure time) of UV light energy incident on the window of the device in order to reliably insure complete erasure is 15 W-s/cm^2. The UV erasure unit should be periodically calibrated if minimum exposure times are to be used. (Minimum exposure times range from 10 to 45 minutes, depending on model type and age of UV lamp.) If longer exposure times are possible, variations in the output light intensity of the UV light source are not critical.

Programming

After erasure with a UV source all bits of the memory will be sensed as V_{OH} levels. Any word of the memory may have V_{OL} levels programmed into it. All eight outputs are programmed at one time for any selected address. Words may be programmed in any order. Programming time for any word regardless of the number of bits to be programmed is 50 ms; maximum programming time for all addresses is 205 s. Once programmed to a V_{OL} level a bit of the array can be changed back to a V_{OH} level by exposing the entire array to a UV source.

The programming procedure is as follows:

1. Apply V_{CC} and V_{SS} with $\overline{E}$ at V_{IH}.
2. Apply V_{PP} to the $\overline{G}$/VPP Input.
3. Apply V_{IL} and V_{IH} to the Address inputs and outputs to select the data combination to be programmed.
4. Apply a 50 ms wide V_{IL} pulse to $\overline{E}$.
5. Apply V_{IL} to $\overline{G}$/VPP and remove the drivers from the output. Read out the contents of the memory (this verification step is optional).
6. Repeat steps 3 through 5 until all desired data has been programmed.
7. Reduce the $\overline{G}$/VPP voltage to V_{IL} to change to the normal read mode.

Caution

It is recommended that a 0.1 μF capacitor be connected between $\overline{G}$/VPP and ground to prevent voltage transients that may damage the device.

Program Mode dc Electrical Requirements and Characteristics $T_A = 25°C \pm 5°C$

Symbol	Characteristic	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
V_{PP}	Programming Input Voltage	24	25	26	V	1
V_{IL}	Input LOW Voltage	−0.1		0.8	V	
V_{IH}	Input HIGH Voltage (Except $\overline{G}$/VPP)	2.0		V_{CC} + 1	V	
I_{IN}	Input Leakage Current (for any input)			10	μA	2
I_{PP}	V_{PP} Supply Current			30	mA	3
I_{CC}	V_{CC} Supply Current		85	150	mA	

Notes on following page.

Program Mode ac Electrical Characteristics and Requirements $T_A = 25°C \pm 5°C$ (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Note
t_{AS}	Address Set-up Time	2			μs	
t_{OES}	$\overline{G}$ Set-up Time	2			μs	
t_{DS}	Data Set-up Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{OEH}	$\overline{G}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{PD}	Power-down Delay from $\overline{E}$ to Outputs OFF	0		120	ns	3
t_{CE}	Chip Enable to Data Valid			1	μs	4
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PR}	$\overline{G}$ Pulse Rise Time During Programming	50			ns	
t_{VR}	V_{PP} Recovery Time	2			μs	

Notes

1. A 0.1 μF capacitor must be connected between $\overline{G}/V_{PP}$ and ground to prevent voltage transients which may damage the device.
2. V_{IN} = 5.25 V to 0 V.
3. $\overline{E} = V_{IL}$.
4. $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$.

Program Mode Timing Diagram