BA3128N
BA3128F

Audio-switched operational amplifier (2 inputs, 1 output)

The BA3128N and BA3128F are operational amplifiers provided with an analog switch. This enables the gain of the amplifiers to be switched at the same time as the inputs to the amplifiers.

Control of the gain is controlled externally by setting one of the pins ON or OFF.

The ICs can be powered by single or dual power supplies.

Features

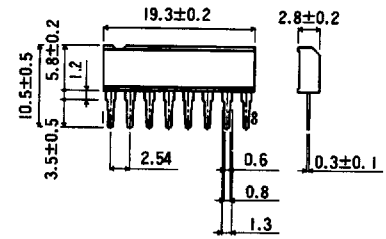
- available in SIP8 and SOP8 packages
- single power supply: 5 ~ 32 V
  dual power supply: ±2.5 ~ ±16 V
- low noise: $V_N = 2.0\ \mu V_{rms}$ typically
- low switching noise
- high gain and low distortion:
  $G_{VO} = 110$ dB, THD = 0.0015%

Applications

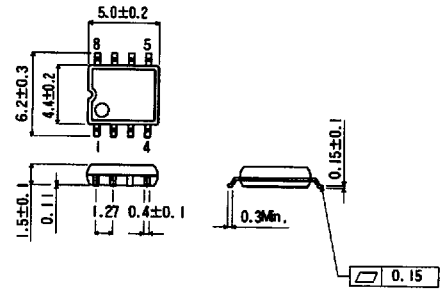
- video tape recorders
- amplifiers

Dimensions (Units : mm)

BA3128N (SIP8)

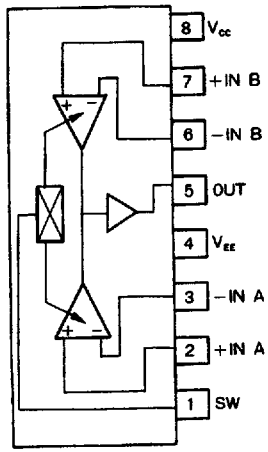


BA3128F (SOP8)



Block diagram

BA3128N



BA3128F

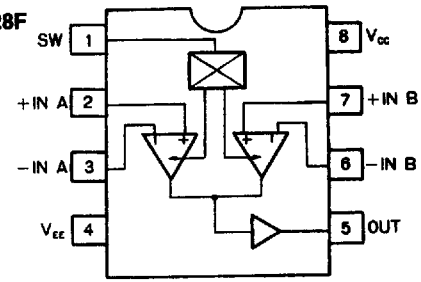
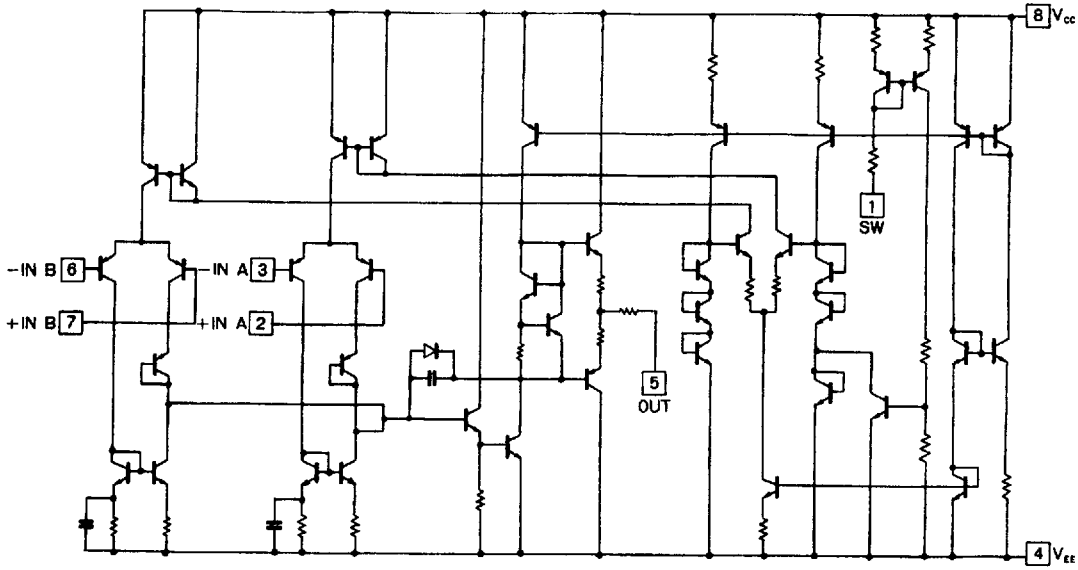


Table 1 Pin description

Pin number	Pin names	Function
1	SW	Channel switch control
2	+ IN A	A channel non-inverted input
3	− IN A	A channel inverted input
4	V_{EE}	− Power supply (GND)
5	OUT	Output
6	− IN B	B channel inverted input
7	+ IN B	B channel non-inverted input
8	V_{CC}	+ Power supply

Circuit diagram



Absolute maximum ratings (T_a = 25°C)

Parameter		Symbol	Limits	Unit	Conditions
Applied voltage		V_{CC}	±18	V	
Power dissipation	BA3128F	P_d	450	mW	Reduce power by 4.5 mW/°C for each degree above 25°C.
	BA3128N		900		Reduce power by 9 mW/°C for each degree above 25°C.
Operational temperature		T_{opr}	−20 ~ +75	°C	
Storage temperature		T_{stg}	−55 ~ +125	°C	
Differential input voltage		V_{id}	±V_{CC}	V	
Common mode input voltage		V_i	−V_{CC} ~ +V_{CC}	V	
Load current		$I_{o\ max}$	±50	mA	

Electrical characteristics (unless otherwise noted, T_a = 25°C, V_{CC} = 15 V, V_{EE} = -15 V)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test figure
Quiescent current	I_Q		2.5	5.0	mA	V_{in} = 0, R_L = ∞, SW pin open	2
Input offset voltage	V_{IO}		0.5	5.0	mV	$R_S \leq 10$ kΩ	1
Input offset current	I_{IO}		5	200	nA		1
Input bias current	I_B		50	500	nA	Direction of I_B is out of IC (because 1st stage is PNP transistor)	1
High amplitude voltage gain	A_V	86	110		dB	$R_L \geq 2$ kΩ, V_O = ±10 V	1
Common mode input voltage	V_{ICM}	±12	±14		V		1
Common mode rejection ratio	CMRR	70	90		dB	$R_S \leq 10$ kΩ	1
Power supply rejection ratio	PSRR	76	90		dB	$R_S \leq 10$ kΩ	1
Maximum output voltage	V_{OH}/V_{OL}	±12	±14		V	$R_L \geq 10$ kΩ	3, 4
		±10	±13		V	$R_L \geq 2$ kΩ	
Slew rate	SR		2.4		V/μs	G_V = 0 dB, R_L = 2 kΩ	5
Frequency band width gain	G_{BW}		6.5		MHz	f = 10 kHz	6
Input conversion noise voltage	V_n		2.0		μV	R_S = 2 kΩ, B. P. F. = 20 Hz ~ 30 kHz	7
A to B crosstalk	CT_{A-B}		85		dB	f = 1 kHz	8
Total harmonic distortion	THD		0.0015		%	f = 1 kHz, V_O = 5 V_{rms}	9

Figure 1 Test circuit 1

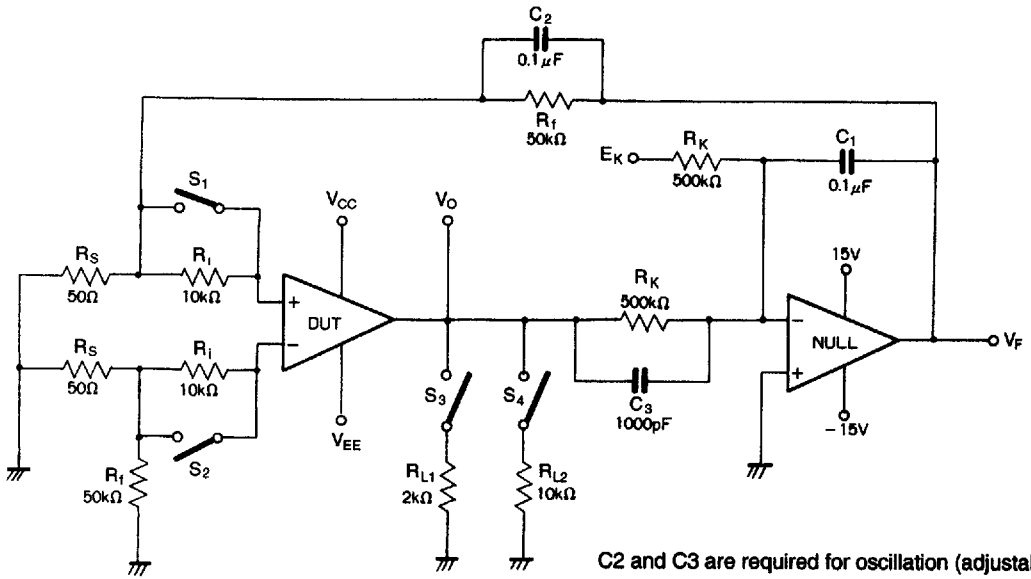


Table 2 Test conditions for Test circuit 1

Test item	V_{CC}	V_{EE}	E_K	V_F	S_1	S_2	S_3	S_4	Formula
Input offset voltage	15	−15	0	V_{F1}	ON	ON	OFF	OFF	1
Input offset current	15	−15	0	V_{F2}	OFF	OFF	OFF	OFF	2
Input bias current	15	−15	0	V_{F3}	OFF	ON	OFF	OFF	3
				V_{F4}	ON	OFF			
High amplitude voltage gain	15	−15	−10	V_{F5}	ON	ON	ON	OFF	4
			10	V_{F6}					
Common mode input voltage Common mode rejection ratio	3	−27	12	V_{F7}	ON	ON	OFF	OFF	5
	27	−3	−12	V_{F8}					
Power supply rejection ratio	2	−2	0	V_{F9}	ON	ON	OFF	OFF	6
	16	−16	0	V_{F10}					

1. Input offset voltage $(V_{IO}) = \dfrac{|V_{F1}|}{1 + R_f/R_S}$

2. Input offset current $(I_{IO}) = \dfrac{|V_{F2} - V_{F1}|}{R_i(1 + R_f/R_S)}$

3. Input bias current $(I_B) = \dfrac{|V_{F4} - V_{F3}|}{2R_i(1 + R_f/R_S)}$

4. High amp volt gain $(I_{IO}) = 20\log\dfrac{20(1 + R_f/R_S)}{|V_{F6} - V_{F5}|}$

5. Common mode rejection ratio
$(CMRR) = 20\log\dfrac{24(1 + R_f/R_S)}{|V_{F8} - V_{F7}|}$

6. Power supply rejection ratio
$(PSRR) = 20\log\dfrac{28(1 + R_f/R_S)}{|V_{F10} - V_{F9}|}$

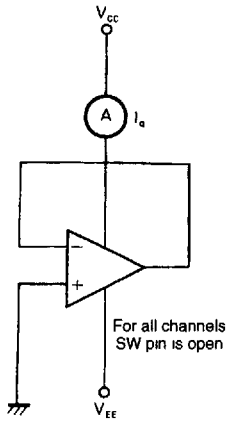


Figure 2 Test circuit 2 (I_Q)

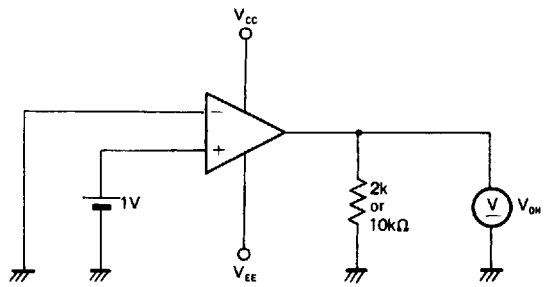


Figure 3 Test circuit 3 (V_{OH})

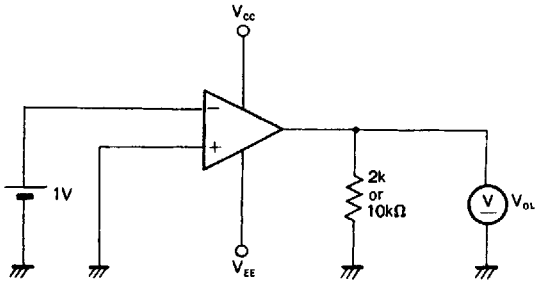


Figure 4 Test circuit 4 (V_{OL})

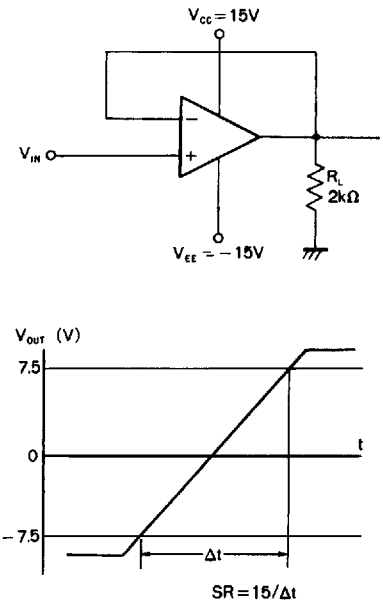


Figure 5 Test circuit 5 (Slew rate)

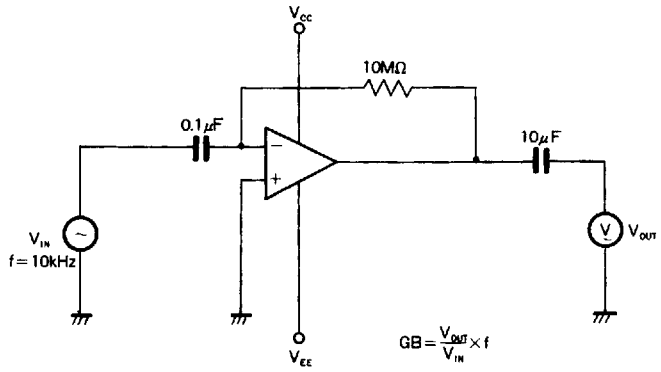


Figure 6 Test circuit 6 (Gain bandwidth)

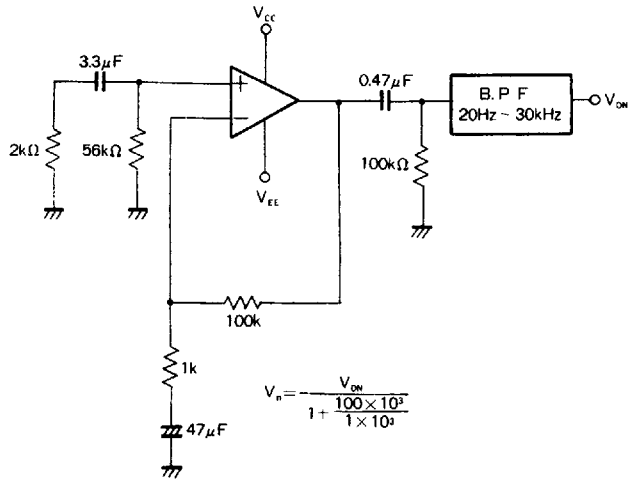


Figure 7 Test circuit 7 (V_N)

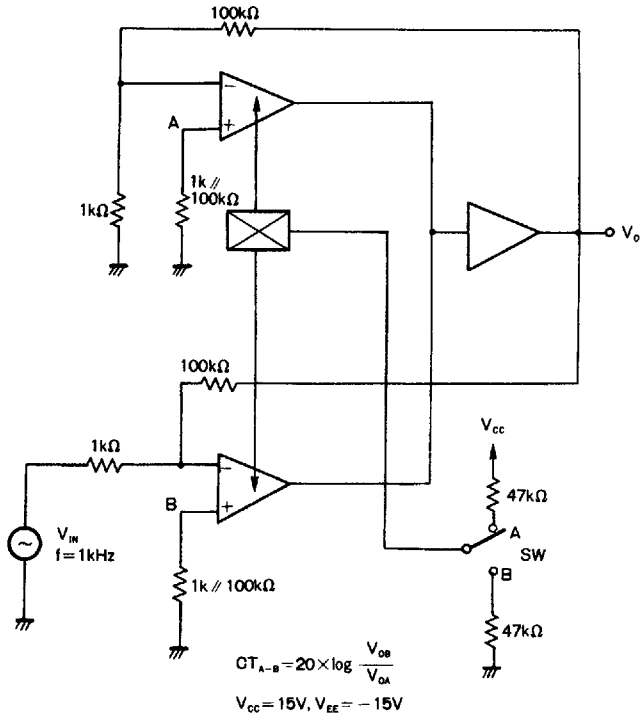


Figure 8 Test circuit 8 (CT_{A-B})

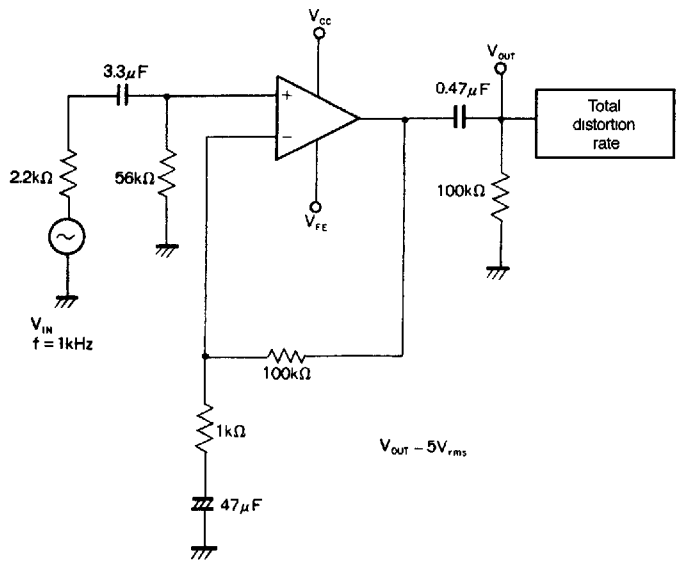
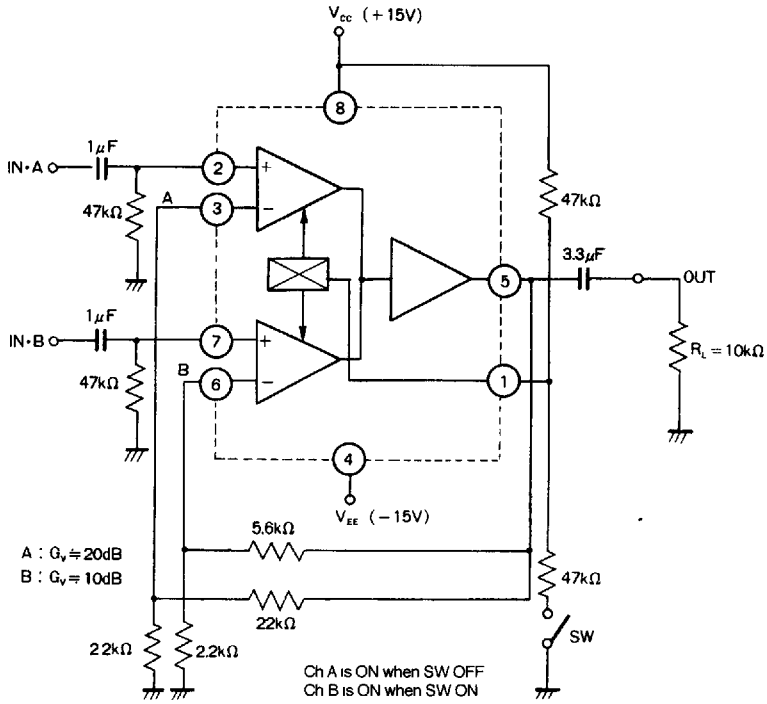


Figure 9 Test circuit 9 (THD)

Figure 10 Application example

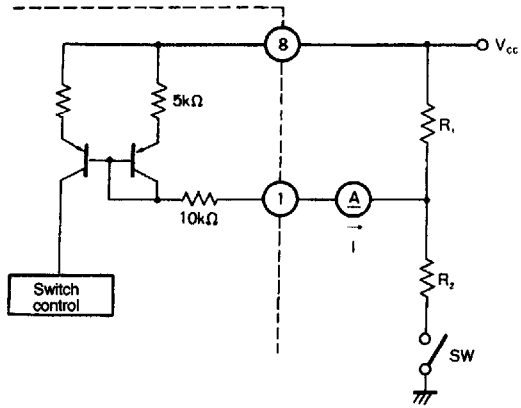


The input switch is operated by the external switch. When the external switch (SW) is OFF, the A-channel functions. When the external switch (SW) is ON, the B-channel functions. The pin voltage (V) of the control pin is

$$V \cong V_{CC} - (5 \times 10^3 + 10 \times 10^3)\, I - 0.7$$

Therefore, make sure to select R1 and R2 such that when SW is OFF, the switch current (I) is below 1 μA and when SW is ON, the switch current (I) is above 20 μA (see Figure 10).

Figure 11 Equivalent circuit for the switch circuit



Electrical characteristic curves

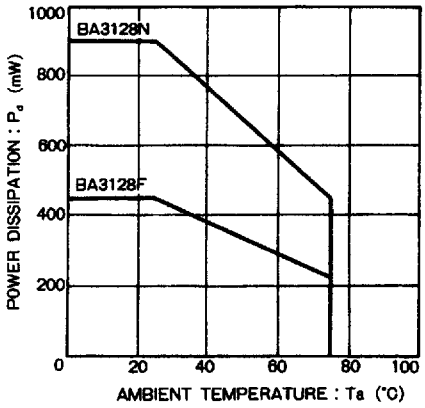


Figure 12

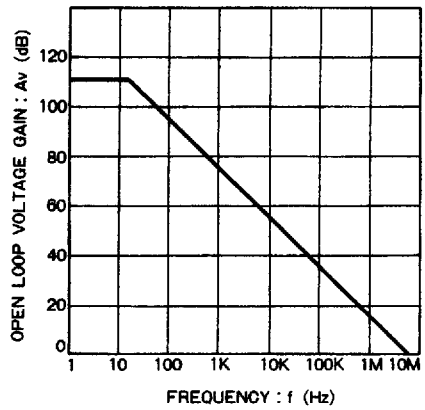


Figure 13

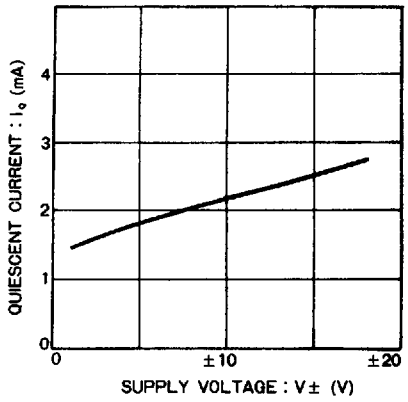


Figure 14

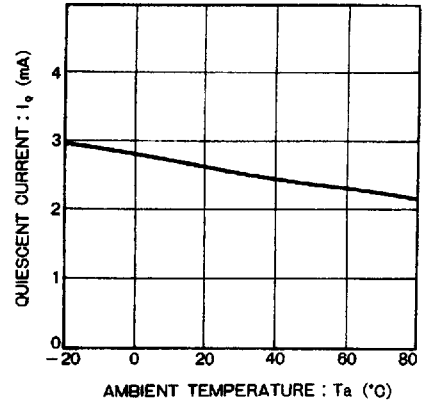


Figure 15

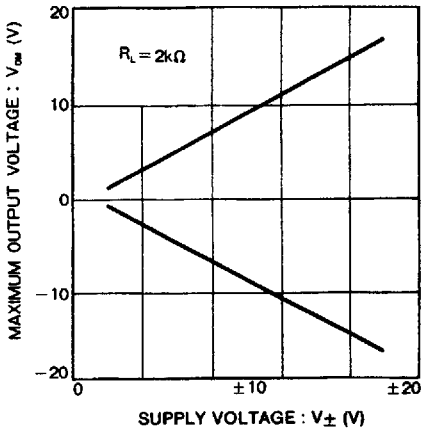


Figure 16

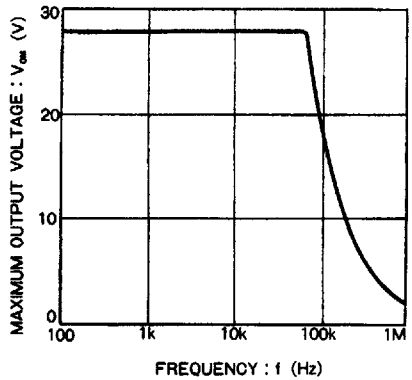


Figure 17