T-79-40

HARRIS

CA3280A
CA3280

Dual Variable Operational Amplifiers

August 1991

Features

- Low Initial Input-Offset Voltage: 500μV Max. (CA3280A)
- Low Offset-Voltage Change vs I_{ABC}: <500μV Typ. for All Types
- Low Offset-Voltage Drift: 5μV/C Max. (CA3280A)
- Excellent Matching of the Two Amplifiers for All Characteristics
- Internal Current-Driven Linearizing Diodes Reduce the External Input Current to an Offset Component

Applications

- Voltage-Controlled Amplifiers
- Voltage-Controlled Oscillators
- Multipliers
- Demodulators
- Sample and Hold
- Instrumentation Amplifiers
- Function Generators
- Triangle Wave-to-Sine Wave Converters
- Comparators
- Audio Preamplifiers

Description

The CA3280 and CA3280A types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset-voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Inter-digitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

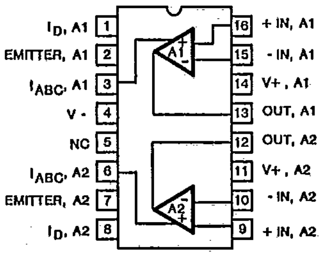
The CA3280 has all the generic characteristics of an operational voltage amplifier except that the forward transfer characteristics is best described by transcondcutance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced in 1969*, and it has since gained wide acceptance as a gateable, gain-controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and highspeed comparators.

The operating-temperature ranges are -55°C to +125°C for the CA3280A, and 0°C to +70°C for the CA3280. The CA3280 and CA3280A are supplied in the 16 lead dual-in-line plastic package (E suffix), in the 16 lead dual-in-line frit-seal ceramic package (F suffix), and in chip form (H suffix).

For additional application information on this device and on OTAs in general, please refer to Application Notes: ICAN-6818, ICAN-6668, and ICAN-6077.

Pinouts

E AND F SUFFIX
TOP VIEW



Functional Diagram

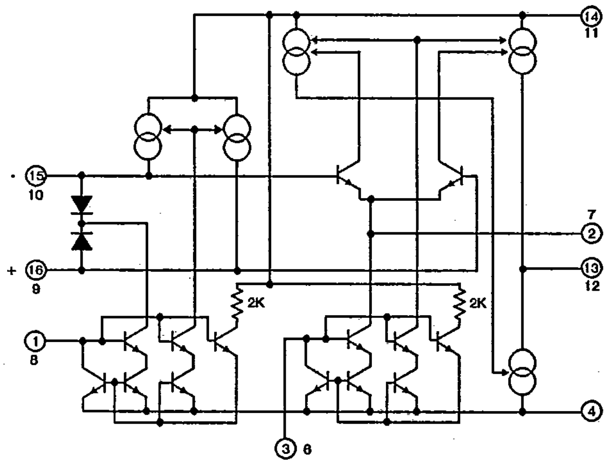


FIGURE 1. FUNCTIONAL DIAGRAM OF ½ CA3280

*"OTA Obsoletes Op Amp," by C.F. Wheatley and H.A. Wittlinger, NEC Proceedings, December 1969.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 1174.1

T-79-40

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V+ AND V- TERMINALS)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE RANGE	V+ to V-
INPUT SIGNAL CURRENT AT $I_D = 0$	100 μA
AMPLIFIER BIAS CURRENT	10 mA
OUTPUT SHORT CIRCUIT DURATION*	Indefinite
LINEARIZING DIODE BIAS CURRENT, I_D	5 mA
PEAK INPUT CURRENT WITH LINEARIZING DIODE	$\pm I_D$
POWER DISSIPATION, P_D:	
Either Amplifier	600 mW
Total Package	750 mW
Above 55° C	Derate linearly at 6.67 mW/° C
AMBIENT TEMPERATURE RANGE, T_A:	
Operating:	
CA3280	0 to +70° C
CA3280A	-55 to +125° C
Storage, All Types	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10 sec. max	+265° C

*Short circuit may be applied to ground or to either supply.

T-79-40

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $V^{\pm}$ = 15 V (Unless Otherwise Stated)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA3280 Min.	CA3280 Typ.	CA3280 Max.	CA3280A Min.	CA3280A Typ.	CA3280A Max.	UNITS
Input Offset Voltage, V_{IO}	I_{ABC}=1 mA	–	–	3	–	–	0.5	mV
	I_{ABC}=100µA	–	0.7	3	–	0.25	0.5	mV
	I_{ABC}=10µA	–	–	3	–	–	0.5	mV
	I_{ABC}=1mA to 10µA, T_A=full temp. range	–	0.8	4	–	0.8	1.5	mV
Input Offset Voltage Change, $\|\Delta V_{IO}\|$	I_{ABC}=1µA to 1mA	–	0.5	1	–	0.5	1	mV
	I_{ABC}=100µA, T_A=full temp. range	–	5	–	–	3	5	µV/°C
Amplifier Bias Voltage, V_{ABC}	I_{ABC}=100µA	–	1.2	–	–	1.2	–	V
Peak Output Voltage: Positive V_{OM}^+	I_{ABC}=500µA	12	13.7	–	12.5	13.7	–	V
Negative V_{OM}^-	I_{ABC}=500µA	12	−14.3	–	−13.3	−14.3	–	V
Positive V_{OM}^+	I_{ABC}=5µA	12	13.9	–	12.5	13.9	–	V
Negative V_{OM}^-	I_{ABC}=5µA	12	−14.5	–	−13.5	−14.5	–	V
Common-Mode Input Voltage Range, V_{ICR}	I_{ABC}=100µA	−13	–	13	−13	–	13	V
Noise Voltage, e_N: 10 Hz	I_{ABC}=500µA	–	20	–	–	20	–	nV/√Hz
1 kHz	I_{ABC}=500µA	–	8	–	–	8	–	nV/√Hz
10 kHz	I_{ABC}=500µA	–	7	–	–	7	–	nV/√Hz
Input Offset Current, I_{IO}	I_{ABC}=500µA	–	0.3	0.7	–	0.3	0.7	µA
Input Bias Current, I_{IB}	I_{ABC}=500µA	–	1.8	5	–	1.8	5	µA
	I_{ABC}=500µA, T_A=full temp. range	–	3	8	–	3	8	µA
Peak Output Current: Source I_{OM}^+	I_{ABC}=500µA	350	410	650	350	410	650	µA
Sink I_{OM}^-	I_{ABC}=500µA	−350	−410	−650	−350	−410	−650	µA
Source I_{OM}^+	I_{ABC}=5µA	3	4.1	7	3	4.1	7	µA
Sink I_{OM}^-	I_{ABC}=5µA	−3	−4.1	−7	−3	−4.1	−7	µA
Sink and Source, I_{OM}^-, I_{OM}^+	I_{ABC}=500µA, T_A=full temp. range	350	450	550	350	450	550	µA
Linearization Diodes: Dynamic Impedance	I_D = 100µA	–	700	–	–	700	–	Ω
Offset Current	I_D=100µA	–	10	–	–	10	–	µA
	I_D=10µA	–	0.5	1	–	0.5	1	µA

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA3280 Min.	CA3280 Typ.	CA3280 Max.	CA3280A Min.	CA3280A Typ.	CA3280A Max.	UNITS
Diode Network Supply Current	I_{ABC}=100μA	250	400	800	250	400	800	μA
Amplifier Supply Current (Per amplifier)	I_{ABC}=500μA	–	2	2.4	–	2	2.4	mA
Amplifier Output Leakage Current, I_{OL}	I_{ABC}=0, V_O=0V.	–	0.015	0.1	–	0.015	0.1	nA
	I_{ABC}=0, V_O=30V	–	0.15	1	–	0.15	1	nA
Common-Mode Rejection Ratio, CMRR	I_{ABC}=100μA	80	100	–	94	100	–	dB
Power-Supply Rejection Ratio, PSRR	I_{ABC}=100μA	86	105	–	94	105	–	dB
Open-Loop Voltage Gain, A_{OL}	I_{ABC}=100μA, R_L=∞, V_O=20 Vp-p	94	100	–	94	100	–	dB
		50K	100K	–	50K	100K	–	V/V
Forward Transconductance: Large Signal, Gm	I_{ABC}=50μA	–	0.8	1.2	–	0.8	1.2	mmho
Small Signal, gm	I_{ABC}=1mA	–	16	22	–	16	22	
Input Resistance, R_I	I_{ABC}=10μA	0.5	–	–	0.5	–	–	MΩ
Channel Separation	f=1 kHz	–	94	–	–	94	–	dB
Open-Loop Total Harmonic Distortion	f=1 kHz, I_{ABC}=1.5 mA, R_L=15kΩ, V_O=20 Vp-p	–	0.4	–	–	0.4	–	%
Bandwidth	I_{ABC}=1mA, R_L=100Ω	–	9	–	–	9	–	MHz
Slew Rate, SR: Open Loop	I_{ABC}=1mA	–	125	–	–	125	–	V/μs
Capacitance: Input, C_I	I_{ABC}=100μA	–	4.5	–	–	4.5	–	pF
Output, C_O		–	7.5	–	–	7.5	–	pF
Output Resistance, R_O	I_{ABC}=100μA	–	63	–	–	63	–	MΩ

Figs. 2 and 3 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common-mode range of the CA3280.

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single-ended converters, as shown in Fig. 4. A matched resistor network requires ratio matching of 0.01% or trimming for 80 dB of common-mode rejection. The CA3280, with its excellent common-mode rejection ratio, is capable of converting a small (±25 mV) differential input signal to a single-ended output without the need for a matched resistor network.

Fig. 5 shows the CA3280 in a typical gain-control application. The input-signal range as a function of distortion at various levels of linearization diode current is shown in Fig. 6 This curve shows only the AGC capability of the diode network, but gain control can also be performed with the amplifier bias current (I_{ABC}). With no diode bias current, the gain is merely gmR_L. For example, with an I_{ABC} of 1 mA, the gm is approximately 16 mmhos. With the CA3280 operating into a 5 kΩ resistor, the gain is 80.

The need for external buffers can be eliminated by the use of low-value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

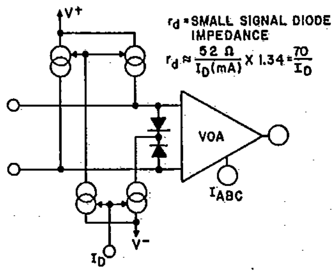


Fig. 2 — VOA showing linearization diodes and current drive.

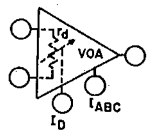


Fig. 3 — Block diagram of linearized VOA.

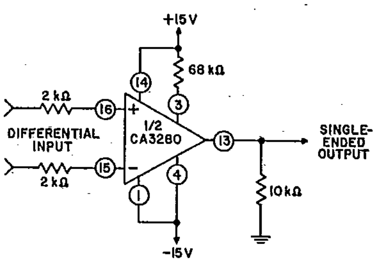


Fig. 4 — Differential to single-ended converter.

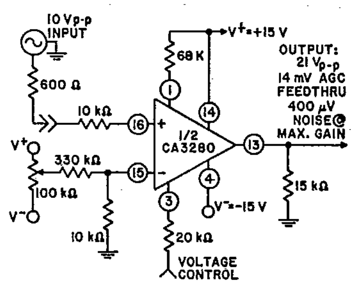


Fig. 5 — Typical gain control circuit.

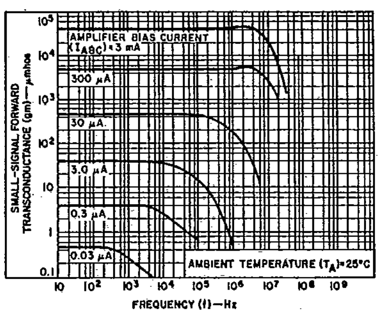


Fig. 6 — Amplifier gain as a function of frequency.

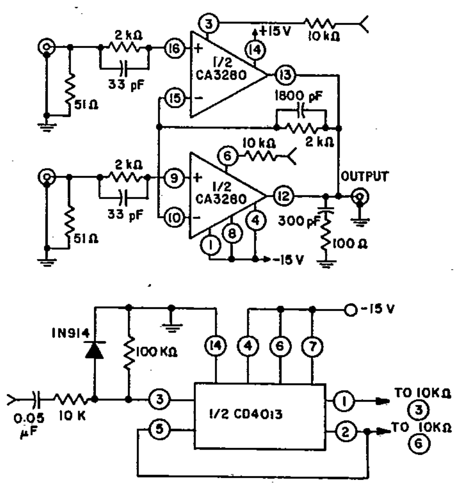


Fig. 7 — Two-channel linear multiplexer.

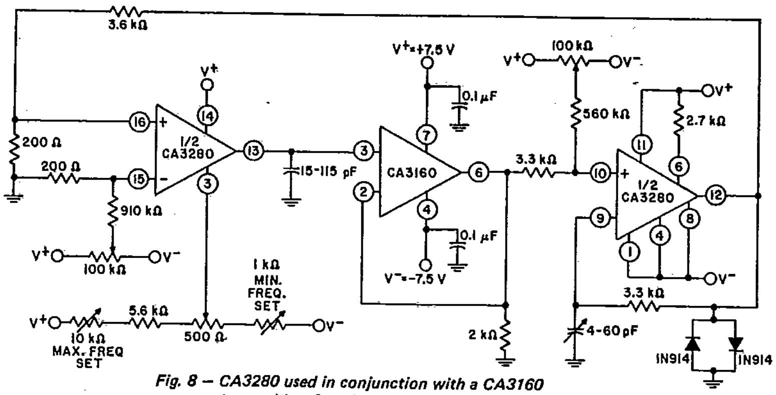


Fig. 8 – CA3280 used in conjunction with a CA3160 to provide a function generator with a tunable range of from 2 Hz to 1 MHz.

Fig. 9 shows a triangle wave-to-sine wave converter using the CA3280. Two 100KΩ resistors are connected between the differential amplifier emitters and V+ to reduce the current flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is approximately 0.37% for this circuit.

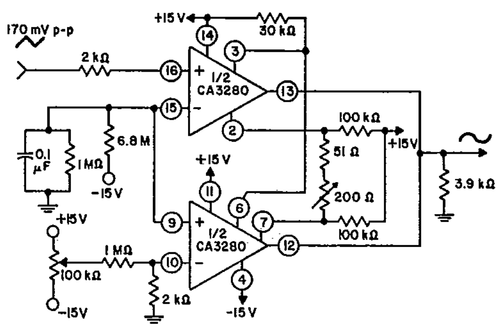


Fig. 9 – Triangle wave-to-sine wave converter.

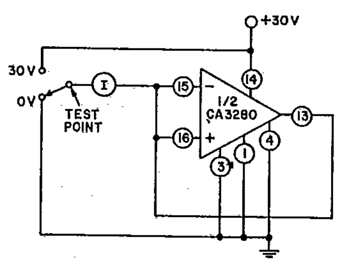


Fig. 10 – Leakage current test circuit.

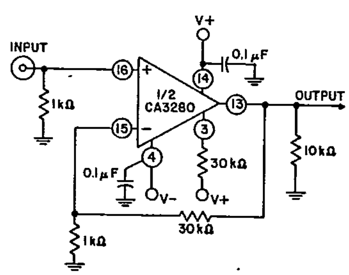


Fig. 11 – Channel separation test circuit.

I_{abc} = 650 μA
I_D = 200 μA
VERT = 200 μA/DIV
HOR = 1 V/DIV

a) With diode programming terminal active

I_{abc} = 650 μA
I_D = 0
VERT = 200 μA/DIV
HOR = 25 mV/DIV

b) With diode programming terminal cut-off

Fig. 12 – CA3280 transfer characteristics.

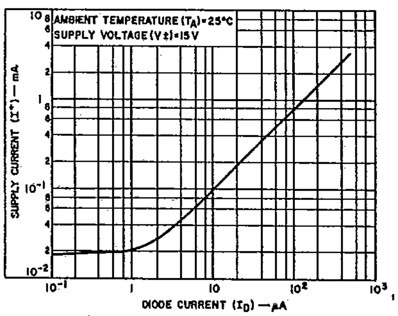


Fig. 13 – Supply current as a function of diode current.

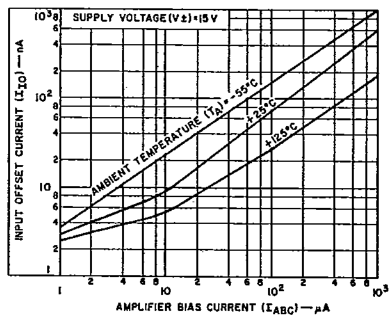


Fig. 14 – Input offset current as a function of amplifier bias current.

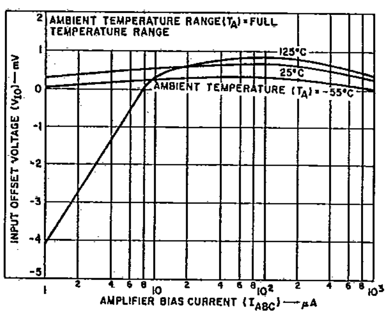


Fig. 15 – Input offset voltage as a function of amplifier bias current.

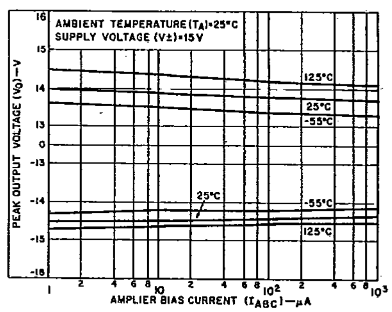


Fig. 16 – Peak output voltage as a function of amplifier bias current.

3

OPERATIONAL AMPLIFIERS

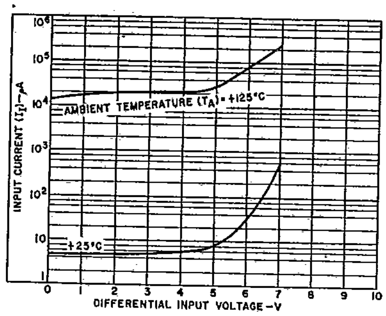


Fig. 17 – Input current as a function of input differential voltage.

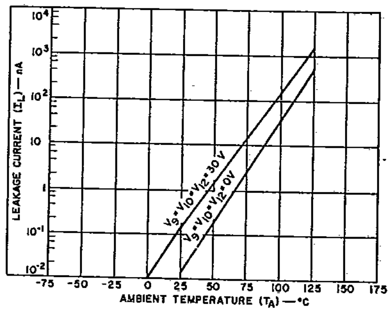


Fig. 18 – Leakage current as a function of temperature.

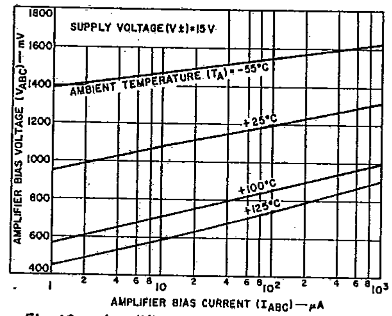


Fig. 19 – Amplifier bias voltage as a function of amplifier bias current.

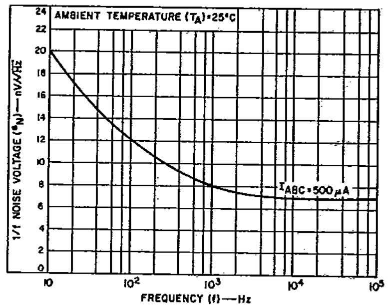


Fig. 20 – I/F noise as a function of frequency.

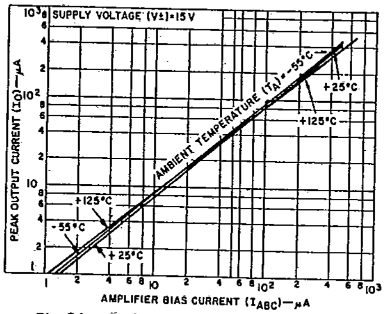


Fig. 21 – Peak output current as a function of amplifier bias current.

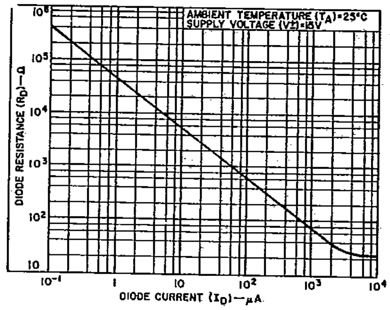


Fig. 22 – Diode resistance as a function of diode current.

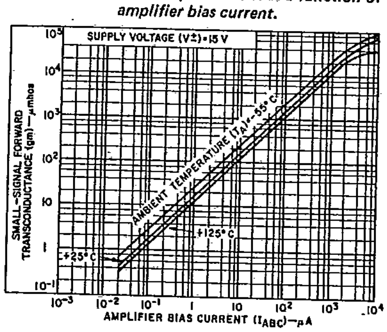


Fig. 23 – Amplifier gain as a function of amplifier bias current.

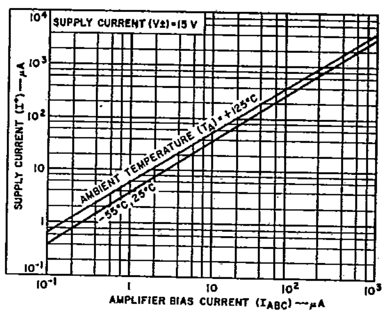


Fig. 24 – Supply current as a function of amplifier bias current.

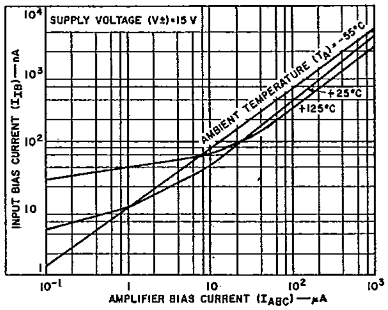
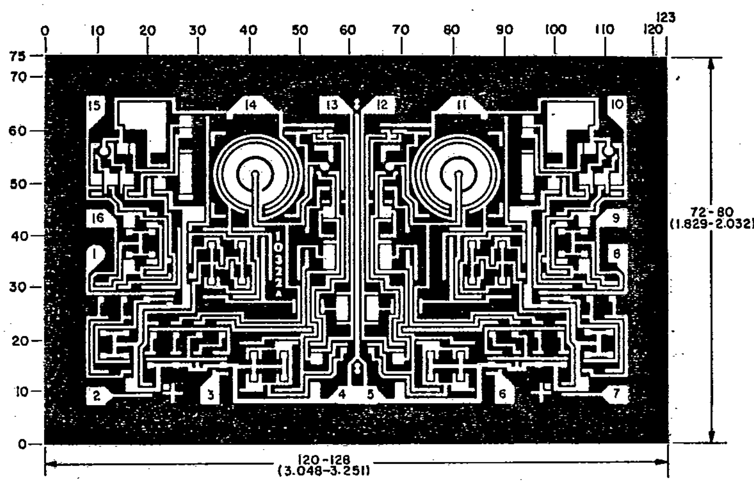


Fig. 25 — Input bias current as a function of amplifier bias current.



Dimensions and pad layout for CA3280H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).