FEATURES

- ❑ Pipeline Registers —
  Dual 7-Deep (L29C524) or
  Dual 8-Deep (L29C525)
- ❑ Configurable to Single 14-Deep and
  Single 16-Deep
- ❑ Low Power CMOS Technology
- ❑ Replaces AMD Am29524 and
  Am29525
- ❑ Load, Shift, and Hold Instructions
- ❑ Separate Data In and Data Out Pins
- ❑ Three-State Outputs
- ❑ DESC SMD No. 5962-91696
- ❑ Available 100% Screened to
  MIL-STD-883, Class B
- ❑ Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic Flatpack
  - 28-pin Plastic LCC, J-Lead

DESCRIPTION

The **L29C524** and **L29C525** are high-speed, low power CMOS pipeline registers. They are pin-for-pin compatible with the AMD Am29524 and Am29525. The products can be configured as two independent 7-level (or 8-level) pipelines or as single 14-level (or 16-level) pipeline. The configuration implemented is determined by the instruction code (I_{1-0}) as shown in Table 2.

The I_{1-0} instruction code controls the internal routing of data and loading of each register. For instruction $I_{1-0} = 00$ (Push A and B), data applied at the D_{7-0} inputs is latched into register A0 on the rising edge of CLK. The contents of A0 simultaneously move to register A1, A1 moves to A2, and so on. The contents of the last register on the A side (A6 for the L29C524, A7 for the L29C525) are wrapped back to register B0. The registers on the B side are similarly shifted, with the contents of the last register on the B side (B6 for the L29C524, B7 for the L29C525) lost.

Instruction $I_{1-0} = 01$ (Push B) acts similarly to the Push A and B instruction, except that only the B side registers are shifted. The input data is applied to register B0, and the contents of the last register on the B side (B6 for the L29C524, B7 for the L29C525) are lost. The contents of the A side registers are unaffected. Instruction $I_{1-0} = 10$ (Push A) is identical to the Push B instruction, except that the A side registers are shifted and the B side registers are unaffected.

Instruction $I_{1-0} = 11$ (Hold) causes no internal data movement. It is equivalent to preventing the application of a clock edge to any internal register.

The contents of any of the registers is selectable at the output through the use of the S_{3-0} control inputs. On the L29C524, the input pins D_{7-0} may also be selected to drive the output, and all output pins may be forced to zero. The independence of the I and S control lines allows simultaneous reading and writing. Encoding for the S_{3-0} controls is given in Table 3.

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L29C524/525 BLOCK DIAGRAM

*Applies to L29C525 only — refer to Table 3
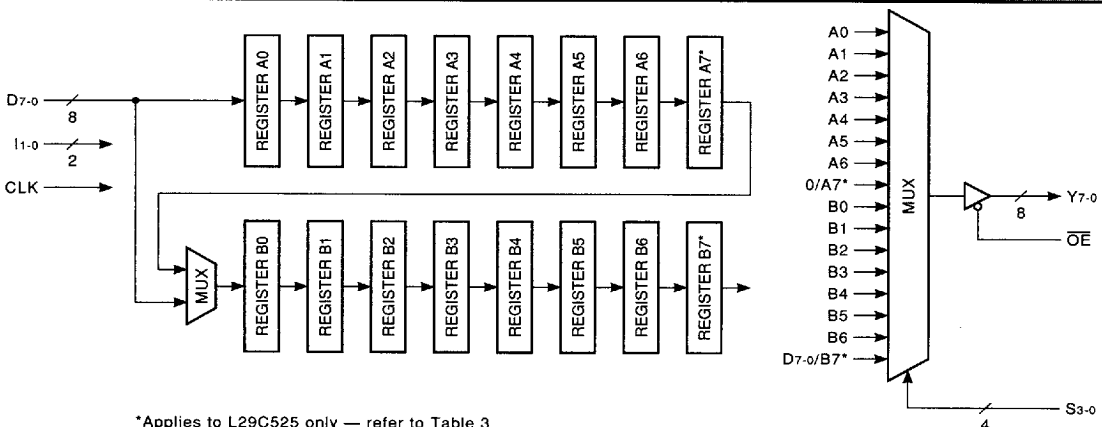
Pipeline Registers

01/19/94-LDS.524/5-E

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TABLE 1. REGISTER LOAD OPERATIONS

Single 14/16 Level	Dual 7/8 Level		
Push A and B	Push B	Push A	Hold All Registers

*Applies to L29C525 only

TABLE 2. INSTRUCTION SET

Mnemonics	Inputs		Description
	I1	I0	
Shift	0	0	Push A and B
LDB	0	1	Push B
LDA	1	0	Push A
HLD	1	1	Hold All Registers

TABLE 3. OUTPUT SELECT

S3	S2	S1	S0	Y7-0
0	0	0	0	A0
0	0	0	1	A1
0	0	1	0	A2
0	0	1	1	A3
0	1	0	0	A4
0	1	0	1	A5
0	1	1	0	A6
0	1	1	1	0 (L29C524) A7 (L29C525)
1	0	0	0	B0
1	0	0	1	B1
1	0	1	0	B2
1	0	1	1	B3
1	1	0	0	B4
1	1	0	1	B5
1	1	1	0	B6
1	1	1	1	D7-0 (L29C524) B7 (L29C525)

Pipeline Registers

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MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature .... −65°C to +150°C

Operating ambient temperature .... −55°C to +125°C

Vcc supply voltage with respect to ground .... −0.5 V to +7.0 V

Input signal with respect to ground .... −3.0 V to +7.0 V

Signal applied to high impedance output .... −3.0 V to +7.0 V

Output current into low outputs .... 25 mA

Latchup current .... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	Vcc = Min., I_{OH} = −12 mA	2.4			V
V_{OL}	Output Low Voltage	Vcc = Min., I_{OL} = 24 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ Vcc (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ Vcc (Note 12)			±20	µA
I_{CC1}	Vcc Current, Dynamic	(Notes 5, 6)		10	35	mA
I_{CC2}	Vcc Current, Quiescent	(Note 7)			1.0	mA

Pipeline Registers

01/19/94–LDS.524/5-E

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol	Parameter	L29C524/525– 20 Min	Max	15 Min	Max
tPD	Clock to Output Delay		20		15
tSEL	Select to Output Delay		20		15
tPDDO	Data to Output Delay (L29C524)		20		15
tPW	Clock Pulse Width	12		10	
tSD	Data Setup Time	7		5	
tHD	Data Hold Time	0		0	
tSI	Instruction Setup Time	7		5	
tHI	Instruction Hold Time	2		2	
tENA	Three-State Output Enable Delay (Note 11)		15		15
tDIS	Three-State Output Disable Delay (Note 11)		13		13

MILITARY OPERATING RANGE (–55°C to +125°C) Notes 9, 10 (ns)

Symbol	Parameter	L29C524/525– 25 Min	Max	20 Min	Max
tPD	Clock to Output Delay		25		20
tSEL	Select to Output Delay		25		20
tPDDO	Data to Output Delay (L29C524)		25		20
tPW	Clock Pulse Width	12		12	
tSD	Data Setup Time	7		7	
tHD	Data Hold Time	2		2	
tSI	Instruction Setup Time	7		7	
tHI	Instruction Hold Time	2		2	
tENA	Three-State Output Enable Delay (Note 11)		15		15
tDIS	Three-State Output Disable Delay (Note 11)		13		13

SWITCHING WAVEFORMS

Pipeline Registers

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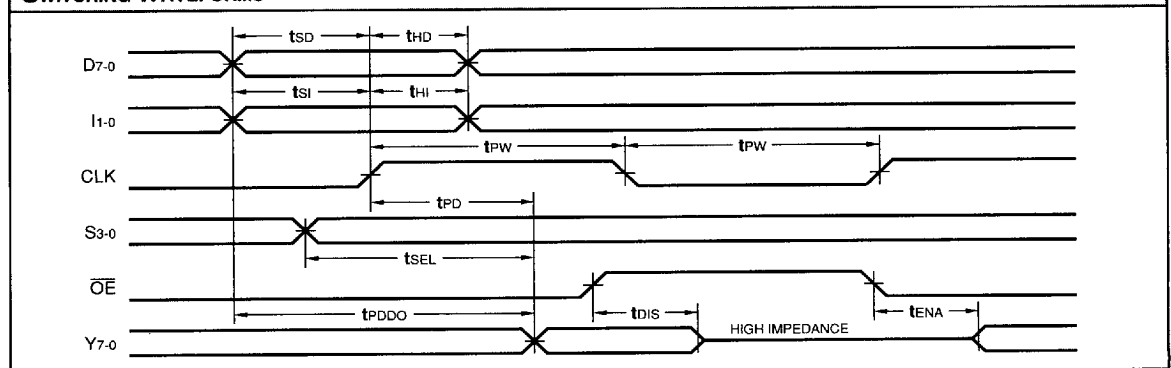
NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at –0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tENA/tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For tENABLE and tDISABLE measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.
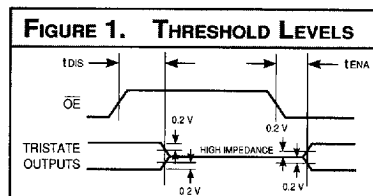
c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from

the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
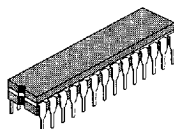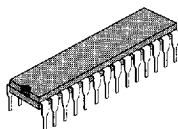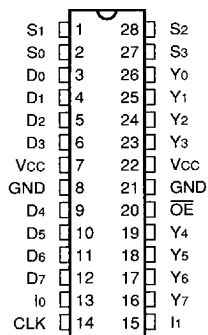
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.
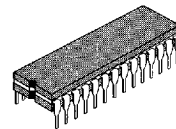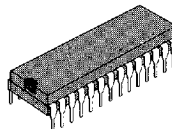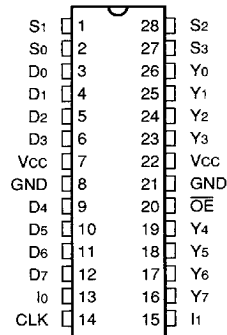

FIGURE 1. THRESHOLD LEVELS

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L29C524 — ORDERING INFORMATION

28-pin — 0.3" wide

```
        S1  [ 1    28 ]  S2
        S0  [ 2    27 ]  S3
        D0  [ 3    26 ]  Y0
        D1  [ 4    25 ]  Y1
        D2  [ 5    24 ]  Y2
        D3  [ 6    23 ]  Y3
        Vcc [ 7    22 ]  Vcc
        GND [ 8    21 ]  GND
        D4  [ 9    20 ]  OE
        D5  [ 10   19 ]  Y4
        D6  [ 11   18 ]  Y5
        D7  [ 12   17 ]  Y6
        I0  [ 13   16 ]  Y7
        CLK [ 14   15 ]  I1
```

28-pin — 0.4" wide

```
        S1  [ 1    28 ]  S2
        S0  [ 2    27 ]  S3
        D0  [ 3    26 ]  Y0
        D1  [ 4    25 ]  Y1
        D2  [ 5    24 ]  Y2
        D3  [ 6    23 ]  Y3
        Vcc [ 7    22 ]  Vcc
        GND [ 8    21 ]  GND
        D4  [ 9    20 ]  OE
        D5  [ 10   19 ]  Y4
        D6  [ 11   18 ]  Y5
        D7  [ 12   17 ]  Y6
        I0  [ 13   16 ]  Y7
        CLK [ 14   15 ]  I1
```

Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P11)	Ceramic DIP (C10)
0°C to +70°C — Commercial Screening				
20 ns	L29C524PC20	L29C524CC20	L29C524NC20	L29C524IC20
15 ns	L29C524PC15	L29C524CC15	L29C524NC15	L29C524IC15
–55°C to +125°C — Commercial Screening				
25 ns		L29C524CM25		L29C524IM25
20 ns		L29C524CM20		L29C524IM20
–55°C to +125°C — MIL-STD-883 Compliant				
25 ns		L29C524CMB25		L29C524IMB25
20 ns		L29C524CMB20		L29C524IMB20

Pipeline Registers

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L29C524 — ORDERING INFORMATION
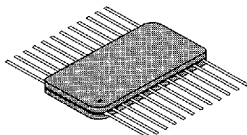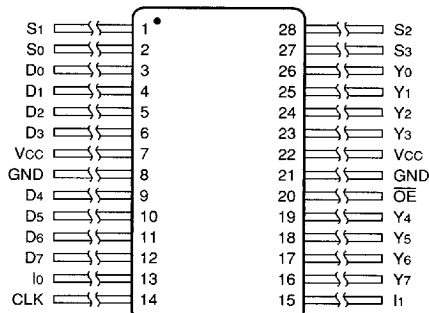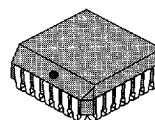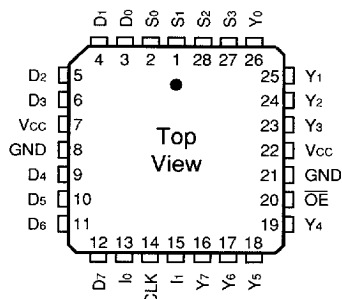
28-pin

```
S1  ⊏⊐  1 •        28  ⊏⊐  S2
S0  ⊏⊐  2          27  ⊏⊐  S3
D0  ⊏⊐  3          26  ⊏⊐  Y0
D1  ⊏⊐  4          25  ⊏⊐  Y1
D2  ⊏⊐  5          24  ⊏⊐  Y2
D3  ⊏⊐  6          23  ⊏⊐  Y3
VCC ⊏⊐  7          22  ⊏⊐  VCC
GND ⊏⊐  8          21  ⊏⊐  GND
D4  ⊏⊐  9          20  ⊏⊐  OE
D5  ⊏⊐ 10          19  ⊏⊐  Y4
D6  ⊏⊐ 11          18  ⊏⊐  Y5
D7  ⊏⊐ 12          17  ⊏⊐  Y6
I0  ⊏⊐ 13          16  ⊏⊐  Y7
CLK ⊏⊐ 14          15  ⊏⊐  I1
```

28-pin

```
        D1  D0  S0  S1  S2  S3  Y0
         4   3   2   1  28  27  26
D2  ⊏  5                        25 ⊐ Y1
D3  ⊏  6                        24 ⊐ Y2
VCC ⊏  7          Top           23 ⊐ Y3
GND ⊏  8         View           22 ⊐ VCC
D4  ⊏  9                        21 ⊐ GND
D5  ⊏ 10                        20 ⊐ OE
D6  ⊏ 11                        19 ⊐ Y4
        12  13  14  15  16  17  18
        D7  I0  CLK  I1  Y7  Y6  Y5
```

Speed	Ceramic Flatpack (M2)	Plastic J-Lead Chip Carrier (J4)
0°C to +70°C — COMMERCIAL SCREENING		
20 ns	L29C524MC20	L29C524JC20
15 ns	L29C524MC15	L29C524JC15
−55°C to +125°C — COMMERCIAL SCREENING		
25 ns	L29C524MM25	
20 ns	L29C524MM20	
−55°C to +125°C — MIL-STD-883 COMPLIANT		
25 ns	L29C524MMB25	
20 ns	L29C524MMB20	

Pipeline Registers

5-33

L29C525 — ORDERING INFORMATION

28-pin — 0.3" wide

```
       S1  [ 1      28 ]  S2
       S0  [ 2      27 ]  S3
       D0  [ 3      26 ]  Y0
       D1  [ 4      25 ]  Y1
       D2  [ 5      24 ]  Y2
       D3  [ 6      23 ]  Y3
      Vcc  [ 7      22 ]  Vcc
      GND  [ 8      21 ]  GND
       D4  [ 9      20 ]  OE
       D5  [ 10     19 ]  Y4
       D6  [ 11     18 ]  Y5
       D7  [ 12     17 ]  Y6
       I0  [ 13     16 ]  Y7
      CLK  [ 14     15 ]  I1
```

28-pin — 0.4" wide

```
       S1  [ 1      28 ]  S2
       S0  [ 2      27 ]  S3
       D0  [ 3      26 ]  Y0
       D1  [ 4      25 ]  Y1
       D2  [ 5      24 ]  Y2
       D3  [ 6      23 ]  Y3
      Vcc  [ 7      22 ]  Vcc
      GND  [ 8      21 ]  GND
       D4  [ 9      20 ]  OE
       D5  [ 10     19 ]  Y4
       D6  [ 11     18 ]  Y5
       D7  [ 12     17 ]  Y6
       I0  [ 13     16 ]  Y7
      CLK  [ 14     15 ]  I1
```
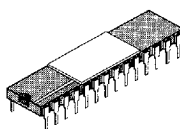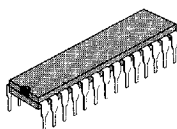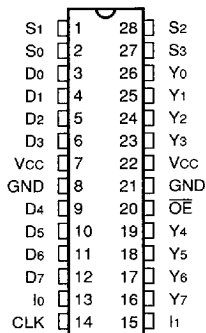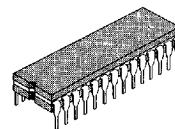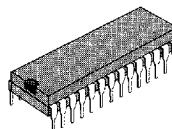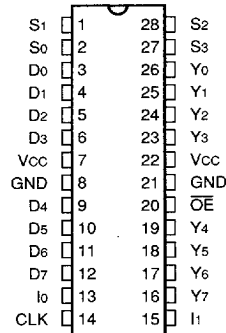
Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	Plastic DIP (P11)	Ceramic DIP (C10)
0°C to +70°C — COMMERCIAL SCREENING				
20 ns	L29C525PC20	L29C525DC20	L29C525NC20	L29C525IC20
15 ns	L29C525PC15	L29C525DC15	L29C525NC15	L29C525IC15
−55°C to +125°C — COMMERCIAL SCREENING				
25 ns		L29C525DM25		L29C525IM25
20 ns		L29C525DM20		L29C525IM20
−55°C to +125°C — MIL-STD-883 COMPLIANT				
25 ns		L29C525DMB25		L29C525IMB25
20 ns		L29C525DMB20		L29C525IMB20

Pipeline Registers

01/19/94–LDS.524/5-E

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L29C525 — ORDERING INFORMATION
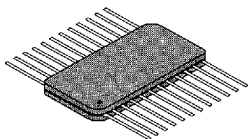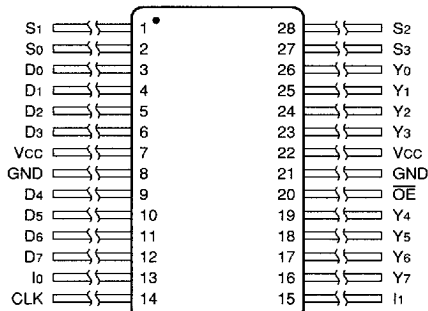
28-pin

28-pin
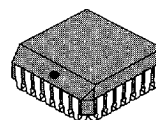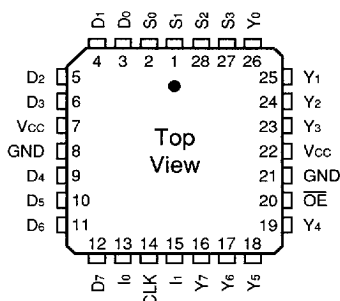
Top View

Speed	Ceramic Flatpack (M2)	Plastic J-Lead Chip Carrier (J4)
0°C to +70°C — COMMERCIAL SCREENING		
20 ns	L29C525MC20	L29C525JC20
15 ns	L29C525MC15	L29C525JC15
–55°C to +125°C — COMMERCIAL SCREENING		
25 ns	L29C525MM25	
20 ns	L29C525MM20	
–55°C to +125°C — MIL-STD-883 COMPLIANT		
25 ns	L29C525MMB25	
20 ns	L29C525MMB20	

Pipeline Registers

01/19/94–LDS.524/5-E

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