Features

- High Speed - 150 ps Gate Delay
  - 2 Input NAND, FO=2 (nominal)
- Up to 3.6 Million Used Gates and 1,024 Pins
- System Level Integration Technology
  - ARM7TDMI™ and AV*R*™ RISC Microcontrollers
  - OakDSP™ and Lode™ DSP Cores
  - 10T/100 Ethernet, USB and PCI Cores
  - SRAM, ROM, CAM and FIFO; Gate Level or Embedded
- I/O Interfaces; CMOS, LVTTL, PCI, USB
  - Output Currents up to 20 mA
  - 5V Tolerant I/O
- Deep Submicron CAD Flow

Description

The ATL35/ATLS35 Series Gate Array and Embedded Array families from Atmel are fabricated in a 0.35µ CMOS process, with up to 4 levels of metal. This family features arrays with up to 3.6 million routable gates and 1,024 pins. The high density and high pin count capabilities of the ATL35 family, coupled with the ability to embed microcontroller cores, or DSP engines, or memory, or all three together on the same silicon, makes the ATL35/ATLS35 series of arrays an ideal choice for System Level Integration.

ATLS35 Array Organization

Device Number	4LM Routable Gates	3LM Routable Gates	Max Pin Count	Max I/O Count	Gate[1] Speed
ATLS35/80	24,418	21,705	80	72	150ps
ATLS35/100	39,698	35,287	100	92	150ps
ATLS35/120	55,276	48,773	120	112	150ps
ATLS35/144	80,620	71,136	144	136	150ps
ATLS35/160	100,461	88,642	160	152	150ps
ATLS35/208	173,063	152,703	208	200	150ps
ATLS35/225	189,764	168,043	228	220	150ps
ATLS35/256	249,682	218,472	256	248	150ps
ATLS35/316	383,907	335,919	316	308	150ps
ATLS35/352	448,768	388,932	352	344	150ps
ATLS35/388	547,816	474,774	388	380	150ps
ATLS35/432	680,580	589,836	432	424	150ps
ATLS35/500	855,231	733,055	500	492	150ps
ATLS35/600	1,237,072	1,060,347	600	592	150ps
ATLS35/740	1,888,494	1,618,709	740	732	150ps
ATLS35/860	2,554,602	2,189,657	860	852	150ps
ATLS35/1,024	3,631,358	3,112,596	1,024	992	150ps

Note: 1. Nominal 2 Input NAND Gate FO=2 at 3.3 volts

ATL35 and ATLS35 Series Gate Arrays/ Embedded Arrays

Preliminary

0802B–7/97

ATL35 Array Organization

Device Number	4LM Routable Gates	3LM Routable Gates	Max Pin Count	Max I/O Count	Gate[1] Speed
ATL35/5	6,219	5,528	44	36	150ps
ATL35/18	19,846	17,641	68	60	150ps
ATL35/30	33,534	29,808	84	76	150ps
ATL35/45	50,340	44,745	100	92	150ps
ATL35/65	72,277	63,774	120	112	150ps
ATL35/95	108,885	96,049	144	136	150ps
ATL35/120	137,017	120,897	160	152	150ps
ATL35/165	185,971	164,092	184	176	150ps
ATL35/200	228,129	199,682	208	200	150ps
ATL35/240	277,635	242,931	228	220	150ps
ATL35/310	354,450	310,143	256	248	150ps
ATL35/440	508,491	444,929	304	296	150ps
ATL35/560	647,329	561,018	352	344	150ps
ATL35/690	793,591	687,779	388	380	150ps
ATL35/860	989,820	857,884	432	424	150ps
ATL35/1100	1,251,753	1,084,853	484	476	150ps
ATL35/1560	1,817,373	1,557,748	600	592	150ps
ATL35/2100	2,489,906	2,134,205	700	692	150ps
ATL35/3000	3,404,139	2,917,883	816	808	150ps

Note: 1. Nominal 2 Input NAND Gate FO=2 at 3.3 volts

Design

Design Systems Supported

Atmel supports several major software systems for design with complete macro cell libraries, as well as utilities for checking the netlist and accurate pre-route delay simulations. Cadence™ Verilog-XL™ is Atmel's golden simulator. Mentor™ QuickSim II™ and Synopsys VSS™ are sign-off level simulators. The following design systems are supported:

- Cadence™ LogicDesign Planner
- Synopsys™
- Mentor™
- Exemplar™
- Viewlogic ™ Motive
- Veribest™
- Sunrise™
- Model Tech™

Design Flow and Tools

Atmel's design flow for digital ASICs is structured to allow the ASIC designer to consolidate the greatest number of system components possible onto the same silicon chip, using available third party design tools. Atmel's cell library reflects silicon performance over extremes of temperature, voltage, and process, and includes the effects of metal loading, inter-level capacitance, and edge rise and fall times. The Design Flow includes clock tree synthesis to customer specified skew and latency goals. RC extraction is performed on final design databases and incorporated into the timing analysis.

The **Typical Gate Array/Embedded Array Design Flow**, shown on page 4, provides a pictorial description of the typical interaction between Atmel's ASIC design staff and the customer. Atmel will deliver VITAL libraries to support the customer's synthesis, verification, floorplanning, and SCAN insertion activities. Tools such as Synopsys™, Cadence™, Verilog-HDL™, CTgen™, Exemplar™, PathMILL™ and TimeMILL™ are used, and many others are available. Should a design include embedded memory

Design Flow and Tools (Continued)

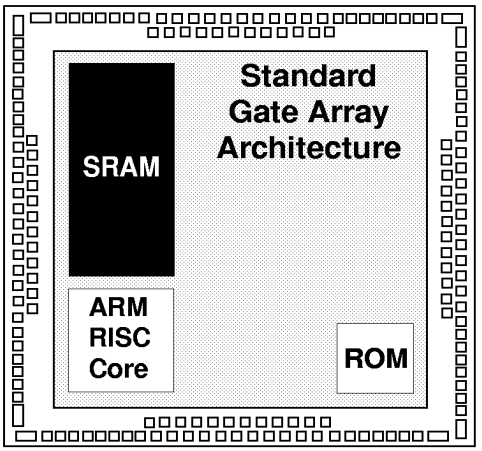
(SRAM, ROM or CAM) or an embedded core, Atmel will support a design review with the customer. The purpose of the design review is to permit Atmel to understand the partition of the ASIC, and define the location of the memory blocks and / or cores so that an underlayer layout model can be created.

Automated Test Pattern Generation (ATPG) is performed on the SCAN paths using Synopsys™ or Sunrise™ tools. Following a Preliminary Design Review, the design is routed, using tools such as Cadence DSM™, and post-route RC data is extracted, using the Arcadia™ tool. Following post-route verification and a Final Design Review, the design is taped out for fabrication.

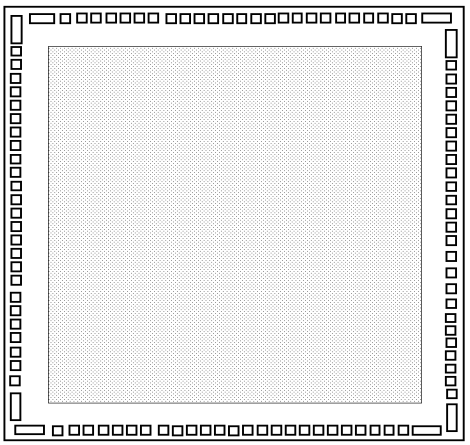
Pin Definition Requirements

Within the Physical Design Step (i.e., layout) certain restrictions apply during pin definition. The ATL35 corner pins are reserved for Power and Ground only. All other buffer pins are fully programmable as Input, Output, Bidirectional, Clock-into-Array, Power, or Ground. The corner pins for the ATLS35 are not reserved for Power and Ground, but are fully programmable.

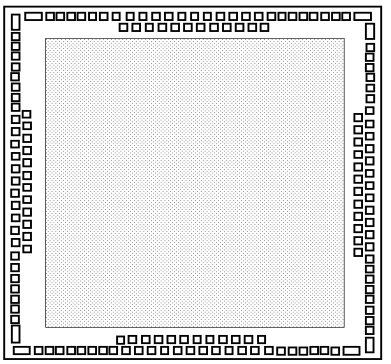
When implementing a design with 5V tolerant buffers, one buffer site must be reserved for the V_{DD5} pin, which is used to distribute power to the buffers.



Embedded Array

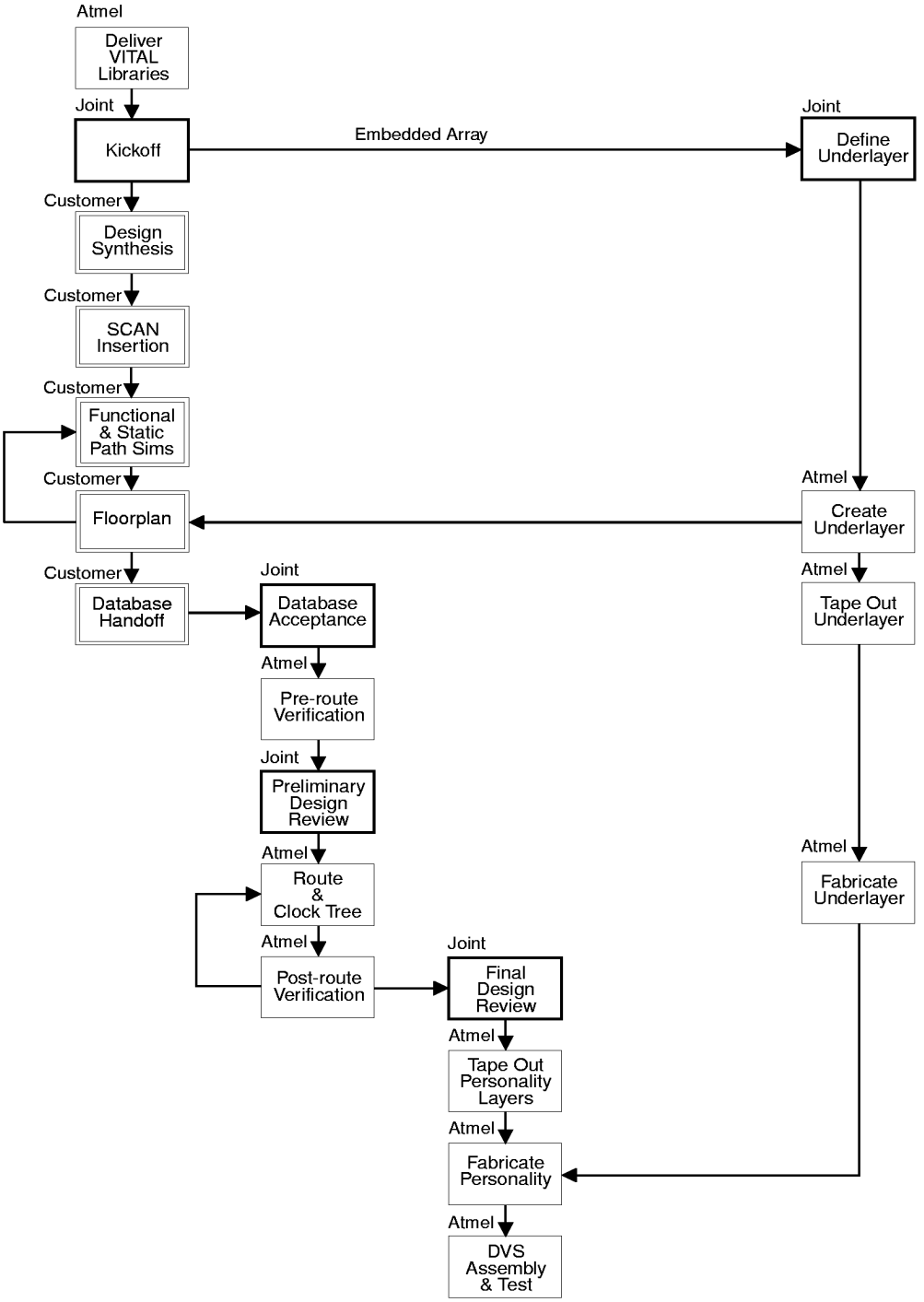


Gate Array



Staggered Array

Typical Gate Array / Embedded Array Design Flow



Design Options

VHDL/Verilog-HDL

Atmel can accept Register Transfer Level (RTL) designs for VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL™ format. Atmel fully supports Synopsys for VHDL™ simulation as well as synthesis. VHDL or Verilog-HDL is Atmel's preferred method of performing a gate array design.

ASIC Design Translation

Atmel has successfully translated dozens of existing designs from most major ASIC vendors (LSI Logic™, Motorola™, SMOS™, Oki™, NEC™, Fujitsu™, AMI™ and others) into our gate arrays. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

Schematic Capture

The schematic capture method of design is performed by the customer using an Atmel provided macro cell library. A complete netlist and vector set must then be provided to Atmel. Upon acceptance of this data set, Atmel continues with the standard design flow.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx™, Actel™, Altera™, AMD™ and Atmel) into our gate arrays. There are four primary reasons to convert from an FPGA/PLD to a gate array. Conversion of high volume devices (over 10,000 units) for a single or combined design is cost effective. Performance can often be optimized for speed or power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, a gate array may provide a lower cost answer for long-term volume production.

Macro Cores

AVR (8-bit RISC) Microcontroller (8515)

The AVR RISC Microcontroller is a true 8-bit RISC Architecture, ideally suited for embedded control applications. The AVR is offered as a gate level, soft macro in the ATL35 family.

The AVR supports a powerful set of 120 instructions. The AVR pre-fetches an instruction during prior instruction execution, enabling the execution of one instruction per clock cycle.

The Fast Access RISC register file consists of 32 general purpose working registers. These 32 registers eliminate the data transfer delay in the traditional program code intensive accumulator architectures.

The AVR can incorporate up to 8k x 8 program memory (ROM) and 64k x 8 data memory (SRAM). Also included are several optional peripherals: UART, 8 bit timer/counter, 16 bit timer/counter, external and internal interrupts and programmable watchdog timer.

ARM7TDMI Embedded Microcontroller Core

The ARM7TDMI (Advanced RISC Machines) is a powerful 32-bit processor offered as an embedded core in the ATL35 series arrays.

The ARM7TDMI is a member of the Advanced RISC Machines (ARM) family of general purpose 32-bit microprocessors, which offer high performance for very low power consumption.

The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective chip.

Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM memory interface has been designed to allow the performance potential to be realized without incurring high costs in the memory system. Speed critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals facilitate the exploitation of the fast local access modes offered by industry standard dynamic RAMs.

The ARM7TDMI core includes several optional peripheral macros. The options offered are Real Time Clock, DMA Controller, USART, External Bus Interface, Interrupt, Timer and Advanced Power Management and Controller.

OakDSPCore

Atmel's embedded OakDSPCore is a 16-bit, general-purpose low-power, low-voltage and high-speed Digital Signal Processor (DSP).

OAK is designed for mid-to-high-end telecommunications and consumer electronics applications, where low-power and portability are major requirements. Among the applications supported are digital cellular telephones, fast modems, advanced facsimile machines and hard disk drives.OAK is available as a DSP core in Atmel's Gate Array cell library, to be utilized as an engine for DSP-based ASICs. It is specified with several levels of modularity in SRAM, ROM, I/O blocks, allowing efficient DSP-based ASIC development.

OAK is aimed at achieving the best cost-performance factor for a given (small) silicon area. As a key element of a system-on-chip, it takes into account such requirements as program size, data memory size, glue logic, power management, etc.

The OAK core consists of three main execution units operating in parallel: the Computation/Bit Manipulation Unit (CBU), the Data Addressing Arithmetic Unit (DAAU) and the Program Control Unit (PCU).

The Core also contains ROM and SRAM addressing units, and Program Control Logic (PCL). All other peripheral blocks, which are application specific, are defined as part of the user-specific logic, implemented around the DSP core on the same silicon die.

OAK has an enhanced set of DSP and general microprocessor functions to meet the application requirements. The OAK programming model and instruction set are aimed at straightforward generation of efficient and compact code.

Lode DSP Core

The LODE DSP Core is offered in the ATL35 series arrays as an embedded core. Lode is an advanced, 16-bit Digital Signal Processor (DSP) core designed for optimal performance in digital cellular, speech and voice communications applications. The Lode core architecture efficiently performs the baseband functions - speech compression, forward error correction, and modem functions - required by digital cellular standards. Lode is the first general-purpose DSP that provides two multiplier-accumulators (MACs) that reduce power consumption by effectively cutting cycle times in half. Lode's suite of user-friendly development tools are easy to learn, thus accelerating the time it takes to get your product to market.

ATL35 Series Cell Library

Atmel's ATL35 Series gate arrays make use of an extensive library of macro cell structures, including logic cells, buffers and inverters, multiplexers, decoders, and I/O options. Soft macros are also available.

The ATL35 Series PLL operates at frequencies of up to 250 MHz with minimal phase error and jitter, making it ideal for frequency synthesis of high speed on-chip clocks and chip to chip synchronization. Output buffers are programmable to meet the voltage and current requirements of PCI (20mA). These cells are well characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test arrays. Characterization is performed over the rated temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Cell Index

Signal Name	Description	Site Count
ADD3X	1 bit full adder with buffered outputs	10
AND2	2 input AND	2
AND2H	2 input AND - high drive	3
AND3	3 input AND	3
AND3H	3 input AND - high drive	4
AND4	4 input AND	3
AND4H	4 input AND - high drive	4
AND5	5 input AND	5
AOI22	2 input AND into 2 input NOR	2
AOI22H	2 input AND into 2 input NOR - high drive	4
AOI222	Two, 2 input ANDs into 2 input NOR	2
AOI222H	Two, 2 input ANDs into 2 input NOR - high drive	4
AOI2223	Three, 2 input ANDs into 3 input NOR	4
AOI2223H	Three, 2 input ANDs into 3 input NOR - high drive	8
AOI23	2 input AND into 3 input NOR	3
BUF1	1x buffer	2
BUF2	2x buffer	2
BUF2T	2x Tri State bus driver with active high enable	4
BUF2Z	2x Tri State bus driver with active low enable	4
BUF3	3x buffer	3
BUF4	4x buffer	3
BUF4T	4x Tri-State bus driver with active high enable	6
BUF8	8x buffer	5
BUF8T	8x Tri-State bus driver with active high enable	10
BUF12	12x buffer	8
BUF16	16x buffer	10
CLA7X	7 input carry lookahead	5
DEC4	2:4 decoder	8
DEC4N	2:4 decoder with active low enable	10

Cell Index

Signal Name	Description	Site Count
DEC8N	3:8 decoder with active low enable	22
DFF	D flip-flop	8
DFFBCPX	D flip-flop with asynchronous clear and preset with complementary outputs	16
DFFBSRX	D flip-flop with asynchronous set and reset with complementary outputs	16
DFFC	D flip flop with asynchronous clear	9
DFFR	D flip-flop with asynchronous reset	10
DFFRQ	Quad D flip-flop with asynchronous reset	40
DFFS	D flip-flop with asynchronous set	9
DFFSR	D flip-flop with asynchronous set and reset	11
DLY1500	Delay buffer 1.5 ns	7
DLY2000	Delay buffer 2.1 ns	9
DLY3000	Delay buffer 3.0 ns	11
DLY6000	Delay buffer 6.0 ns	20
DSS	Set scan flip-flop	12
DSSQ	Quad Set scan D flip-flop	36
DSSBCPY	Set scan flip-flop with clear and preset	16
DSSBR	Set scan flip-flop with reset	14
DSSBS	Set scan flip-flop with set	14
DSSR	Set scan D flip-flop with reset	12
DSSRQ	Quad Set Scan D Flip Flop with reset	48
DSSS	Set scan D flip-flop with set	14
DSSSR	Set scan D flip-flop with set and reset	16
HLD1	Bus hold cell	4
INV1	1x inverter	1
INV2	2x inverter	1
INV2T	2x Tri State inverter with active high enable	3
INV3	3x inverter	2
INV4	4x inverter	2
INV8	8x inverter	4
INV10	10x inverter	8
INV1D	Dual 1x inverter	2
INV1Q	Quad 1x inverter	4
INV1TQ	Quad 1x Tri State inverter with active high enable	8
JKF	JK flip-flop	10

Cell Index

Signal Name	Description	Site Count
JKFBCPX	Clear preset JK flip-flop with asynchronous clear and preset and complementary outputs	16
JKFC	JK flip-flop with asynchronous clear	12
LAT	LATCH	6
LATB	LATCH with complementary outputs	6
LATBG	LATCH with complementary outputs and inverted gate signal	6
LATBH	LATCH with high drive complementary outputs	7
LATIQ	Quad Latch	20
LATR	LATCH with reset	5
LATS	LATCH with set	6
LATSR	LATCH with set and reset	8
MUX2	2:1 MUX	4
MUX2H	2:1 MUX - high drive	5
MUX2I	2:1 MUX with inverted output	3
MUX2IH	2:1 MUX with inverted output - high drive	4
MUX2N	2:1 MUX with active low enable	5
MUX2NQ	Quad 2:1 MUX with active low enable	18
MUX2Q	Quad 2:1 MUX	16
MUX3I	3:1 MUX with inverted output	6
MUX3IH	3:1 MUX with inverted output - high drive	8
MUX4	4:1 MUX	10
MUX4X	4:1 MUX with transmission gate data inputs	9
MUX4XH	4:1 MUX with transmission gate data inputs - high drive	10
MUX5H	5:1 MUX - high drive	14
MUX8	8:1 MUX	20
MUX8N	8:1 MUX with active low enable	20
MUX8XH	8:1 MUX with transmission gate data inputs - high drive	16
NAN2	2 input NAND	2
NAN2D	Dual 2 input NAND	3
NAN2H	2 input NAND - high drive	2
NAN3	3 input NAND	2
NAN3H	3 input NAND - high drive	3
NAN4	4 input NAND	3
NAN4H	4 input NAND - high drive	4
NAN5	5 input NAND	5
NAN5S	5 input NAND with set	3
NAN5H	5 input NAND - high drive	6

Cell Index

Signal Name	Description	Site Count
NAN6	6 input NAND	6
NAN6H	6 input NAND - high drive	7
NAN8	8 input NAND	7
NAN8H	8 input NAND - high drive	8
NOR2	2 input NOR	2
NOR2D	Dual 2 input NOR	3
NOR2H	2 input NOR - high drive	2
NOR3	3 input NOR	2
NOR3H	3 input NOR - high drive	3
NOR4	4 input NOR	3
NOR4H	4 input NOR - high drive	5
NOR5	5 input NOR	5
NOR5S	5 input NOR with set	3
NOR8	8 input NOR	7
OAI22	2 input OR into 2 input NAND	2
OAI22H	2 input OR into 2 input NAND - high drive	4
OAI222	Two, 2 input ORs into 2 input NAND	3
OAI222H	Two, 2 input ORs into 2 input NAND - high drive	6
OAI22224	Four, 2 input ORs into 4 input NAND	8
OAI23	2 input OR into 3 input NAND	3
ORR2	2 input OR	2
ORR2H	2 input OR - high drive	3
ORR3	3 input OR	3
ORR3H	3 input OR - high drive	4
ORR4	4 input OR	3
ORR4H	4 input OR - high drive	4
ORR5	5 input OR	5
XNR2	2 input exclusive NOR	4
XNR2H	2 input exclusive NOR - high drive	4
XOR2	2 input exclusive OR	4
XOR2H	2 input exclusive OR - high drive	4

I/O Buffer Cell Index

Signal Name	Description
PBD2C	4 mA bidi CMOS buffer
PBC3C	6 mA bidi CMOS buffer
PBD5C	10 mA bidi TTL buffer with Schmitt Trigger
PBS1C	2 mA bidi CMOS buffer
PBS1CS	2 mA bidi CMOS buffer with Schmitt Trigger
PBS2C	4 mA bidi CMOS input buffer
PBS2CS	4 mA bidi CMOS input buffer with Schmitt Trigger
PBS3C	6 mA bidi CMOS buffer
PBS3CS	6 mA with Schmitt Trigger
PBS4C	8 mA bidi CMOS buffer
PBS4CS	8 mA bidi CMOS buffer with Schmitt Trigger
PBS5C	10 mA bidi CMOS buffer
PBS5CS	10 mA bidi with Schmitt Trigger
PBS6C	12 mA bidi CMOS buffer
PBS6CS	12 mA bidi Schmitt Trigger
PIC	CMOS input buffer
PICI	CMOS inverting input buffer
PICS	CMOS input buffer with Schmitt Trigger
PK6	12 mA clock driver
PO1	2 mA output buffer
PO2	4 mA output buffer
PO2B	4 mA inverting output buffer
PO3	6 mA output buffer
PO4	8 mA output buffer
PO5	10 mA output buffer
PTD2	4 mA Tri State output buffer with dual enable
PTD3	6 mA Tri State output buffer with dual enable
PTD5	10 mA Tri State output buffer with dual enable
PTS1	2 mA Tri State output buffer with single enable
PTS2	4 mA Tri State output buffer with single enable
PTS3	6 mA Tri State output buffer with single enable
PTS4	8 mA Tri State output buffer with single enable
PTS5	10 mA Tri State output buffer with single enable
PTS6	12 mA Tri State output buffer with single enable

Absolute Maximum Ratings*

Operating Ambient Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Maximum Input Voltage	
Inputs	V_{DD} +0.5V
5V tolerant	V_{DD5} +0.5V
Maximum Operating Voltage	3.6V
Maximum Junction Temperature	+150°C

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.3 Volt DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55		125	degrees C
V_{DD}	Supply Voltage	All except 5V tolerant		3.0	3.3	3.6	V
V_{DD5}	Supply Voltage	5V tolerant		4.5	5.0	5.5	V
I_{IH}	High-level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD(max)}$			5	µA
		PCI				5	
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD(max)}$, No pull up	-5			µA
		PCI		-5			
I_{OZ}	High-impedance state Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD(max)}$, No pull up	-5		5	µA
I_{OS}	Output Short-circuit Current	4mA Buffer	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD(max)}$		17		mA
		4mA Buffer	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD(max)}$		-40		
V_{IH}	High-level Input Voltage	CMOS, LVTTL		2.0			V
		PCI		0.475V_{DD}			
		TTL Level Schmitt		2.0	1.7		
		5V - tolerant		2.4	5.0	5.5	
V_{IL}	Low-level Input Voltage	CMOS				0.5	V
		PCI				0.325V_{DD}	
		TTL Level Schmitt			1.1	0.8	
V_{HYS}	Hysteresis	TTL Level Schmitt			0.6		V
V_{OH}	High-level Output Voltage	CMOS, LVTTL	I_{OH} = as rated, $V_{DD} = V_{DD(min)}$	0.7V_{DD}			V
		PCI	I_{OH} = -500uA	0.9V_{DD}			
		5V - tolerant	I_{OH} = as rated			V_{DD}-0.6	
V_{OL}	Low-level Output Voltage	CMOS	I_{OL} = as rated, $V_{DD} = V_{DD(min)}$			0.4	V
		PCI	I_{OL} = 1.5mA			0.1V_{DD}	

USB (Universal Serial Bus)

Applicable over the recommended ambient range of 0°C
$\leq T_a <$ +70°C and 3.0V$\leq V_{dd} \leq$ 3.6V

Receiver

Test	Description	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance				20	pF
I_{LO}	Hi-Z State Data Line Leakage		-10		10	µA
V_{SE}	Single Ended Receiver Threshold		0.8		2.0	V
V_{CM}	Differential Receiver Common Mode Range		0.2		2.5	V
V_{DI}	Differential Input Sensitivity		200			mV

Driver

Full Speed Mode (12Mb/s)

Test	Description	Conditions	Min	Typ	Max	Units
Z_{DRV}	Source Resistance	DC	28		43	Ohms
t_R/t_F	Rise/Fall Time	50pF	4		20	ns
t_{RFM}	Rise/Fall Matching	t_R/t_F	90		110	%
V_{CRS}	Data Line Crossover Voltage		1.3		2.0	V

Low Speed Mode (1.5Mb/s)

Test	Description	Conditions	Min	Typ	Max	Units
t_R/t_F	Rise/Fall Time	50pF	75			ns
t_R/t_F	Rise/Fall Time	350pF			300	ns
t_{RFM}	Rise/Fall Matching	t_R/t_F	80		120	%
V_{CRS}	Data Line Crossover Voltage		1.3		2.0	V

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Typ	Units
C_{IN}	Capacitance, Input Buffer (die)	3.3 V	2.4	pF
C_{OUT}	Capacitance, Output Buffer (die)	3.3 V	5.6	pF
$C_{I/O}$	Capacitance, Bi-Directional	3.3 V	6.6	pF

Testability Techniques

For complex designs, involving blocks of memory and / or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs and the number of functional vectors that would need to be created to exercise them fully strongly suggests the use of more efficient techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and Atmel the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, a microcontroller or DSP engine or both, SRAM to support the microcontroller or DSP engine, and glue logic to support the interconnectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high performance digital tester. Combinations of parametric, functional, and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and / or parametric testing can be performed. Since a digital tester must control all the clocks during the testing of an ASIC, provision must be made for the VCO to be bypassed. Atmel's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test, without impinging upon the normal functionality.

In a similar vein, access to microcontroller, DSP, and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. The AVR and ARM microcontrollers support SCAN testing, as do the three main execution units of the Oak DSP. SRAM and CAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins provides a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that, in almost all of these cases, the purpose of the testability technique is to provide Atmel a means to assess the structural integrity of an ASIC, i.e., sort devices with manufacturing-induced defects. All of the techniques described above should be considered supplemental to a set of patterns which exercise the functionality of the design in its anticipated operating modes.

Advanced Packaging

The ATL35 Series gate arrays are offered in a wide variety of standard packages, including plastic and ceramic quad flatpacks, thin quad flatpacks, ceramic pin grid arrays, and ball grid arrays. High volume onshore and offshore contractors provide assembly and test for commercial product, with prototype capability in Colorado Springs. Custom package designs are also available as required to meet a customer's specific needs, and are supported through Atmel's package design center. When a standard package cannot meet a customer's need, a package can be designed to precisely fit the application and to maintain the performance obtained in silicon. Atmel has delivered custom-designed packages in a wide variety of configurations.

Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 256, 304
TQFP	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391, 447
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
BGA	121, 169, 225, 313, 352, 388
Power Quad	144, 160, 208, 240, 304
Super BGA	168, 204, 240, 256, 304, 352, 432, 560, 600