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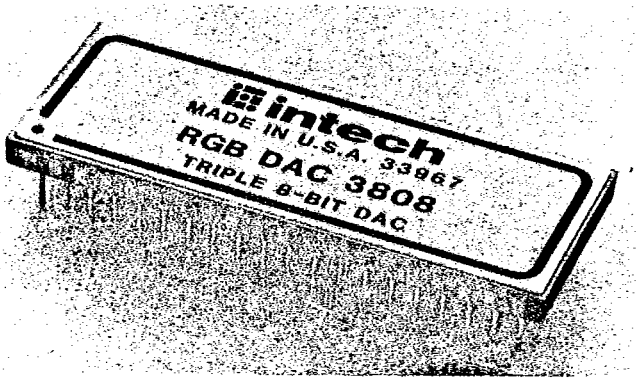
ADVANCED ANALOG

RGB DAC 3808

CMOS, TRIPLE, 8-BIT COLOR MAPPED VIDEO DAC



DESCRIPTION

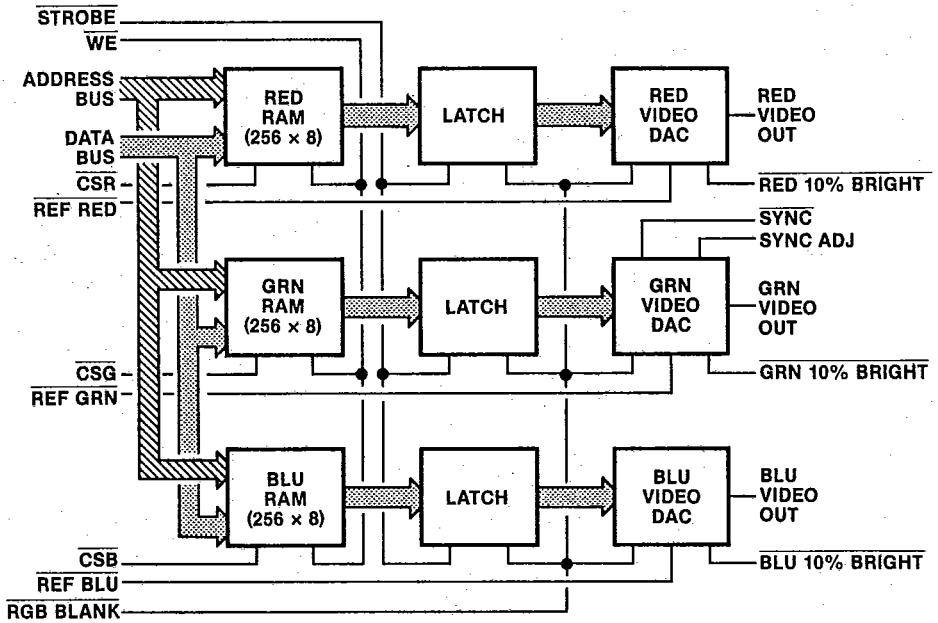
This hybrid digital-to-analog converter provides 3 channels of video output for RGB-type video displays with picture element (pixel) rates to 40 MHz. The RGB DAC contains 3 video DAC's and 3 RAM arrays (256 × 8).

The RGB DAC 3808 provides 8-BITs of resolution or 256 levels of "gray scale" per channel. This gives the user a (2^{24}) or 16.7 million color palette. The 256 × 8 RAM array per channel allows the user a choice of any 256 of the 16.7 million colors for each sweep. The write speed is also high enough to allow the color map to be updated during the vertical retrace or even horizontal retrace in some systems. The high update rates and the ability to generate 0.6 volt video output across a 75 ohm load makes this DAC ideally suited for color computer graphics using raster scan technology.

FEATURES

- LOW POWER CMOS CIRCUITRY
- 16.7 MILLION COLOR PALETTE
- 3 VIDEO DACs
- 3 RAMs (256 × 8) FOR COLOR MAP
- UPDATE RATES TO 40 MHz
- COMPOSITE BLANKING SIGNALS
- TTL, CMOS COMPATIBLE INPUTS
- 75 OHM RGB OUTPUTS
- CLEAN OUTPUTS (DE-GLITCHING NOT REQUIRED)
- SINGLE 5V SUPPLY OPERATION
- 40 PIN DIP PACKAGE

BLOCK DIAGRAM



SPECIFICATIONS

(Typical @ +25°C, +5V and 75Ω load unless otherwise stated)

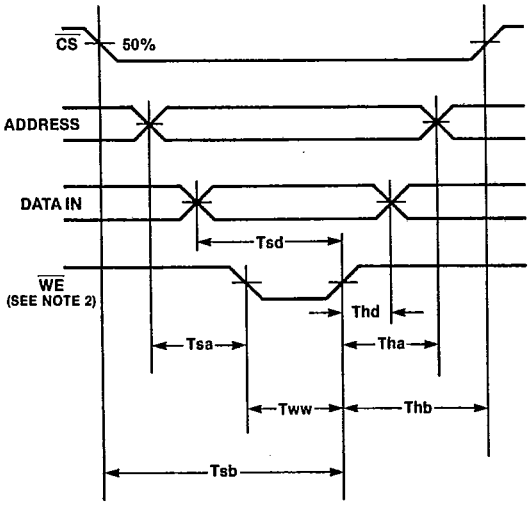
RESOLUTION	8 BITs
PALLETTE	
(256 colors per sweep)	16.7 million
ANALOG OUTPUTS	
(each channel)	
Voltage Range (±5%)	0 to 1.04
Current	8 mA
Short Circuit Current	17 mA
Impedance (±0.1%)	75Ω
Compliance	±1.5V
VIDEO OUTPUT LEVEL	0 to 0.06375 V
BLANKING OUTPUT LEVEL	
(Referred to Black Level) ±5%	−53 mV
SYNC OUTPUT LEVEL	
(Referred to Blanking Level)	−280 mV
10% BRIGHT LEVEL	+70 mV
ACCURACY	
(each channel)	
Channel to Channel Gain Difference	±1 LSB
Absolute Accuracy	±1.6 LSB
Differential Linearity	±1 LSB
Offset	±1.0 mV
Offset Tempco	±10 ppm/°C
Gain Tempco	±200 ppm/°C
Linearity Tempco	±100 ppm/°C
PSRR	±0.2%/%
DYNAMIC CHARACTERISTICS	
(each DAC)	
Settling Time (to 1 LSB)	10 ns
Update Rate (min)	40 MHz
Rise Time	5 ns
Slew Rate	100V/μs

DATA and ADDRESS INPUTS	
Compatibility	TTL, CMOS
Coding	BIN
CONTROL INPUTS	
(see timing diagram)	
$\overline{\text{STROBE}}$	
Compatibility	TTL, CMOS
Set-up Time (max)	35 ns
Hold Time	0 ns
Update Rate	40 MHz
Propagation (max)	20 ns
Width (min)	10 ns
COMPOSITE $\overline{\text{BLANKING}}$, $\overline{\text{SYNC}}$	
Compatibility	TTL, CMOS
Settling Time	10 ns
Set-up Time (max)	10 ns
Propagation Time (max)	20 ns
DYNAMIC CHARACTERISTICS	
(each RAM)	
Width of Write Pulse (Tww) (min)	20 ns
Address Before Write Pulse (Tsa) (min)	0 ns
Data Set-up Time (Tsd)	20 ns
CS Set-up Time (Tsb)	20 ns
Address Hold Time (Tha)	0 ns
Data Hold Time (Thd)	0 ns
Chip Select Hold Time (Thb)	0 ns
Address Access Time (Taa)(max)	25 ns
Chip Select Access Time (Tab)	20 ns
(with valid address)	
POWER REQUIREMENTS	
Voltage	+4.5 to +5.5V
Current	350 mA typ
	455 mA max
TEMPERATURE RANGE	
Ambient	0° to +70°C*

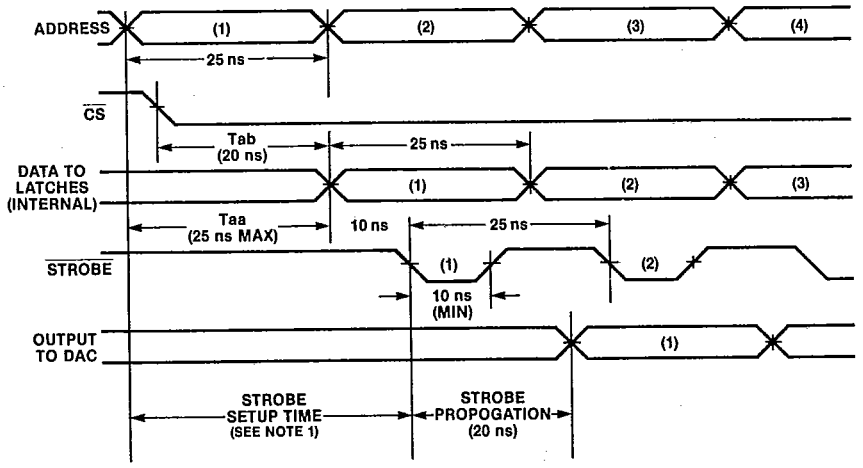
* −55°C to +125°C Ranges Available

TIMING DIAGRAM

WRITE CYCLE



READ CYCLE
(40 MHz PIXEL RATE)



NOTES: 1. Time from stable "Ready Address" to Strobe *HI* to *LO* Transition.
2. Data and Address must be stable during *LO* to *HI* Write Enable Transition.

PIN DESCRIPTIONS

$\overline{\text{STROBE}}$

The transition from logic "1" to logic "0" transfers data from RAM outputs to the Data Register outputs. The strobe is not used for write operations.

$\overline{\text{RGB BLANK}}$

A logic "0" sets the registers to all "0's" and drives all the outputs to a level 53 mV below Ref Black. This signal has priority over the data inputs and is used to shut off the beam for the darkest display possible. Blanking is synchronous with Strobe.

ADDRESS (A_0-A_7)

These inputs are used to select the RAM locations for both the Read and Write operations. In the Write mode these inputs are used to select the location where display pixel color and brightness data is to be stored. In the Read mode they serve as data inputs in that a particular pixel's parameters may be chosen by merely addressing the RAM location where the data for that parameter is stored, and clocking it into the DAC.

DATA (D_0-D_7)

These inputs are used to load display color data into the RAM arrays. The data will be transferred to the DAC inputs, as required, during the read cycle in the same polarity in which it was loaded into the RAMs.

$\overline{\text{SYNC}}$

When enabled (Sync Adj. open) a logic "0" on this input activates the sync function which sets the inputs to the DACs, on all three channels, to all "0's", thereby driving their outputs to Reference Black. In addition it drives the output on the green channel to a level 286 mV more negative than the reference black level. When combined with an active blanking signal the output of all three channels will be driven to 0.0 volts, as shown in the Composite Video Waveforms.

SYNC ADJ

This input should be left open to enable the 286 mV sync level feature of the Green Output. If this feature is not desired this input should be connected to ground. This is not a digital input.

VIDEO OUTPUTS

These are the outputs of the DACs in each channel. They control the CRT display color and brightness in an RGB type color graphics sytem. A separate output is provided for each gun (red, green, and blue) in the CRT. Each of the output waveforms contain the video signals plus a composite blanking level in accordance with the Composite Video Waveforms. In addition the Green Output will supply a composite sync signal which is used to trigger the retrace cycles in the CRT's beam sweep circuitry.

The DAC outputs have been designed to provide a clean signal, free from excessive switching spikes, and no additional deglitching circuitry is required. Its output circuitry will develop a full output across a 75 ohm load which is sufficient to drive the inputs of most CRT video amplifiers directly.

$\overline{\text{WE}}$

Logic "1" selects Read operation.
Logic "0' selects Write operation.
Pixel color data will be "clocked" into the RAMS of any channel with a *LO* on its Chip Select input during a logic "0" to logic "1" transition on the $\overline{\text{WE}}$ input. The outputs of the DACs will not be affected during this time (they will retain the least read output provided no strobe or blanking signal is applied).

$\overline{\text{CSR}}$, $\overline{\text{CSG}}$, $\overline{\text{CSB}}$

These pins provide access control to the RAM arrays in each of the "Red", "Green" and "Blue" channels. A particular channel is activated when a logic "0" is applied to its channel select input. Normally only one channel is selected at a time for writing data into the RAMs, but all three inputs are held at logic "0" throughout the entire read cycle. If a logic "1" is applied to these inputs the data at the inputs to the DAC registers will be undefined, however, if no strobe signal is applied during this time the DAC outputs will retain the last "Read" output level unless a blanking signal is applied. If no blanking signal is applied and these inputs are held at logic "1" during a strobe pulse the DAC outputs will be unpredictable.

$\overline{\text{REF RED}}$, $\overline{\text{GRN}}$, $\overline{\text{BLU}}$

These inputs provide a convenient way to force the output of the DACs to go to their "Ref-White" level. A logic "0" at these inputs will override the digital data inputs and cause the output to go to its full-scale value.

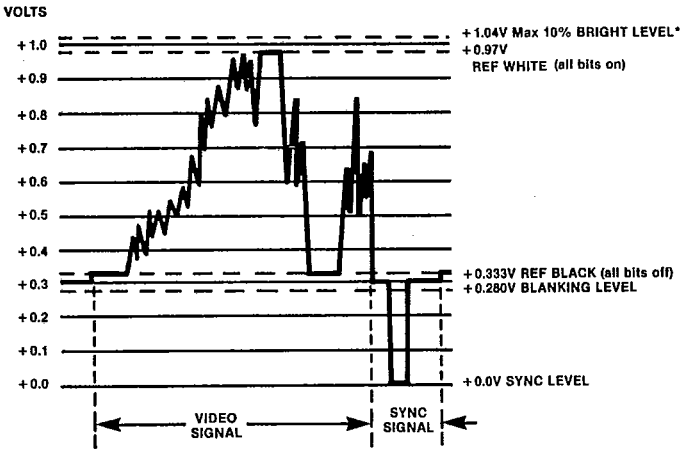
Any one of seven colors, of full intensity, may be generated by using combinations of these inputs. A logic "0" at all inputs simultaneously will generate white pixels at full intensity. These inputs are asynchronous and, for the best results, should be synchronized with the $\overline{\text{STROBE}}$ signal then latched externally.

$\overline{\text{RED}}$, $\overline{\text{GRN}}$, $\overline{\text{BLU}}$ 10% BRIGHT

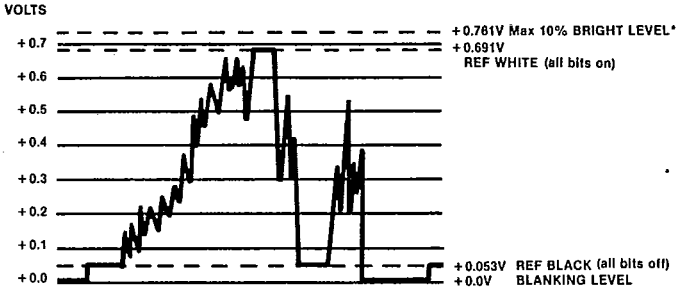
These inputs provide a convenient way to add 10% to the DACs output. A logic "0" at these inputs will increase the DACs output by 70 mV, thus facilitating word or cursor highlighting.

COMPOSITE VIDEO WAVEFORMS

GREEN OUTPUT
(SYNC ENABLED and 10% BRIGHT OFF*)

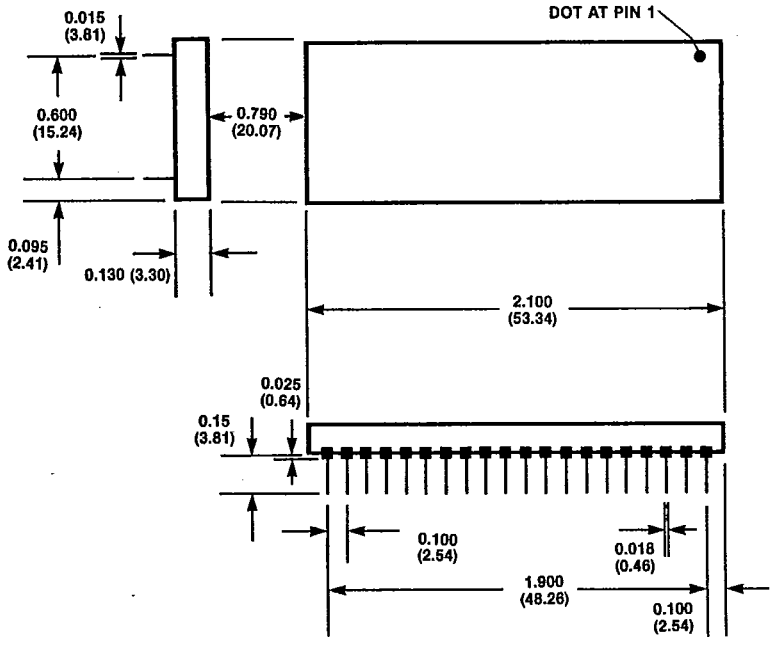


RED & BLUE OUTPUT
(OR GRN OUT with NO SYNC, 10% BRIGHT OFF*)

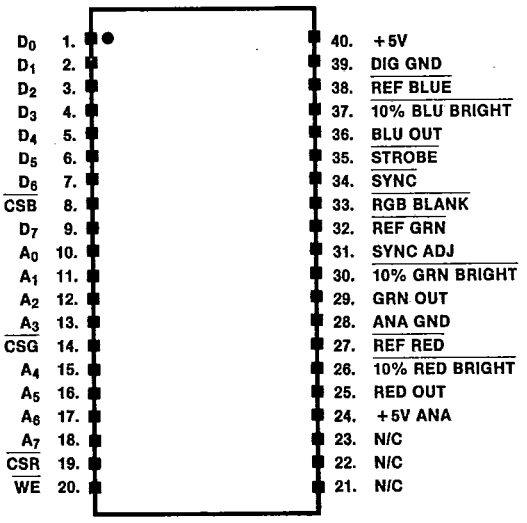


*An active $\overline{\text{10\% BRIGHT}}$ signal on any channel will cause the output level of that channel to go 70 mV more positive regardless of the status of other input signals or output level. The maximum 10% Bright levels shown are with all bits on and the 10% Bright input on.

MECHANICAL OUTLINE



PIN DESIGNATION



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