288Mb CIO Reduced Latency (RLDRAM® II)

MT49H8M36
MT49H16M18
MT49H32M9

For the latest data sheet, refer to Micron's Web site: www.micron.com/rldram

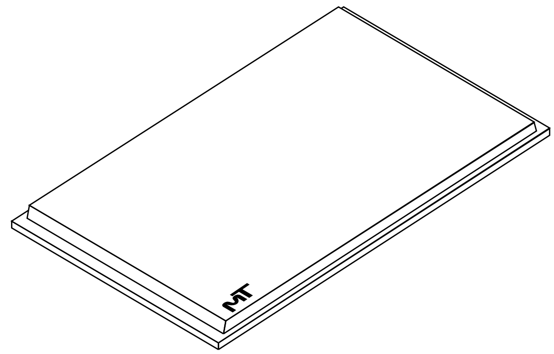
Features

- 400 MHz DDR operation (800 Mb/s/pin data rate)
- Organization
  8 Meg x 36, 16 Meg x 18, and 32 Meg x 9
  8 banks
- Cyclic bank switching for maximum bandwidth
- Reduced cycle time (20ns at 400 MHz)
- Nonmultiplexed addresses (address multiplexing option available)
- SRAM-type interface
- Programmable READ latency (RL), row cycle time, and burst sequence length
- Balanced READ and WRITE latencies in order to optimize data bus utilization
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Differential input data clocks (DKx, DKx#)
- On-chip DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32ms refresh (8K refresh for each bank; 64K refresh command must be issued in total each 32ms)
- 144-ball µBGA package
- HSTL I/O (1.5V or 1.8V nominal)
- 25Ω–60Ω matched impedance outputs
- 2.5V VEXT, 1.8V VDD, 1.5V or 1.8V VDDQ I/O
- On-die termination (ODT) RTT

Table 1: Valid Part Numbers

Part Number	Description
MT49H8M36FM-xx	8 Meg x 36 RLDRAM II
MT49H16M18FM-xx	16 Meg x 18 RLDRAM II
MT49H32M9FM-xx	32 Meg x 9 RLDRAM II

Figure 1: 144-Ball µBGA



Options — Marking

Options	Marking
• Clock cycle timing	
2.5ns (400 MHz)	-25
3.3ns (300 MHz)	-33
5ns (200 MHz)	-5
• Configuration	
8 Meg x 36	MT49H8M36
16 Meg x 18	MT49H16M18
32 Meg x 9	MT49H32M9
• Operating temperature range	
Commercial 0° to +95°C	None
Industrial T_C = -40°C to +95°C T_A = -40°C to 85°C)	IT
• Package	
144-ball µBGA	FM
(11mm x 18.5mm, lead-free)	BM[1]

Notes: 1. Contact Micron for availability of lead-free products.

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General Description

The Micron® 288Mb reduced latency DRAM (RLDRAM®) II is a high-speed memory device designed for high bandwidth communication data storage—telecommunications, networking, and cache applications, etc. The chip's 8-bank architecture is optimized for high speed and achieves a peak bandwidth of 28.8 Gb/s, using a 36-bit interface and a maximum system clock of 400 MHz.

The double data rate (DDR) interface transfers two 36-, 18-, or 9-bit wide data word per clock cycle at the I/O pins. Output data is referenced to the free-running output data clock.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock(s).

Read and write accesses to the RLDRAM are burst-oriented. The burst length is programmable from 2, 4, or 8[1] by setting the mode register.

The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

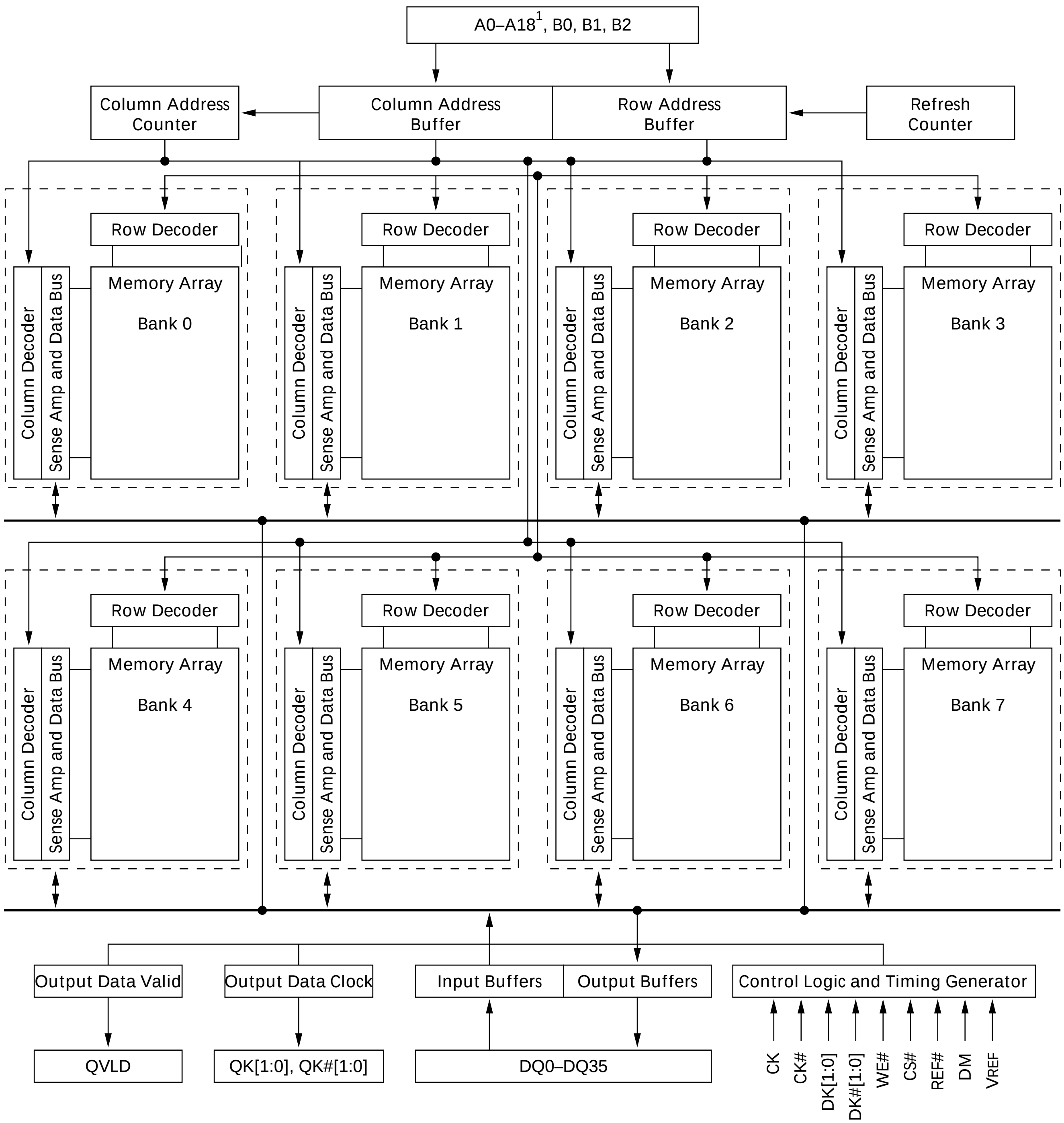
Bank-scheduled refresh is supported with row address generated internally.

A standard µBGA 144-ball package is used to enable ultra high-speed data transfer rates and a simple upgrade path from former products.

Notes: 1. Burst of 8 on x18 and x9 devices only.

Functional Block Diagram

Figure 2: 8 Meg x 36



Notes: 1. When the BL = 4 setting is used, A18 is a “Don’t Care.“

Ball Assignment and Description

Table 2: 8 Meg x 36 Ball Assignment (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DQ8	DQ9	VSSQ					VSSQ	DQ1	DQ0	VDD
C	VTT	DQ10	DQ11	VDDQ					VDDQ	DQ3	DQ2	VTT
D	(A22)[1]	DQ12	DQ13	VSSQ					VSSQ	QK0#	QK0	VSS
E	(A21)[2]	DQ14	DQ15	VDDQ					VDDQ	DQ5	DQ4	(A20)[2]
F	A5	DQ16	DQ17	VSSQ					VSSQ	DQ7	DQ6	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSS	A4	A3
J	DK0	DK0#	VDD	VDD					VDD	VDD	B0	CK
K	DK1	DK1#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DQ24	DQ25	VSSQ					VSSQ	DQ35	DQ34	(A19)[2]
P	A15	DQ22	DQ23	VDDQ					VDDQ	DQ33	DQ32	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	DQ31	DQ30	VSS
T	VTT	DQ20	DQ21	VDDQ					VDDQ	DQ29	DQ28	VTT
U	VDD	DQ18	DQ19	VSSQ					VSSQ	DQ27	DQ26	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

Notes: 1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.

Table 3: 16 Meg x 18 Ball Assignment (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DNU[4]	DQ4	VSSQ					VSSQ	DQ0	DNU[4]	VDD
C	VTT	DNU[4]	DQ5	VDDQ					VDDQ	DQ1	DNU[4]	VTT
D	(A22)[1]	DNU[4]	DQ6	VSSQ					VSSQ	QK0#	QK0	VSS
E	(A21)[2]	DNU[4]	DQ7	VDDQ					VDDQ	DQ2	DNU[4]	(A20)[2]
F	A5	DNU[4]	DQ8	VSSQ					VSSQ	DQ3	DNU[4]	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSS	A4	A3
J	NF[3]	NF[3]	VDD	VDD					VDD	VDD	B0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DNU[4]	DQ14	VSSQ					VSSQ	DQ9	DNU[4]	A19
P	A15	DNU[4]	DQ15	VDDQ					VDDQ	DQ10	DNU[4]	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	DQ11	DNU[4]	VSS
T	VTT	DNU[4]	DQ16	VDDQ					VDDQ	DQ12	DNU[4]	VTT
U	VDD	DNU[4]	DQ17	VSSQ					VSSQ	DQ13	DNU[4]	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

Notes:
1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND
3. No Function. This signal is internally connected and has parasitic characteristics of a clock input signal.
4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND.

Table 4: 32 Meg x 9 Ball Assignment (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	V_{REF}	V_{SS}	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TMS	TCK
B	V_{DD}	DNU[4]	DNU[4]	$V_{SS}Q$					$V_{SS}Q$	DQ0	DNU[4]	V_{DD}
C	V_{TT}	DNU[4]	DNU[4]	$V_{DD}Q$					$V_{DD}Q$	DQ1	DNU[4]	V_{TT}
D	(A22)[1]	DNU[4]	DNU[4]	$V_{SS}Q$					$V_{SS}Q$	QK0#	QK0	V_{SS}
E	(A21)[2]	DNU[4]	DNU[4]	$V_{DD}Q$					$V_{DD}Q$	DQ2	DNU[4]	A20
F	A5	DNU[4]	DNU[4]	$V_{SS}Q$					$V_{SS}Q$	DQ3	DNU[4]	QVLD
G	A8	A6	A7	V_{DD}					V_{DD}	A2	A1	A0
H	B2	A9	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A4	A3
J	NF[3]	NF[3]	V_{DD}	V_{DD}					V_{DD}	V_{DD}	B0	CK
K	DK	DK#	V_{DD}	V_{DD}					V_{DD}	V_{DD}	B1	CK#
L	REF#	CS#	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A14	A13
M	WE#	A16	A17	V_{DD}					V_{DD}	A12	A11	A10
N	A18	DNU[4]	DNU[4]	$V_{SS}Q$					$V_{SS}Q$	DQ4	DNU[4]	A19
P	A15	DNU[4]	DNU[4]	$V_{DD}Q$					$V_{DD}Q$	DQ5	DNU[4]	DM
R	V_{SS}	DNU[4]	DNU[4]	$V_{SS}Q$					$V_{SS}Q$	DQ6	DNU[4]	V_{SS}
T	V_{TT}	DNU[4]	DNU[4]	$V_{DD}Q$					$V_{DD}Q$	DQ7	DNU[4]	V_{TT}
U	V_{DD}	DNU[4]	DNU[4]	$V_{SS}Q$					$V_{SS}Q$	DQ8	DNU[4]	V_{DD}
V	V_{REF}	ZQ	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TDO	TDI

Notes:
1. Reserved for future use. This signal is not connected.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of a clock input signal.
3. No Function. This signal is internally connected and has parasitic characteristics of a clock input signal.
4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND.

Table 5: Ball Descriptions

Symbol	Type	Description
CK, CK#	Input	Input clock: CK and CK# are differential clock inputs. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip select: CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
WE#, REF#	Input	Command inputs: Sampled at the positive edge of CK, WE#, and REF# define (together with CS#) the command to be executed.
A[0:20]	Input	Address inputs: A[0:20] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK. In the x36 configuration, A[20:19] are reserved for address expansion; in the x18 configuration, A[20] is reserved for address epansion. These expansion addresses can be treated as address inputs, but they do not affect the operation of the device.
A21	–	Reserved for future use. This signal is internally connected and can be treated as an address input.
A22	–	Reserved for future use. This signal is not connected and may be connected to ground.
BA[0:2]	Input	Bank address inputs: Select to which internal bank a command is being applied.
DQ0–DQ35	Input/Output	Data input/output: The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK. During WRITE commands, the data is sampled at both edges of DKx.
QKx, QKx#	Output	Output data clocks: QKx and QKx# are opposite polarity, output data clocks. During READs, they are free running and edge-aligned with data output from the RLDRAM. QKx# is ideally 180 degrees out of phase with QKx. For the x36 device, QK0 and QK0# are aligned with DQ0–DQ17. QK1 and QK1# are aligned with DQ18–DQ35. For the x18 device, QK0 and QK0# are aligned with DQ0–DQ8. QK1 and QK1# are aligned with DQ9–DQ17. Consult the RLDRAM II design guide for more details.
DKx, DKx#	Input	Input data clock: DKx and DKx# are the differential input data clocks. All input data is referenced to both edges of DKx. DKx# is ideally 180 degrees out of phase with DKx. For the x36 device, DQ0–DQ17 are referenced to DK0 and DK0#, and DQ18–DQ35 are referenced to DK1 and DK1#. For the x9 and x18 devices, all DQs are referenced to DK and DK#.
DM	Input	Input data mask: The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH, along with the WRITE input data. DM is sampled on both edges of DK (DK1 for the x36 configuration).
QVLD	Output	Data valid: The QVLD indicates valid output data. QVLD is edge-aligned with QKx and QKx#.
TMS TDI	Input	IEEE 1149.1 test inputs: These balls may be left no connects if the JTAG function is not used in the circuit
TCK	Input	IEEE 1149.1 clock input: This ball must be tied to VSS if the JTAG function is not used in the circuit.
TDO	Output	IEEE 1149.1 test output: JTAG Output
ZQ	Input/Output	External impedance [25–60Ω]: This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 × RQ, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode. Connecting ZQ to VDD invokes the maximum impedance mode. Refer to Figure 8 on page 18 to activate this function.
VREF	Input	Input reference voltage: Nominally VDDQ/2. Provides a reference voltage for the input buffers.
VEXT	Supply	Power supply: 2.5V nominal. See Table 22 on page 44 for range.
VDD	Supply	Power supply: 1.8V nominal. See Table 22 on page 44 for range.

Table 5: Ball Descriptions (continued)

Symbol	Type	Description
VDDQ	Supply	DQ power supply: Nominally, 1.5V or 1.8V. Isolated on the device for improved noise immunity. See Table 22 on page 44 for range.
VSS	Supply	Ground.
VSSQ	Supply	DQ ground: Isolated on the device for improved noise immunity.
VTT	Supply	Power supply: Isolated termination supply. Nominally, VDDQ/2. See Table 22 on page 44 for range.
NF	–	No function: These balls may be connected to ground.
DNU	–	Do not use: These balls may be connected to ground.

Commands

According to the functional signal description, the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

Table 6: Address Widths at Different Burst Lengths

Burst Length	Configuration		
	x36	x18	x9
BL = 2	18:0	19:0	20:0
BL = 4	17:0	18:0	19:0
BL = 8	NA	17:0	18:0

Table 7: Command Table
Note 1

Operation	Code	CS#	WE#	REF#	A[20:0]	B[2:0]	Notes
Device DESELECT/No Operation	DESEL/NOP	H	X	X	X	X	
MRS: Mode Register Set	MRS	L	L	L	OPCODE	X	2
READ	READ	L	H	H	A	BA	3
WRITE	WRITE	L	L	H	A	BA	3
AUTO REFRESH	AREF	L	H	L	X	BA	

Notes: 1. X = “Don’t Care”
H = logic HIGH
L = logic LOW
A = valid address
BA = valid bank address.
2. Only A(17:0) are used for the MRS command.
3. See Table 6.

Table 8: Description of Commands

Command	Description
DESEL/NOP[1]	The NOP command is used to perform a no operation to the RLDRAM, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.
MRS	The mode register is set via the address inputs A(17:0). See Figure 8 on page 18 for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress.
READ	The READ command is used to initiate a burst read access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(20:0) selects the data location within the bank.
WRITE	The WRITE command is used to initiate a burst write access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(20:0) selects the data location within the bank. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written).
AREF	The AREF is used during normal operation of the RLDRAM to refresh the memory content of a bank. The command is nonpersistent, so it must be issued each time a refresh is required. The value on the BA(2:0) inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a “Don’t Care” during the AREF command. The RLDRAM requires 64K cycles at an average periodic interval of 0.49µs[2] (MAX). To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLDRAM at periodic intervals of 3.9µs[3].

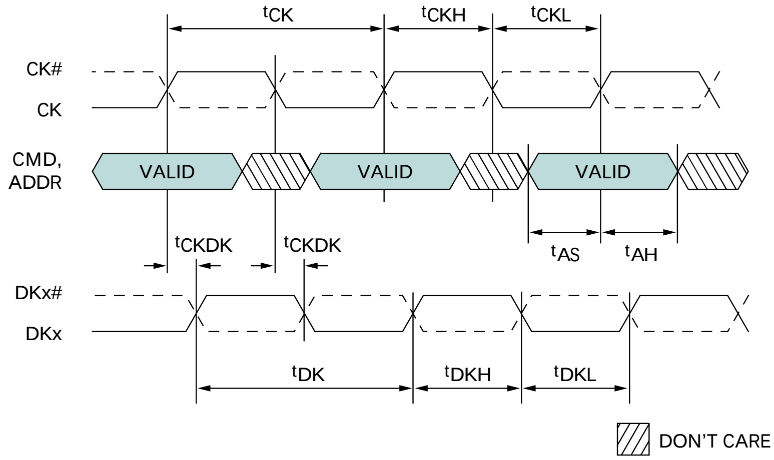
Notes:
1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.
2. Actual refresh is 32ms/8K/8 = 0.488µs.
3. Actual refresh is 32ms/8K = 3.90µs.

Table 9: AC Electrical Characteristics
Note 1

Description	Symbol	-25		-33		-5		Units	Notes
		Min	Max	Min	Max	Min	Max		
Clock									
Clock cycle time	tCK, tDK	2.5	5.7	3.3	5.7	5.0	5.7	ns	
System frequency	fCK, fDK	175	400	175	300	175	200	MHz	
Clock phase jitter	tCKVAR		0.15		0.20		0.25	ns	2
Clock HIGH time	tCKH, tDKH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock LOW time	tCKL, tDKL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock to input data clock	tCKDK	-0.3	0.5	-0.3	1.0	-0.3	1.5	ns	
Mode register set cycle time to any command	tMRSC	6		6		6		tCK	
Setup Times									
Address/command and input setup time	tAS/tCS	0.4		0.5		0.8		ns	
Data-in and data mask to DK setup time	tDS	0.25		0.3		0.4		ns	
Hold Times									
Address/command and input hold time	tAH/tCH	0.4		0.5		0.8		ns	
Data-in and data mask to DK hold time	tDH	0.25		0.3		0.4		ns	
Data and Data Strobe									
Output data clock HIGH time	tQKH	0.9	1.1	0.9	1.1	0.9	1.1	tCKH	
Output data clock LOW time	tQKL	0.9	1.1	0.9	1.1	0.9	1.1	tCKL	
QK edge to clock edge skew	tCKQK	-0.25	0.25	-0.3	0.3	-0.5	0.5	ns	
QK edge to output data edge	tQKQ0, tQKQ1	-0.2	0.2	-0.25	0.25	-0.3	0.3	ns	3
QK edge to any output data edge	tQKQ	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns	4
QK edge to QVLD	tQKVLD	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns	

Notes:
1. All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with VREF of the command, address, and data signals.
2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
3. tQKQ0 is referenced to Q0–Q17 in x36 and Q0–Q8 in x18.
   tQKQ1 is referenced to Q18–Q35 in x36 and Q9–Q17 in x18.
4. tQKQ takes into account the skew between any QKx and any Q.

Figure 3: Clock/Input Data Clock Command/Address Timings



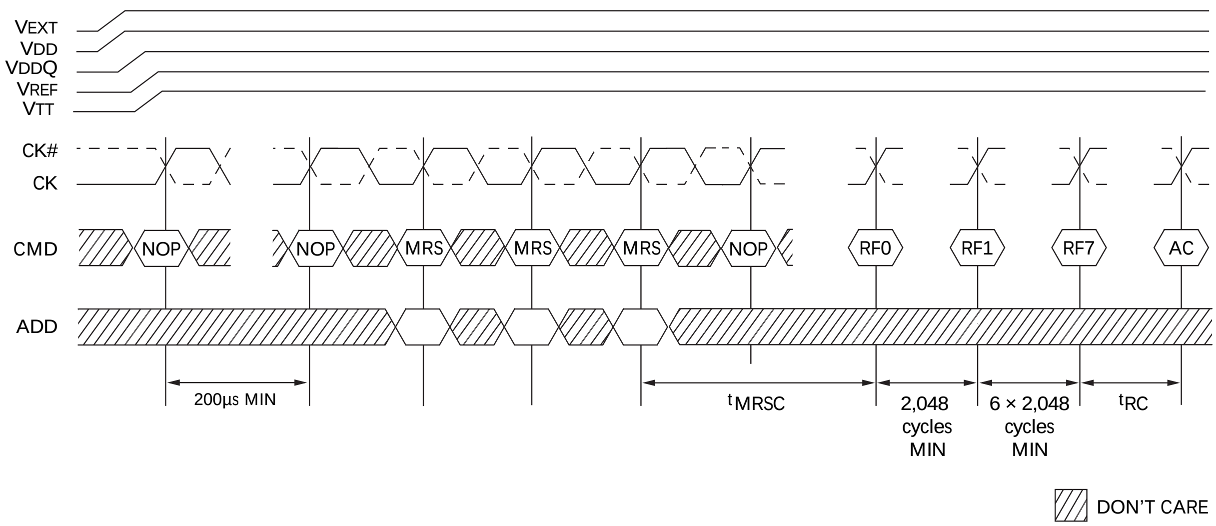
Initialization

The RLDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device.

The following sequence is used for Power-Up:

1. Apply power (V_{EXT}, V_{DD}, $V_{DD}Q$, V_{REF}, V_{TT}) and start clock as soon as the supply voltages are stable. Apply V_{DD} and V_{EXT} before or at the same time as $V_{DD}Q$. Apply $V_{DD}Q$ before or at the same time as V_{REF} and V_{TT}. Although there is no timing relation between V_{EXT} and V_{DD}, the chip starts the power-up sequence only after both voltages are at their nominal levels. The pad supply must not be applied before the core supplies. CK/CK# must meet $V_{ID(DC)}$ prior to being applied. Maintain all remaining balls in NOP conditions.
2. Maintain stable conditions for 200µs (MIN).
3. Issue three MRS commands: two dummies plus one valid MRS. It is recommended that the dummy MRS commands are the same value as the desired MRS.
4. ^{t}MRSC after the valid MRS, issue eight AUTO REFRESH commands, one on each bank and separated by 2,048 cycles. Initial bank refresh order does not matter.
5. After ^{t}RC, the chip is ready for normal operation.

Figure 4: Power-Up Sequence



Notes: 1. MRS: MRS command
RFx: REFRESH Bank x
AC: Any command.

Programmable Impedance Output Buffer

The RLDRAM II is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and VSS. The value of the resistor must be five times the desired impedance. For example, a 300Ω resistor is required for an output impedance of 60Ω. To ensure that output impedance is one fifth the value of RQ (within 15 percent), the range of RQ is 125Ω to 300Ω.

Output impedance updates may be required because, over time, variations may occur in supply voltage and temperature. The device samples the value of RQ. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update.

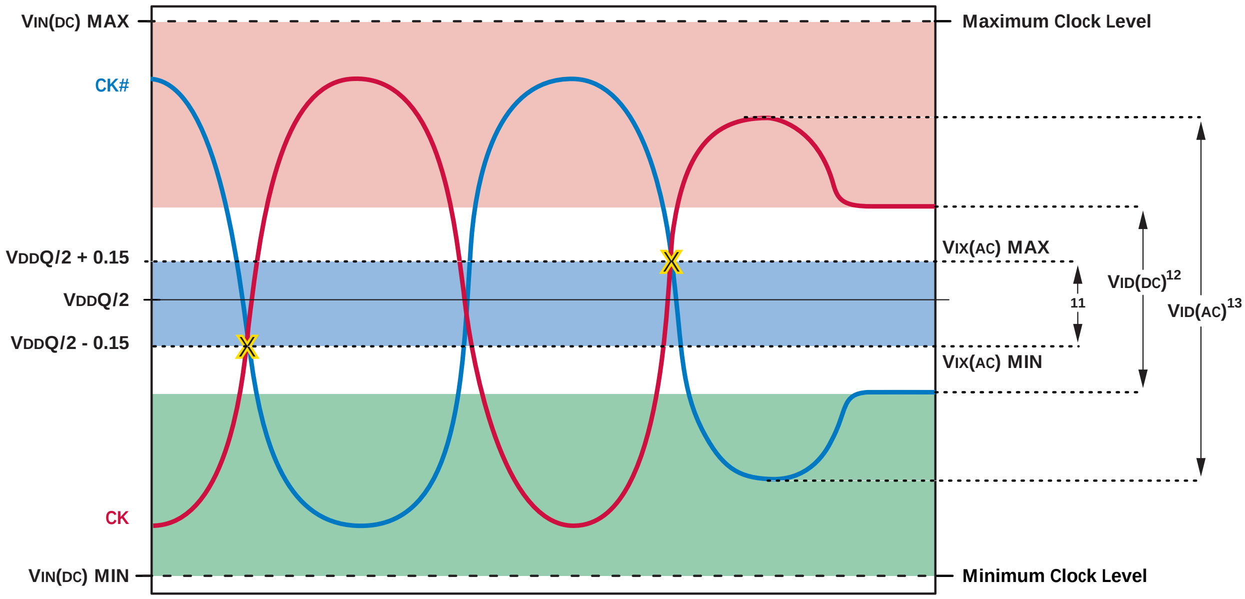
Clock Considerations

The RLDRAM II utilizes internal delay-locked loops for maximum output, data valid windows. It can be placed into a stopped-clock state to minimize power with a modest restart time of 1,024 cycles.

Table 10: Clock Input Operating Conditions
Notes 1–8

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock Input Voltage Level; CK and CK#	VIN(DC)	-0.3	VDDQ + 0.3	V	
Clock Input Differential Voltage; CK and CK#	VID(DC)	0.2	VDDQ + 0.6	V	9
Clock Input Differential Voltage; CK and CK#	VID(AC)	0.4	VDDQ + 0.6	V	9
Clock Input Crossing Point Voltage; CK and CK#	VIX(AC)	VDDQ/2 - 0.15	VDDQ/2 + 0.15	V	10

Figure 5: Clock Input

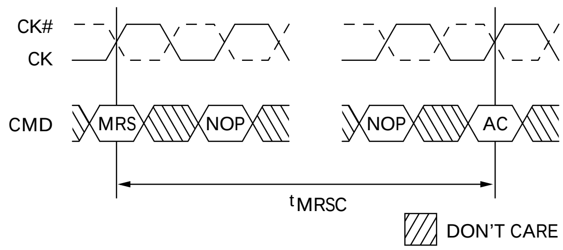


Notes:
1. DKx and DKx# have the same requirements as CK and CK#.
2. All voltages referenced to VSS.
3. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
4. Outputs (except for IDD measurements) measured with equivalent load.
5. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between VIL(AC) and VIH(AC).
6. The AC and DC input level specifications are as defined in the HSTL Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
7. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is VREF.
8. CK and CK# input slew rate must be ≥ 2 V/ns (≥4 V/ns if measured differentially).
9. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
10. The value of VIX is expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.
11. CK and CK# must cross within this region.
12. CK and CK# must meet at least VID(DC) MIN when static and centered around VDDQ/2.
13. Minimum peak-to-peak swing.

Mode Register Set Command (MRS)

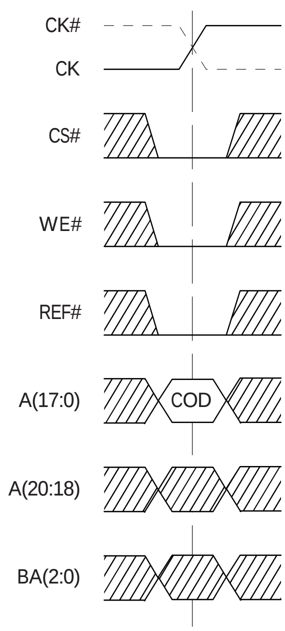
The mode register stores the data for controlling the operating modes of the memory. It programs the RLDRAM configuration, burst length, test mode, and I/O options. During a MRS command, the address inputs A(17:0) are sampled and stored in the mode register. ^{t}MRSC must be met before any command can be issued to the RLDRAM. The mode register may be set at any time during device operation. However, any pending operations are not guaranteed to successfully complete. See the RLDRAM II design guide for more details.

Figure 6: Mode Register Set Timing



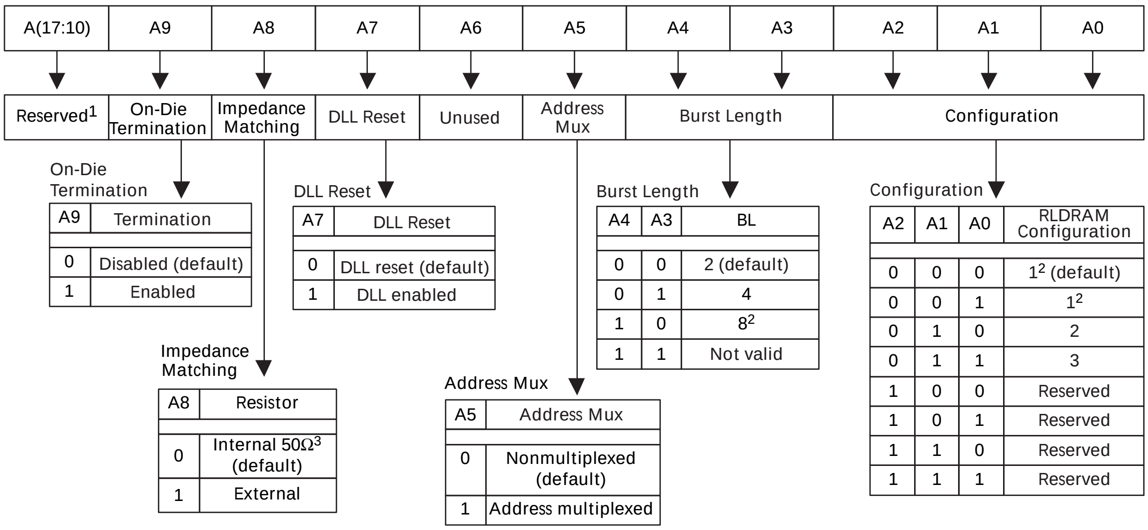
Note: MRS: MRS command; AC: any command.

Figure 7: Mode Register Set



Note: COD: code to be loaded into the register.

Figure 8: Mode Register Bit Map



Notes: 1. Bits A(17:10) *must* be set to zero.
2. BL = 8 is not available for configuration 1.
3. ±15% temperature variation.

Configuration Table

Table 11 shows, for different operating frequencies, the different RLDRAM configurations that can be programmed into the mode register. The READ and WRITE latency (^tRL and ^tWL) values along with the row cycle times (^tRC) are shown in clock cycles as well as in nanoseconds. The shaded areas correspond to configurations that are not allowed.

Table 11: RLDRAM Configuration Table

Frequency	Symbol	Configuration			Units
		1[1]	2	3	
	^tRC	4	6	8	cycles
	^tRL	4	6	8	cycles
	^tWL	5	7	9	cycles
400 MHz	^tRC			20.0	ns
	^tRL			20.0	ns
	^tWL			22.5	ns
300 MHz	^tRC		20.0	26.7	ns
	^tRL		20.0	26.7	ns
	^tWL		23.3	30.0	ns
200 MHz	^tRC	20.0	30.0	40.0	ns
	^tRL	20.0	30.0	40.0	ns
	^tWL	25.0	35.0	45.0	ns

Notes: 1. BL = 8 is not available for configuration 1.

Write Basic Information

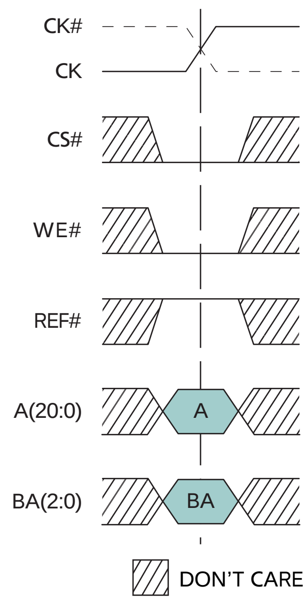
Write accesses are initiated with a WRITE command, as shown in Figure 9. Row and bank addresses are provided together with the WRITE command.

During WRITE commands, data will be registered at both edges of DK according to the programmed burst length (BL). A WRITE latency (WL) one cycle longer than the programmed READ latency (RL + 1) is present, with the first valid data registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command. Figures 13 and 14 illustrate the timing requirements for a WRITE followed by a READ for bursts of two and four, respectively.

Setup and hold times for incoming DQ relative to the DK edges are specified as ^{t}DS and ^{t}DH. The input data is masked if the corresponding DM signal is HIGH. The setup and hold times for data mask are also ^{t}DS and ^{t}DH.

Figure 9: WRITE Command



Note: A: Address; BA: Bank address.

Figure 10: Basic WRITE Burst/DM Timing

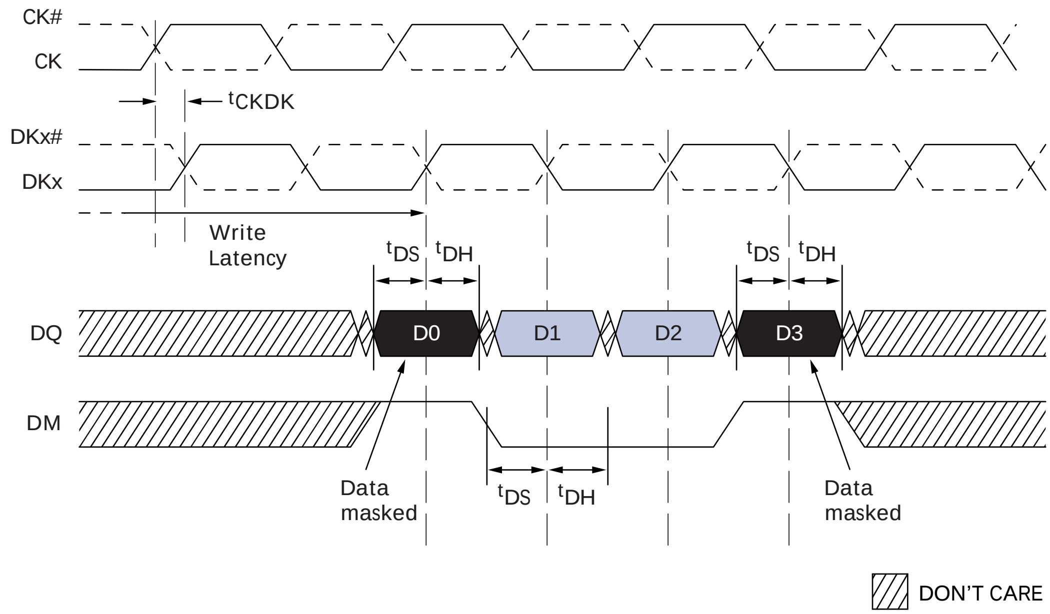


Figure 11: WRITE Burst Basic Sequence: BL = 2, RL = 4, WL = 5, Configuration 1

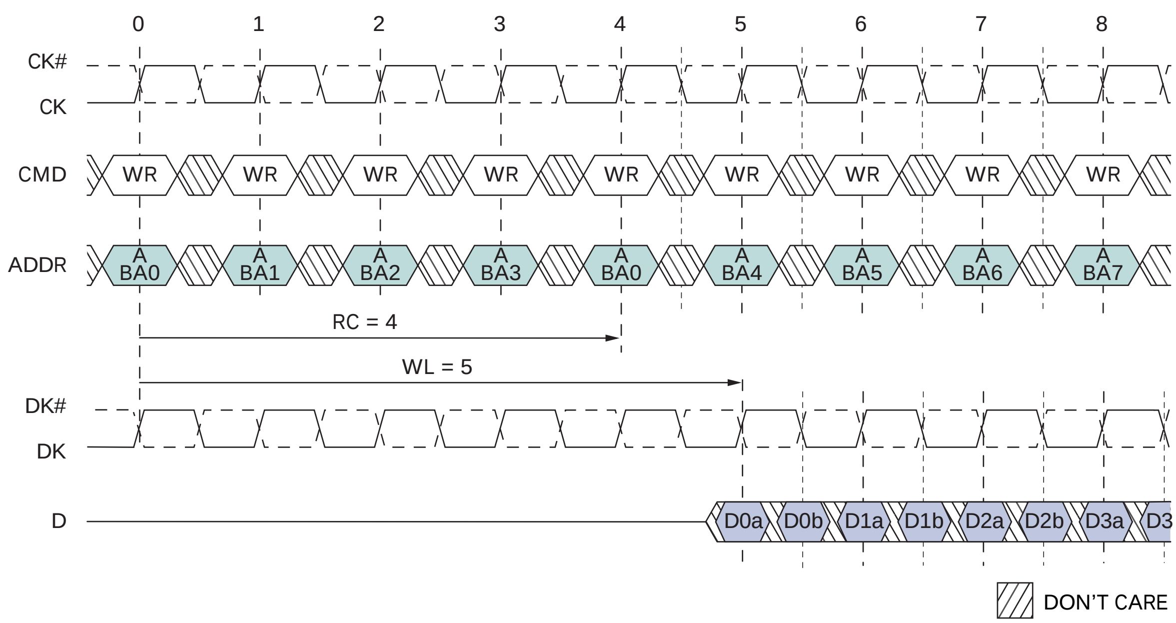
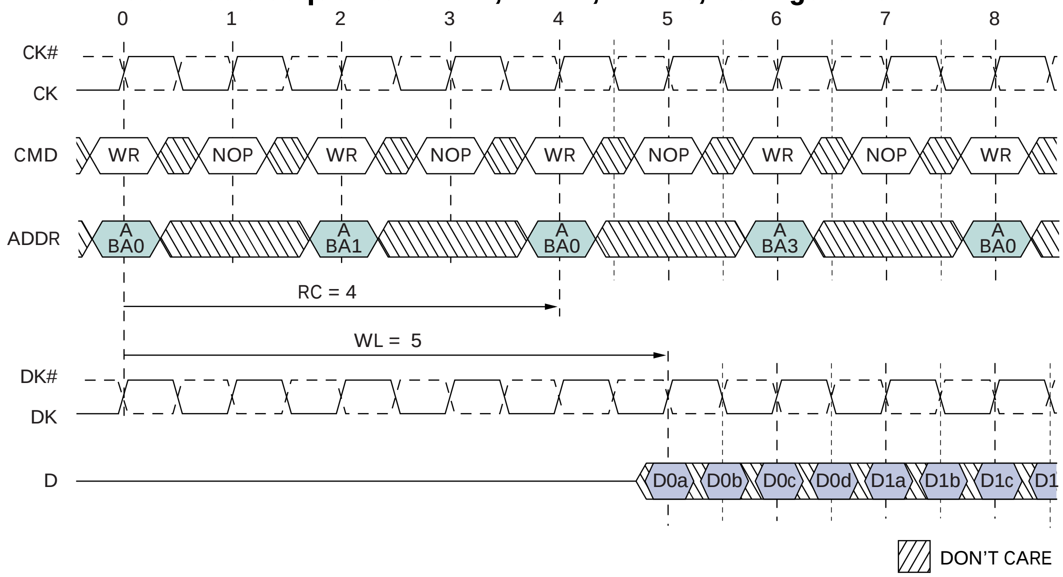


Figure 12: WRITE Burst Basic Sequence: BL = 4, RL = 4, WL = 5, Configuration 1



Notes: 1. A/BA*x*: Address A of bank *x*
WR: WRITE command
D*xy*: Data *y* to bank *x*
RC: Row cycle time
WL: WRITE latency.
2. Any free bank may be used in any given CMD. The sequence shown is only one example of a bank sequence.

Figure 13: WRITE Followed By READ: BL = 2, RL = 4, WL = 5, Configuration 1

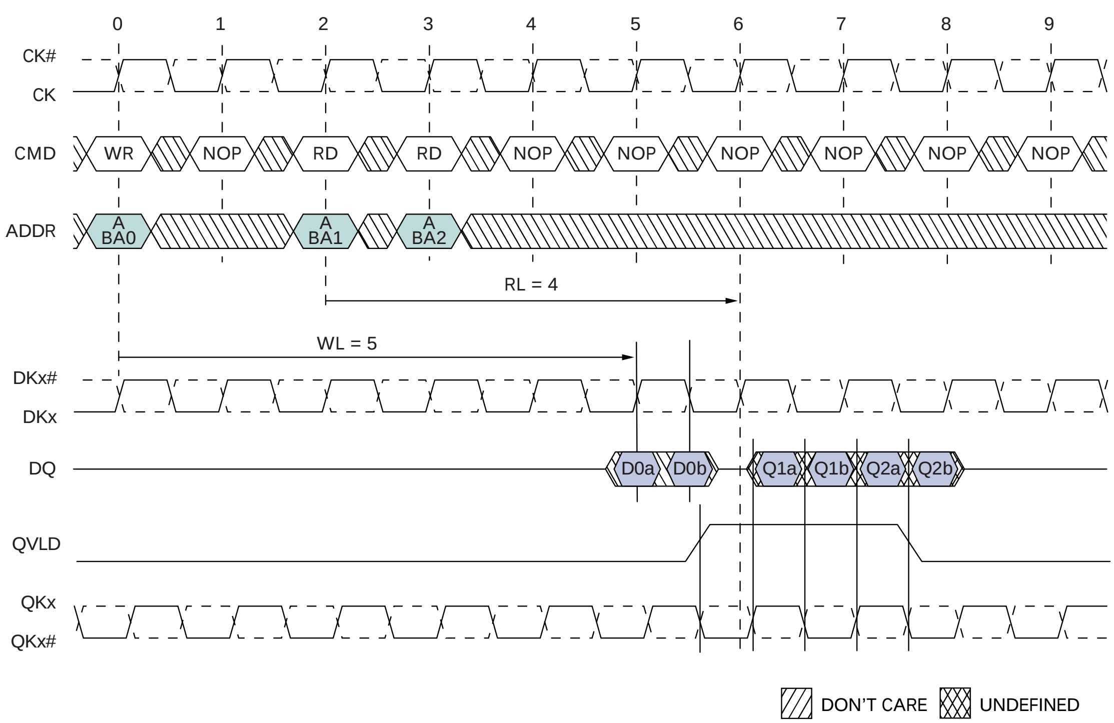
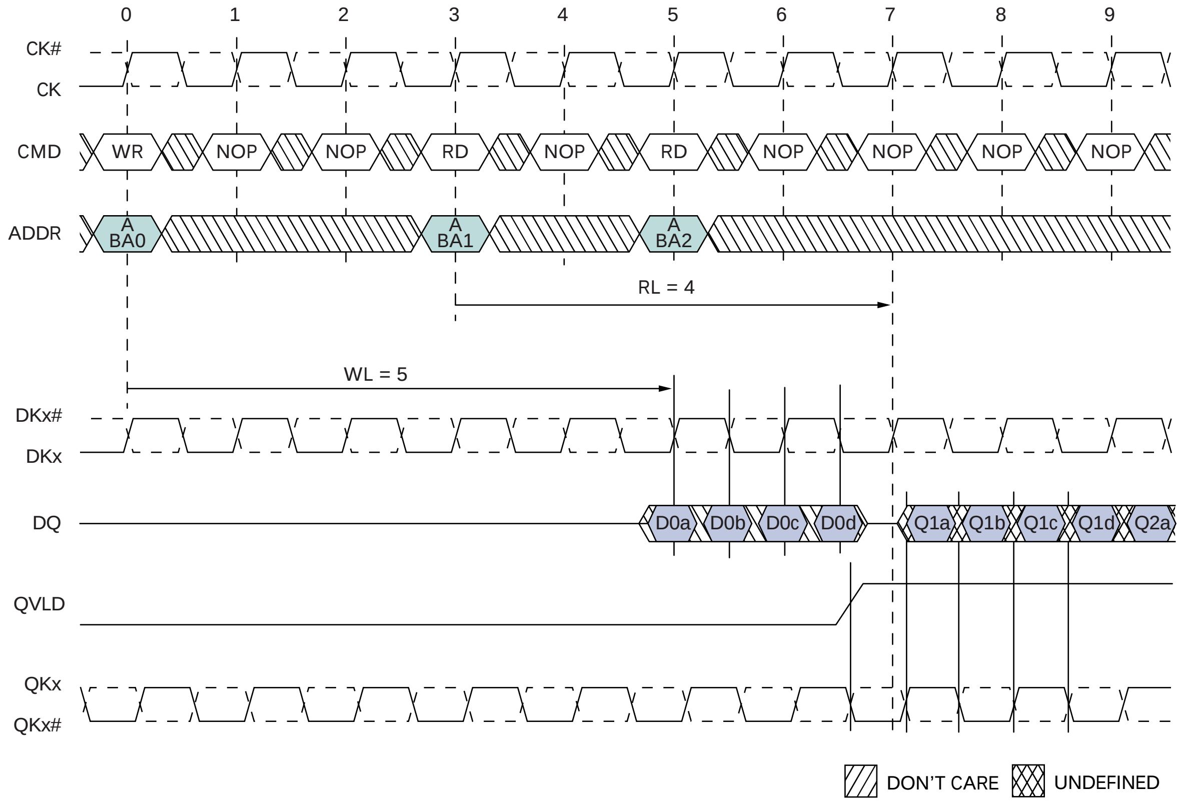


Figure 14: WRITE Followed By READ: BL = 4, RL = 4, WL = 5, Configuration 1



Note: A/BAx: Address A of bank *x*
WR: WRITE
D*xy*: Data *y* to bank x
WL: WRITE latency
RD: READ
Q*xy*: Data *y* from bank *x*
RL: READ latency.

Read Basic Information

Read accesses are initiated with a READ command, as shown in Figure 15. Row and bank addresses are provided with the READ command.

During READ bursts, the memory device drives the read data edge-aligned with the QK signal. After a programmable READ latency, data is available at the outputs. The data valid signal indicates that valid data will be present in the next half clock cycle.

The skew between QK and the crossing point of CK is specified as ^{t}CKQK. ^{t}QKQ0 is the skew between QK0 and the last valid data edge considered over all the data generated at the DQ signals. ^{t}QKQ1 is the skew between QK1 and the last valid data edge considered over all the data generated at the DQ signals. ^{t}QKQx is derived at each QKx clock edge and is not cumulative over time. ^{t}QKQ is the maximum of ^{t}QKQ0 and ^{t}QKQ1.

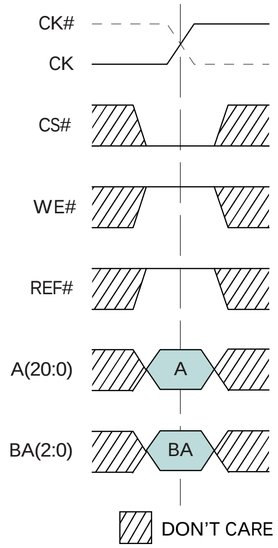
After completion of a burst, assuming no other commands have been initiated, output data (DQ) will go High-Z. Back-to-back READ commands are possible, producing a continuous flow of output data.

The data valid window is derived from each QK transisition and is defined as:

MIN (^{t}QKH, ^{t}QKL) - 2(^{t}QKQ [MAX]).

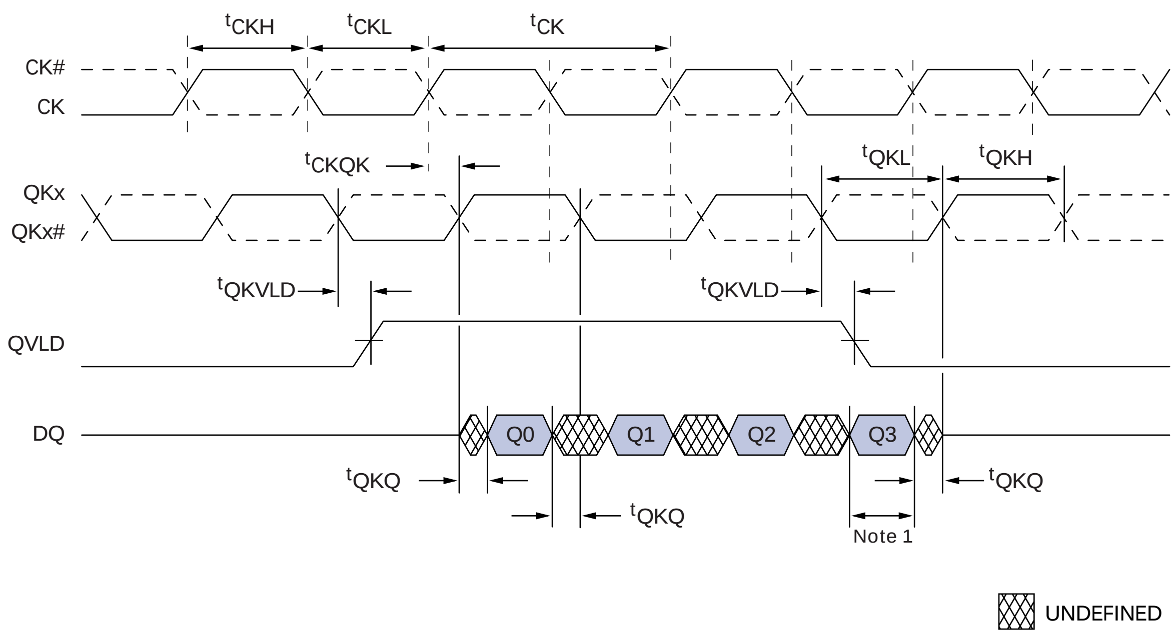
Any READ burst may be followed by a subsequent WRITE command. Figures 19 and 20 illustrate the timing requirements for a READ followed by a WRITE. Depending on the programmed READ latency, a READ-to-WRITE delay occurs in order to prevent bus contention. Some systems having long line lengths or severe skews may need additional idle cycles inserted. Refer to the RLDRAM II design guide for more details.

Figure 15: READ Command



Note: A: Address; BA: Bank address.

Figure 16: Basic READ Burst Timing



Notes: 1. Minimum data valid window can be expressed as MIN (^{t}QKH, ^{t}QKL) - 2 x ^{t}QKQx (MAX).
2. ^{t}QKQ0 is referenced to DQ0–DQ17 in x36 and DQ0–DQ8 in x18.
^{t}QKQ1 is referenced to DQ18–DQ35 in x36 and DQ9–DQ17 in x18.
3. ^{t}QKQ takes into account the skew between any QKx and any DQ.

Figure 17: READ Burst: BL = 2, RL = 4, Configuration 1

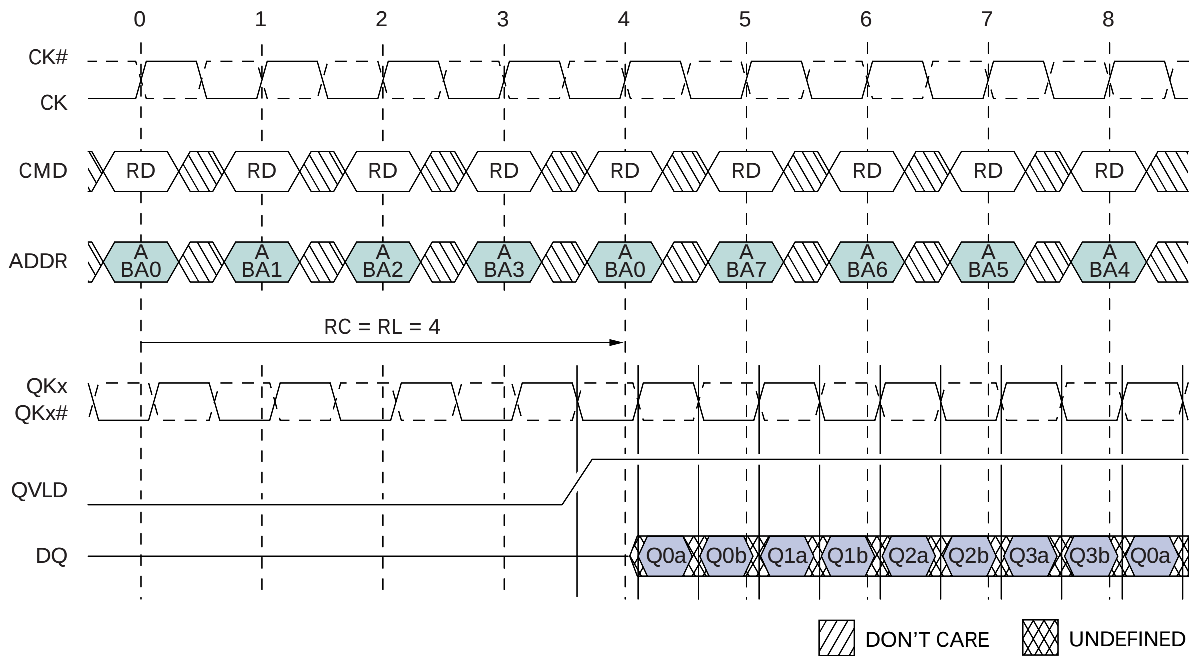
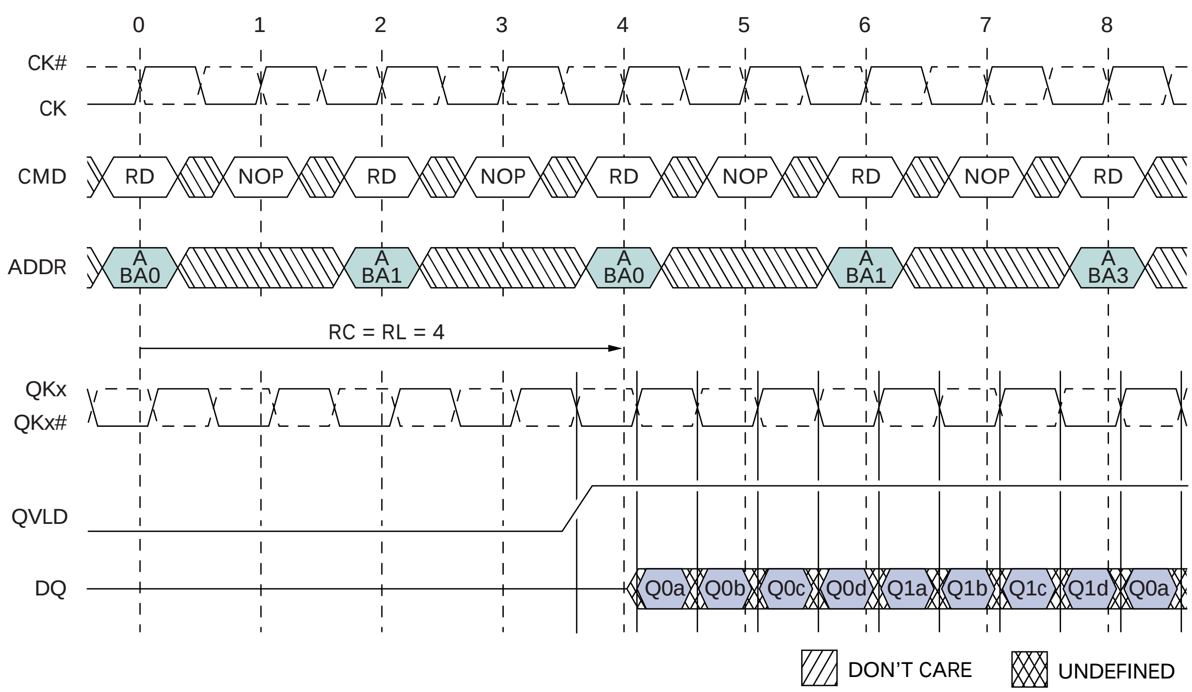


Figure 18: READ Burst: BL = 4, RL = 4, Configuration 1



Note: A/BA*x*: Address A of bank *x*
RD: READ
D*xy*: Data *y* to bank *x*
RC: Row cycle time
RL: READ latency.

Figure 19: READ followed by WRITE, BL = 2, RL = 4, WL = 5, Configuration 1

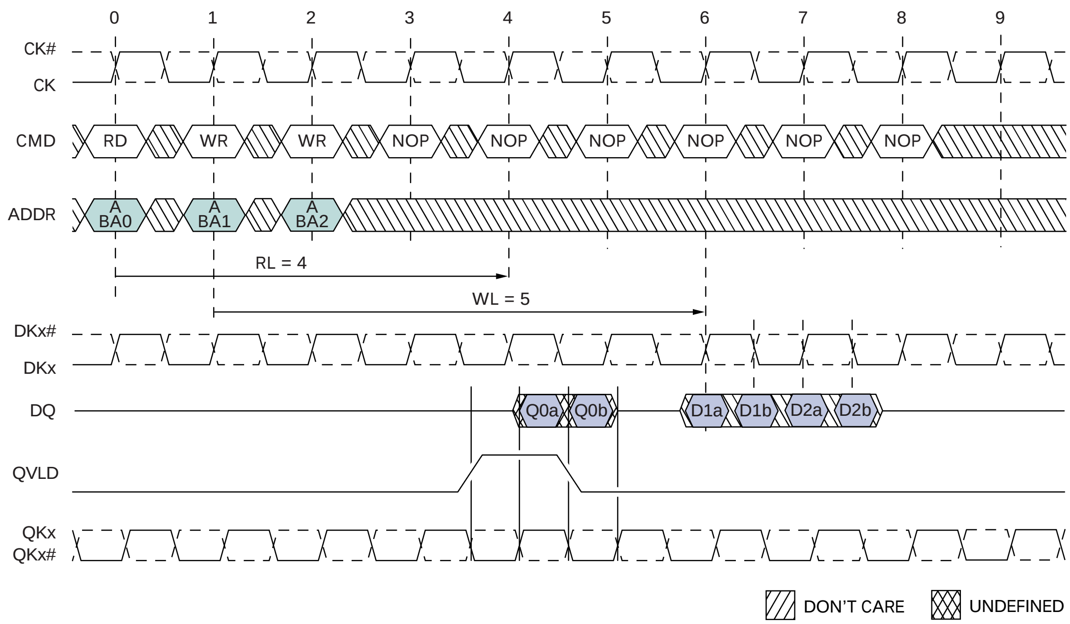
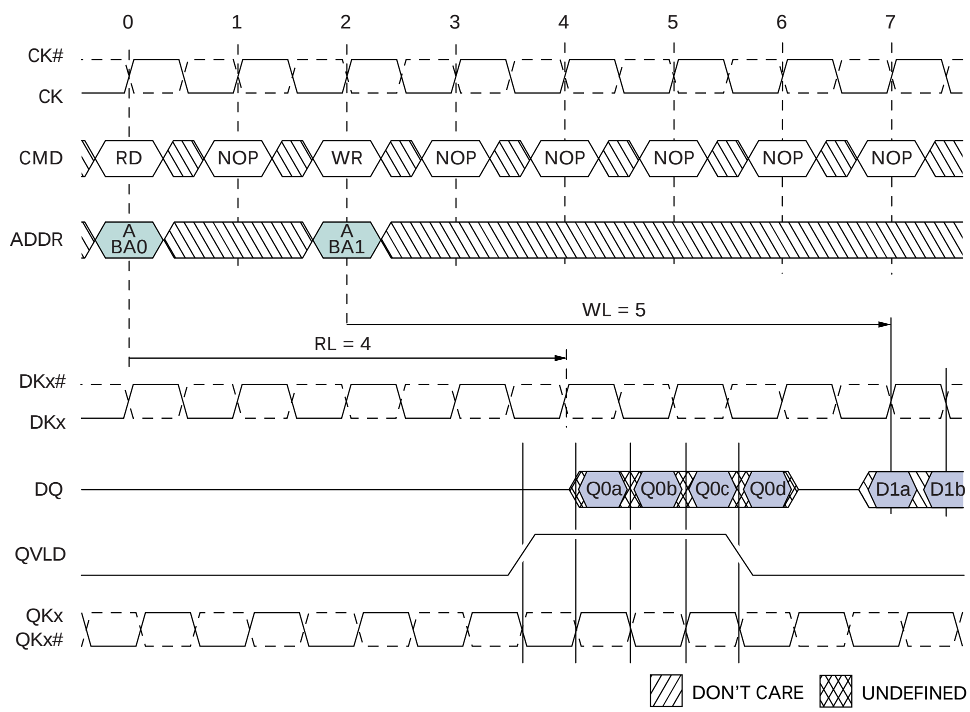


Figure 20: READ followed by WRITE, BL = 4, RL = 4, WL = 5, Configuration 1



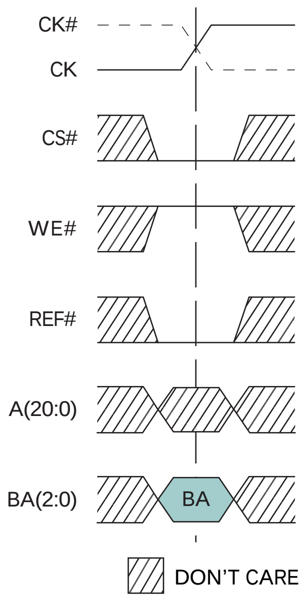
Note: A/BA*x*: Address A of bank *x*
WR: WRITE command
D*xy*: data *y* to bank *x*
WL: Write latency
RD: READ command
Q*xy*: Data *y* from bank *x*
RL: READ latency.

AUTO REFRESH Command (AREF)

AREF is used to perform a REFRESH cycle on one row in a specific bank. The row addresses are generated by an internal refresh counter for each bank; external address balls are "Don't Care." The delay between the AREF command and a subsequent command to the same bank must be at least ^{t}RC.

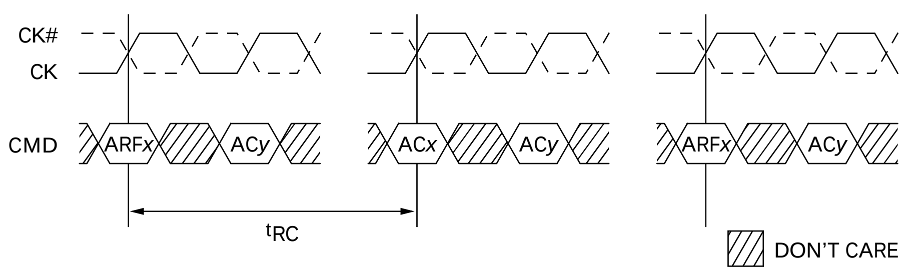
Within a period of 32ms (^{t}REF), the entire memory must be refreshed. Figure 22 illustrates an example of a continuous refresh sequence. Other refresh strategies, such as burst refresh, are also possible.

Figure 21: AUTO REFRESH Command



Note: BA: Bank address.

Figure 22: AUTO REFRESH Cycle



Notes: 1. ACx: Any command on bank x
ARFx: Auto refresh bank x
ACy: Any command on different bank.
2. ^{t}RC is configuration-dependent. Refer to Table 11 on page 18.

On-Die Termination

On-die termination (ODT) is enabled by setting A9 to “1” during a MRS command. With ODT on, all the DQs and DM are terminated to V_{TT} with a resistance R_{TT}. The command, address, and clock signals are not terminated. Figure 23 below shows the equivalent circuit of a DQ receiver with ODT. ODTs are dynamically switched off during READ commands and are designed to be off prior to the RLDRAM driving the bus. Similarly, ODTs are designed to switch on after the RLDRAM has issued the last piece of data.

Table 12: On-Die Termination DC Parameters

Description	Symbol	Min	Max	Units	Notes
Termination Voltage	V_{TT}	0.95 x V_{REF}	1.05 x V_{REF}	V	1, 2
On-Die Termination	R_{TT}	135	165	Ω	3

Notes:
1. All voltages referenced to V_{SS} (GND).
2. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
3. The R_{TT} value is measured at 70°C T_C.

Figure 23: On-Die Termination-Equivalent Circuit

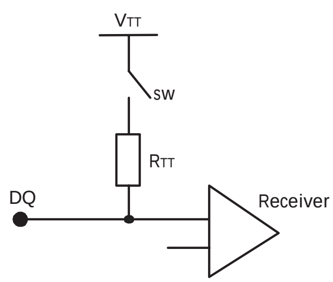
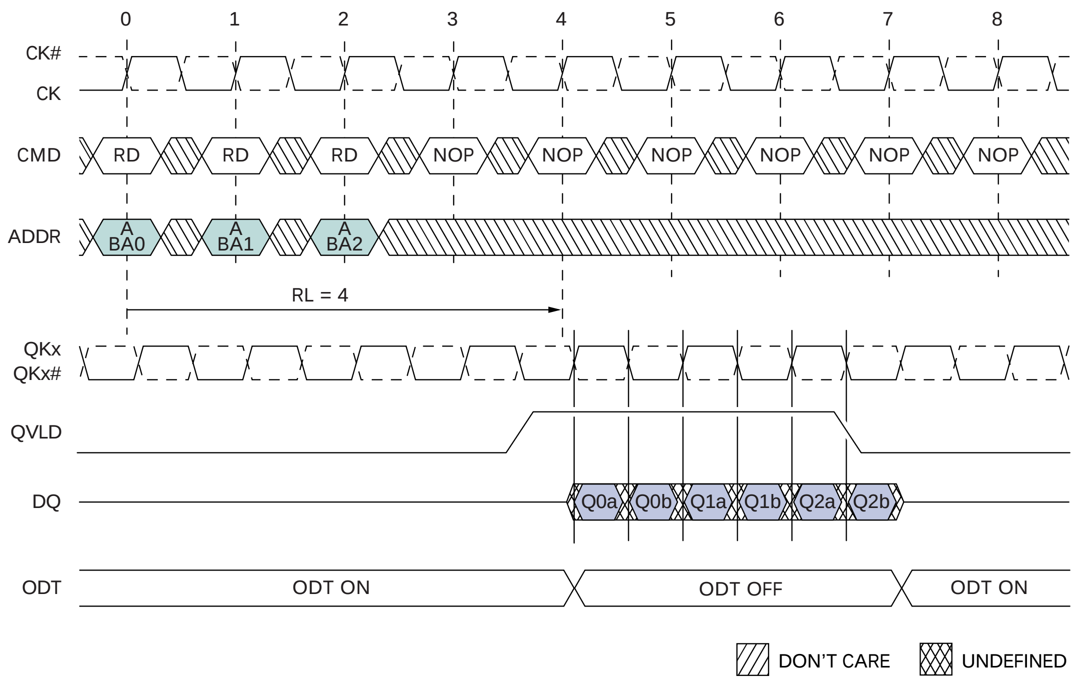


Figure 24: READ Burst with ODT: BL = 2, Configuration 1



Note: A/BA*x*: address A of bank *x*
RD: READ
Q*xy*: Data y to bank *x*
RL: READ latency.

Figure 25: READ NOP READ with ODT: BL = 2, Configuration 1

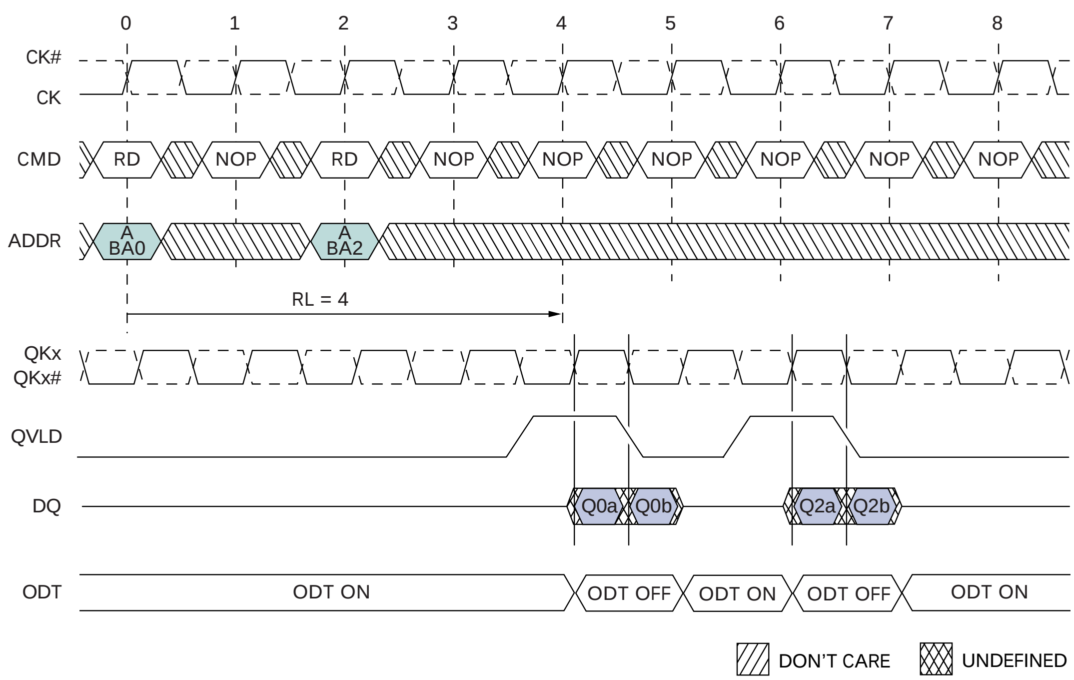
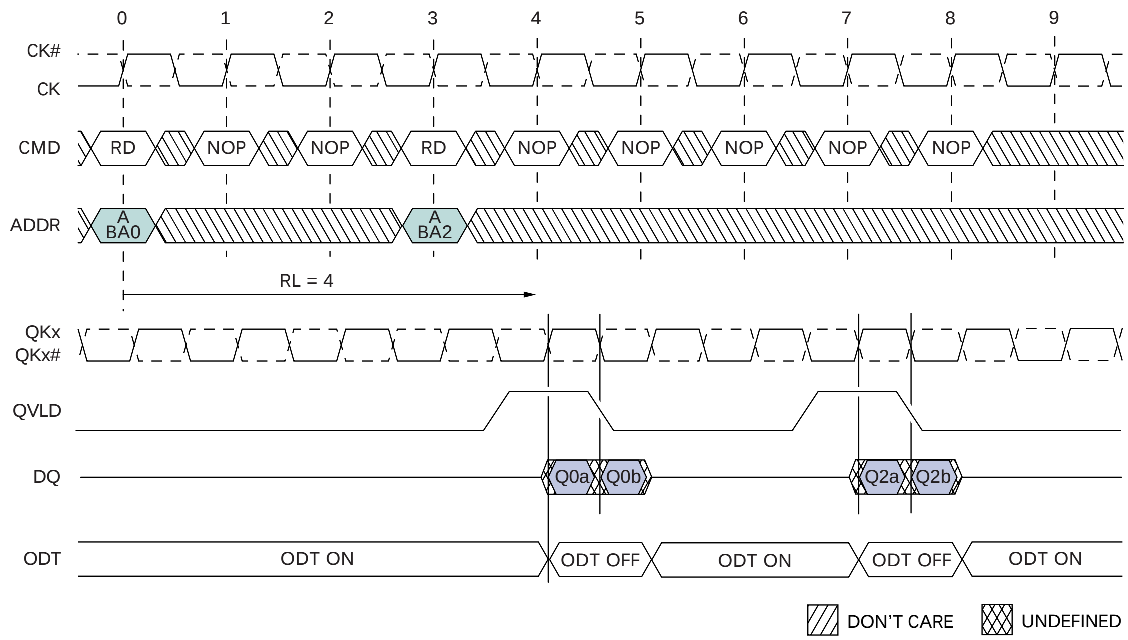


Figure 26: READ NOP NOP READ with ODT: BL = 2, Configuration 1



Note: A/BA*x*: address A of bank *x*
RD: READ
Q*xy*:Data y to bank *x*
RL: READ latency.

Figure 27: READ followed by WRITE with ODT: BL = 2, Configuration 1

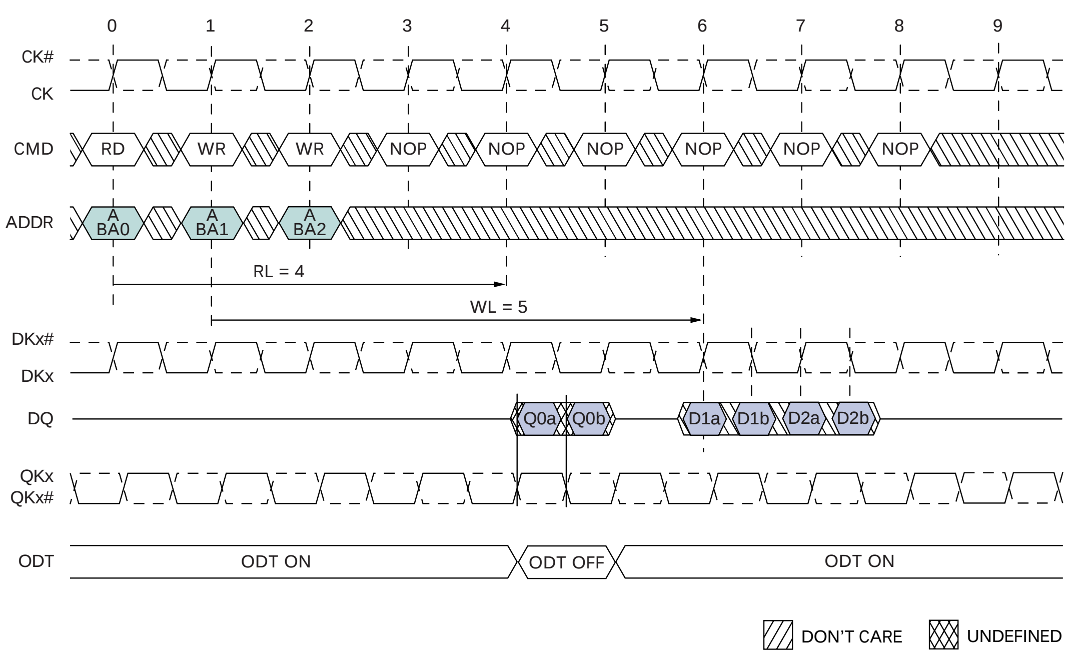
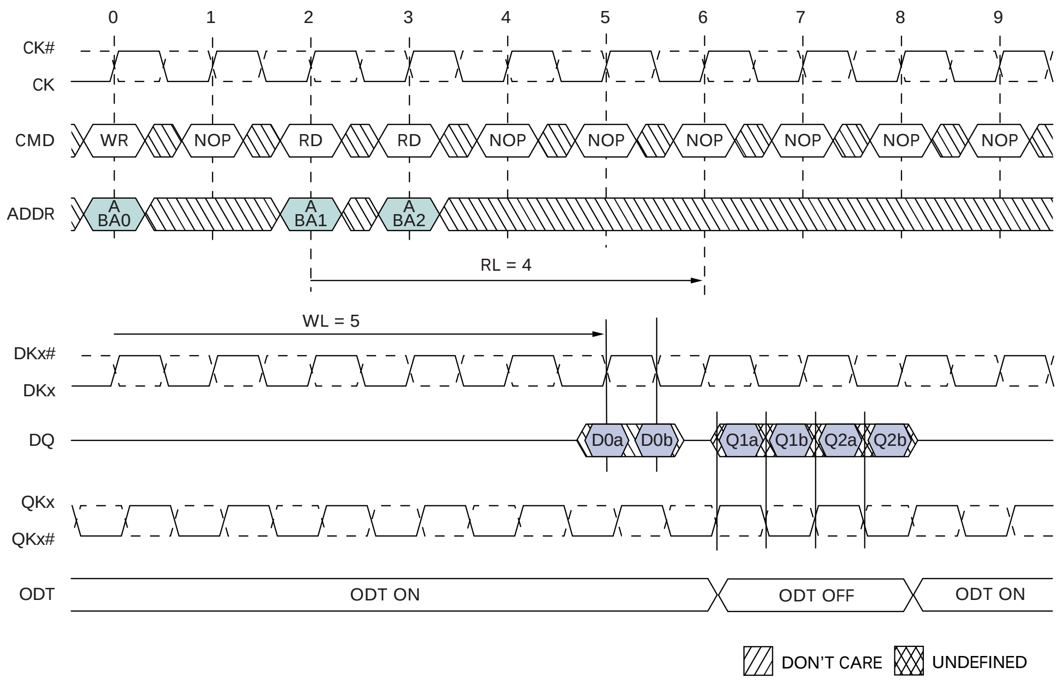


Figure 28: WRITE followed by READ with ODT: BL = 2, Configuration 1



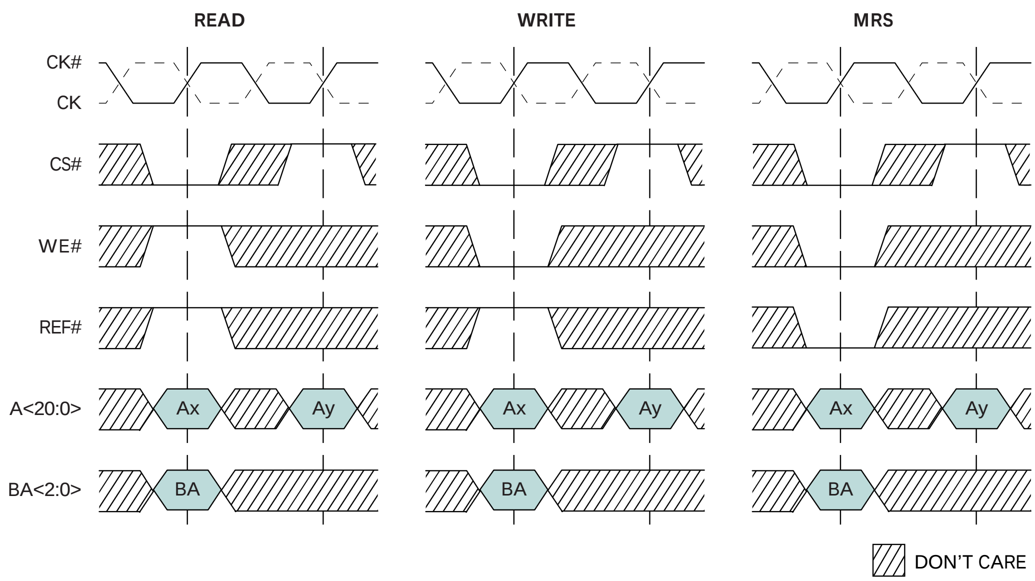
Note: A/BA*x*: Address A of bank x
WR: WRITE command
D*xy*: data *y* to bank *x*
WL: WRITE latency
RD: READ command
Q*xy*: Data *y* from bank *x*
RL: READ latency.

Operation with Multiplexed Addresses

In multiplexed address mode, the address can be provided to the RLDRAM in two parts that are latched into the memory with two consecutive rising clock edges. This provides the advantage that a maximim of 11 address balls are required to control the RLDRAM, reducing the number of balls on the controller side. The data bus efficiency in continuous burst mode is not affected for BL = 4 and BL = 8 since at least two clocks are required to read the data out of the memory. The bank addresses are delivered to the RLDRAM at the same time as the write command and the first address part, Ax.

This option is available by setting bit A5 to “1” in the mode register. Once this bit is set, the READ, WRITE, and MRS commands follow the format described in Figure 29. See Figure 31 on page 32 for the power-up sequence.

Figure 29: Command Description in Multiplexed Address Mode



Notes: 1. *Ax, Ay*: Address
BA: Bank Address.
2. The minimum setup and hold times of the two address parts are defined ^{t}AS and ^{t}AH.

Figure 30: Mode Register Set Command in Multiplexed Address Mode

Ax	A9	A8			A5	A4	A3			A0
Ay			A9	A8				A4	A3	
	On-Die Termination	Impedance Matching	DLL Reset	Unused	Address Mux	Burst Length		Configuration		

On-Die Termination

A9x	Termination
0	Disabled (default)
1	Enabled

Impedance Matching

A8x	Resistor
0	Internal 50Ω[4] (default)
1	External

DLL Reset

A9y	DLL Reset
0	DLL reset (default)
1	DLL enabled

Address Mux

A5x	Address Mux
0	Nonmultiplexed (default)
1	Address multiplexed

Burst Length

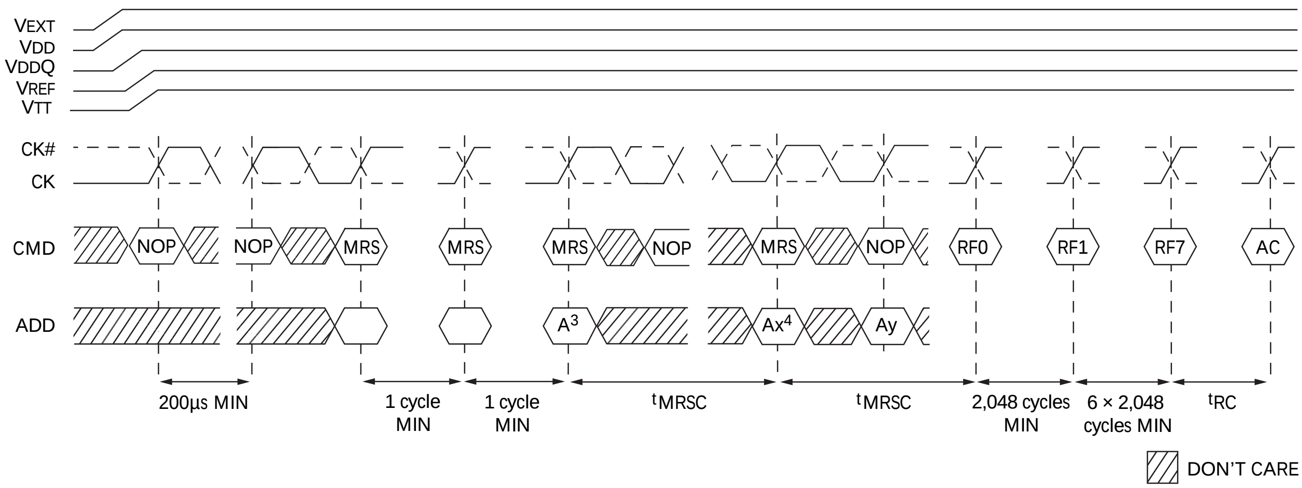
A4x	A3x	BL
0	0	2 (default)
0	1	4
1	0	8[3]
1	1	Not valid

Configuration

A4y	A3y	A0x	RLDRAM Configuration
0	0	0	1[3] (default)
0	0	1	1[3]
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes: 1. The addresses A0, A3, A4, A5, A8, and A9 must be set as follows in order to activate the mode register in the multiplexed address mode
2. Bits A(17:10) *must* be set to zero.
3. BL = 8 is not available for configuration 1.
4. ±15% temperature variation.

Figure 31: Power-Up Sequence in Multiplexed Address Mode



Notes:
1. The above sequence must be respected in order to power up the RLDRAM in the multiplexed address mode.
2. MRS: MRS command
   RFx: REFRESH Bank x
   AC: any command.
3. Address A5 must be set HIGH (muxed address mode setting when RLDRAM is in normal mode of operation).
4. Address A5 must be set HIGH (muxed address mode setting when RLDRAM is already in muxed address mode).

Address Mapping

The address mapping is described in Table 13 as a function of data width and burst length.

Table 13: Address Mapping in Multiplexed Address Mode
Note 1

Data Width	Burst Length	Ball	Address										
			A0[2]	A3	A4	A5[3]	A8	A9	A10	A13	A14	A17	A18
x36	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x18	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x9	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15

Notes:
1. X means "Don't Care."
2. Reserved for A20 expansion in multiplexed mode.
3. Reserved for A21 expansion in multiplexed mode.

Configuration Table

In multiplexed address mode, the read and write latencies are increased by one clock cycle. The RLDRAM cycle time remains the same, as described in Table 14.

Table 14: Configuration Table In Multiplexed Address Mode

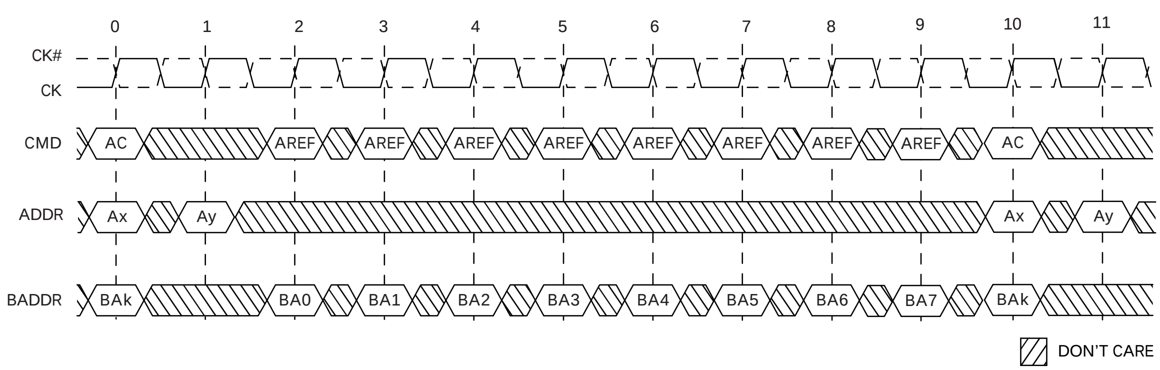
		Configuration			
Frequency	**Symbol**	**1[1]**	**2**	**3**	**Unit**
	^tRC	4	6	8	cycles
	^tRL	5	7	9	cycles
	^tWL	6	8	10	cycles
400 MHz	^tRC			20.0	ns
	^tRL			22.5	ns
	^tWL			25.0	ns
300 MHz	^tRC		20.0	26.7	ns
	^tRL		23.3	30.0	ns
	^tWL		26.7	33.3	ns
200 MHz	^tRC	20.0	30.0	40.0	ns
	^tRL	25.0	35.0	45.0	ns
	^tWL	35.0	40.0	50.0	ns

Notes: 1. BL = 8 is not available for configuration 1.

REFRESH Command in Multiplexed Address Mode

Similar to other commands, the REFRESH command is executed on the next rising clock edge when in the multiplexed address mode. However, since only bank address is required for AREF, the next command can be applied on the following clock. The operation of the AREF command and any other command is represented in Figure 32.

Figure 32: Burst REFRESH Operation



Note: AREF: AUTO REFRESH
AC: Any command
A*x*: First part A*x* of address
A*y*: Second part A*y* of address
BA*k*: Bank *k*; *k* is chosen so that ^tRC is met.

Figure 33: WRITE Burst Basic Sequence: BL = 4, with Multiplexed Addresses, Configuration 1, WL = 6

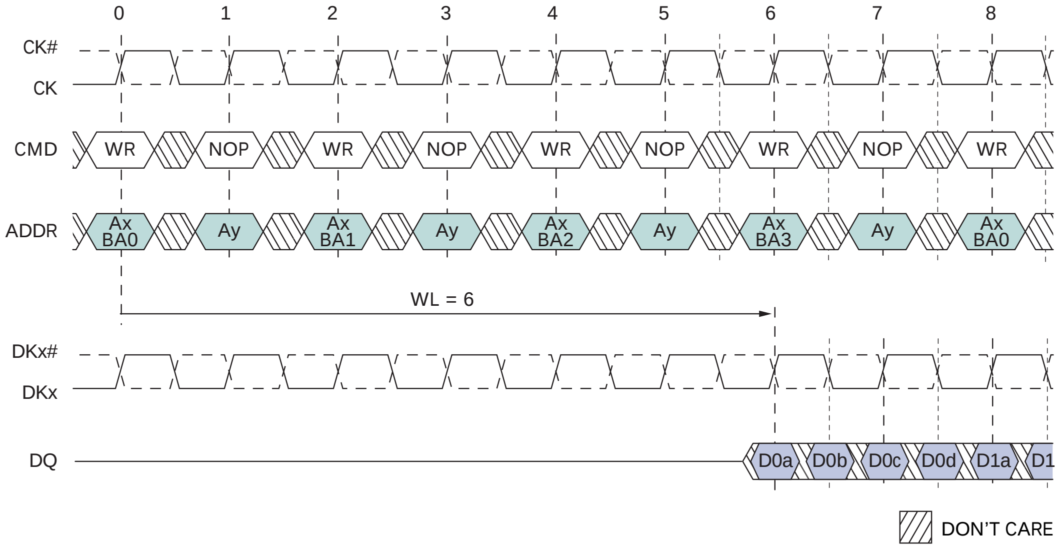
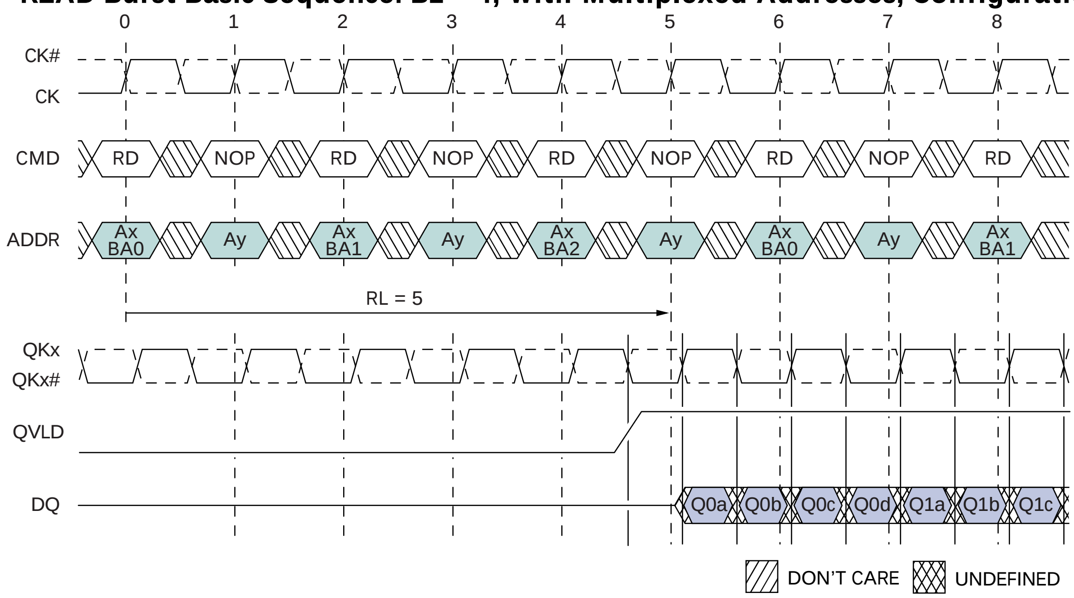


Figure 34: READ Burst Basic Sequence: BL = 4, with Multiplexed Addresses, Configuration 1, RL = 5



Note: A*x*/BA*k*: Address A*x* of bank *k*
A*y*: Address A*y* of bank *k*
WR: WRITE
Djk: Data *k* to bank *j*
WL: WRITE latency
Qjk: Data *k* to bank *j*
RD: READ
RL: READ latency.

IEEE 1149.1 Serial Boundary Scan (JTAG)

RLDRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-2001. The TAP operates using logic levels associated with the VDDQ supply.

RLDRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate RLDRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state, which will not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 35 on page 37. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register (see Figure 36 on page 37).

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Figure 35). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see Figure 36).

Figure 35: TAP Controller State Diagram

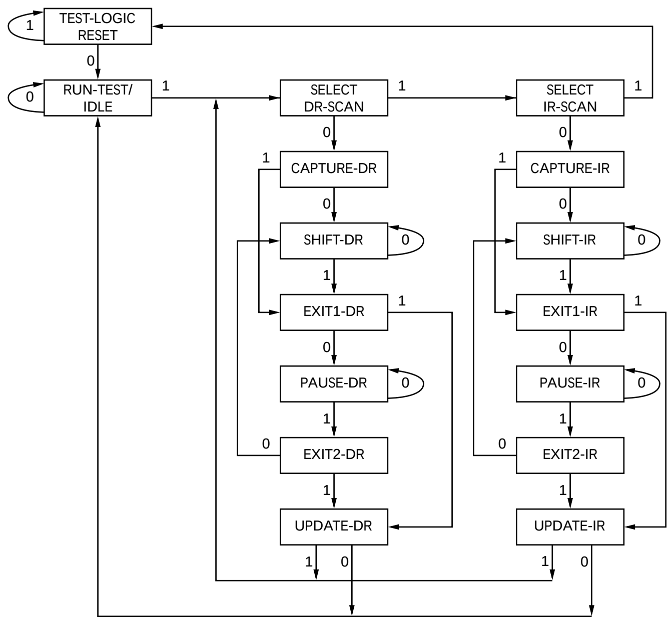
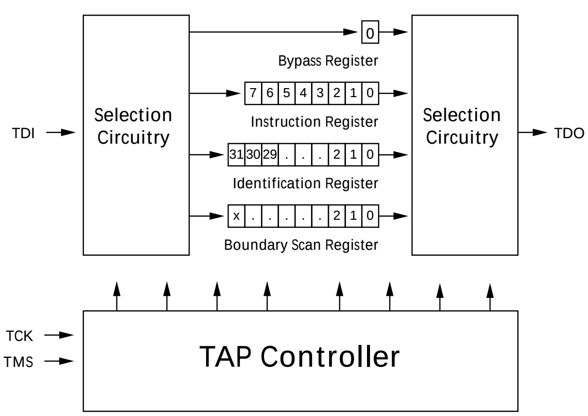


Figure 36: TAP Controller Block Diagram



Note: x = 112 for all configurations.

Performing a TAP RESET

A reset is performed by forcing TMS HIGH (VDDQ) for five rising edges of TCK. This RESET does not affect the operation of the RLDRAM and may be performed while the RLDRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the RLDRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Eight-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls, as shown in Figure 36. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the RLDRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the RLDRAM. Several balls are also included in the scan register to reserved balls. The RLDRAM has a 113-bit register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state.

The Boundary Scan Order tables (see Table 21 on page 43) show the order in which the bits are connected. Each bit corresponds to one of the balls on the RLDRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hard-wired into the RLDRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table on page 42.

TAP Instruction Set

Overview

Many different instructions (2^8) are possible with the 8-bit instruction register. All used combinations are listed in Table 20, Instruction Codes, on page 42. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RLDRAM is fully compliant to the 1149.1 convention.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instrucion. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output balls.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

High-Z

The High-z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RLDRAM outputs into a High-Z state.

CLAMP

When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary scan register.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the RLDRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To ensure that the boundary scan register will capture the correct value of a signal, the RLDRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (tCS plus tCH). The RLDRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved for Future Use

The remaining 22 instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 37: TAP Timing

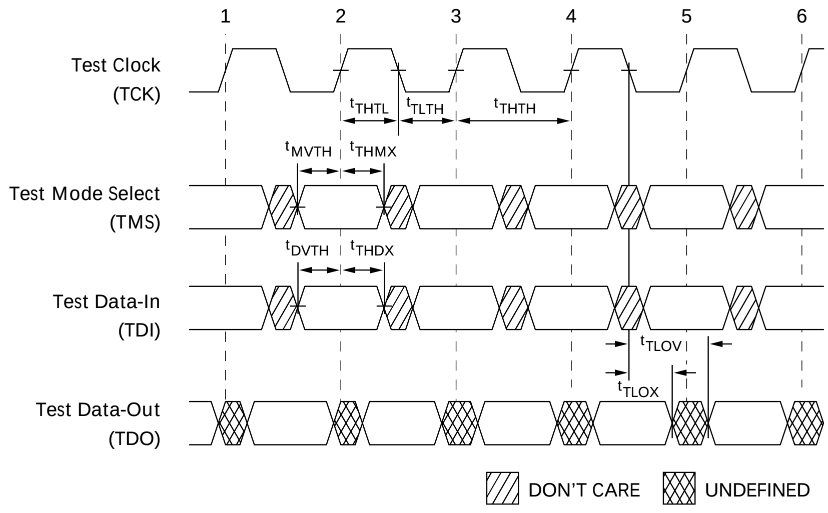


Table 15: TAP AC Electrical Characteristics and Operating Conditions
+0°C ≤ T_C ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V, unless otherwise noted

Description	Symbol	Min	Max	Units	Notes
Input high (Logic 1) voltage	V_{IH}	V_{REF} + 0.3	V_{DD} + 0.3	V	1, 2
Input low (Logic 0) voltage	V_{IL}	V_{SSQ} - 0.3	V_{REF} - 0.3	V	1, 2

Table 16: TAP AC Electrical Characteristics
Note 1; +0°C ≤ T_C ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V

Description	Symbol	Min	Max	Units
Clock				
Clock cycle time	tTHTH	20		ns
Clock frequency	fTF		50	MHz
Clock HIGH time	tTHTL	10		ns
Clock LOW time	tTLTH	10		ns
Output Times				
TCK LOW to TDO unknown	tTLOX	0		ns
TCK LOW to TDO valid	tTLOV		10	ns
TDI valid to TCK HIGH	tDVTH	5		ns
TCK HIGH to TDI invalid	tTHDX	5		ns
Setup Times				
TMS setup	tMVTH	5		ns
Capture setup	tCS	5		ns
Hold Times				
TMS hold	tTHMX	5		ns
Capture hold	tCH	5		ns

Notes: 1. tCS and tCH refer to the setup and hold time requirements of latching data from the boundary scan register.

Table 17: TAP DC Electrical Characteristics and Operating Conditions
$+0°C \le T_C \le +95°C$; $+1.7V \le V_{DD} \le +1.9V$, unless otherwise noted

Description	Condition	Symbol	Min	Max	Units	Notes
Input high (Logic 1) voltage		V_{IH}	V_{REF} + 0.15	V_{DD} + 0.3	V	1, 2
Input low (Logic 0) voltage		V_{IL}	$V_{SS}Q$ - 0.3	V_{REF} - 0.15	V	1, 2
Input leakage current	$0V \le V_{IN} \le V_{DD}$	I_{LI}	-5.0	5.0	µA	
Output leakage current	Output disabled, $0V \le V_{IN} \le V_{DD}Q$	I_{LO}	-5.0	5.0	µA	
Output low voltage	I_{OLC} = 100µA	$V_{OL}1$		0.2	V	1
Output low voltage	I_{OLT} = 2mA	$V_{OL}2$		0.4	V	1
Output high voltage	$\|I_{OHC}\|$ = 100µA	$V_{OH}1$	$V_{DD}Q$ - 0.2		V	1
Output high voltage	$\|I_{OHT}\|$ = 2mA	$V_{OH}2$	$V_{DD}Q$ - 0.4		V	1

Notes: 1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH}(AC) \le V_{DD} + 0.7V$ for $t \le {}^tCK/2$.
Undershoot: $V_{IL}(AC) \ge -0.5V$ for $t \le {}^tCK/2$.
During normal operation, $V_{DD}Q$ must not exceed V_{DD}.

Table 18: Identification Register Definitions

Instruction Field	All Devices	Description
Revision Number (31:28)	abcd	ab = die revision cd = 10 for x36, 01 for x18, 00 for x9.
Device ID (27:12)	00jkidef10100111	def = 000 for 288M, 001 for 576M, 010 for 1G. i = 0 for common I/O, 1 for separate I/O. jk = 00 for RLDRAM, 01 for RLDRAM II.
Micron JEDEC ID Code (11:1)	00000101100	Allows unique identification of RLDRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Table 19: Scan Register Sizes

Register Name	Bit Size
Instruction	8
Bypass	1
ID	32
Boundary Scan	113

Table 20: Instruction Codes

Instruction	Code	Description
Extest	0000 0000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect RLDRAM operations.
ID Code	0010 0001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect RLDRAM operations.
Sample/Preload	0000 0101	Captures I/O ring contents. Places the boundary scan register between TDI and TDO.
Clamp	0000 0111	Selects the bypass register to be connected between TDI and TDO. Data driven by output balls are determined from values held in the boundary scan register.
High-Z	0000 0011	Selects the bypass register to be connected between TDI and TDO. All ouputs are forced into high impedance state.
Bypass	1111 1111	Places the bypass register between TDI and TDO. This operation does not affect RLDRAM operations.

Table 21: Boundary Scan (Exit) Order

Bit#	µBGA Ball	Bit#	µBGA Ball	Bit#	µBGA Ball
1	K1	39	R11	77	C11
2	K2	40	R11	78	C11
3	L2	41	P11	79	C10
4	L1	42	P11	80	C10
5	M1	43	P10	81	B11
6	M3	44	P10	82	B11
7	M2	45	N11	83	B10
8	N1	46	N11	84	B10
9	P1	47	N10	85	B3
10	N3	48	N10	86	B3
11	N3	49	P12	87	B2
12	N2	50	N12	88	B2
13	N2	51	M11	89	C3
14	P3	52	M10	90	C3
15	P3	53	M12	91	C2
16	P2	54	L12	92	C2
17	P2	55	L11	93	D3
18	R2	56	K11	94	D3
19	R3	57	K12	95	D2
20	T2	58	J12	96	D2
21	T2	59	J11	97	E2
22	T3	60	H11	98	E2
23	T3	61	H12	99	E3
24	U2	62	G12	100	E3
25	U2	63	G10	101	F2
26	U3	64	G11	102	F2
27	U3	65	E12	103	F3
28	V2	66	F12	104	F3
29	U10	67	F10	105	E1
30	U10	68	F10	106	F1
31	U11	69	F11	107	G2
32	U11	70	F11	108	G3
33	T10	71	E10	109	G1
34	T10	72	E10	110	H1
35	T11	73	E11	111	H2
36	T11	74	E11	112	J2
37	R10	75	D11	113	J1
38	R10	76	D10	–	–

Notes: 1. Any unused balls that are in the order will read as a logic “0.”

Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Figure 38: Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Storage temperature	-55	+150	°C	
I/O voltage	-0.3V	VDDQ + 0.3	V	
Voltage on VEXT supply relative to VSS	-0.3	+2.8	V	
Voltage on VDD supply relative to VSS	-0.3	+2.1	V	
Voltage on VDDQ supply relative to VSS	-0.3	+2.1	V	
Junction temperature	110		°C	1

Notes: 1. Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

Table 22: DC Electrical Characteristics and Operating Conditions
+0°C ≤ T_C ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V, unless otherwise noted

Description	Condition	Symbol	Min	Max	Units	Notes
Supply voltage		VEXT	2.38	2.63	V	1
Supply voltage		VDD	1.7	1.9	V	1, 4
Isolated output ouffer supply		VDDQ	1.4	VDD	V	1, 4, 5
Reference voltage		VREF	0.49 × VDDQ	0.51 × VDDQ	V	1–3, 8
Termination voltage		VTT	0.95 × VREF	1.05 × VREF	V	9, 10
Input high (Logic 1) voltage		VIH	VREF + 0.1	VDDQ + 0.3	V	1, 4
Input low (Logic 0) voltage		VIL	VSSQ - 0.3	VREF - 0.1	V	1, 4
Output high current	VOH = VDDQ/2	IOH	(VDDQ/2) / (1.15 × RQ/5)	(VDDQ/2) / (0.85 × RQ/5)	mA	6, 7, 11
Output low current	VOL = VDDQ/2	IOL	(VDDQ/2) / (1.15 × RQ/5)	(VDDQ/2) / (0.85 × RQ/5)	mA	6, 7, 11
Clock input leakage current	0V ≤ VIN ≤ VDD	ILC	-5	5	µA	
Input leakage current	0V ≤ VIN ≤ VDD	ILI	-5	5	µA	
Output leakage current	0V ≤ VIN ≤ VDDQ	ILO	-5	5	µA	
Reference voltage current		IREF	-5	5	µA	

Notes:
1. All voltages referenced to VSS (GND).
2. Typically the value of VREF is expect to be 0.5 x VDDQ of the transmitting device. VREF is expected to track variations in VDDQ.
3. Peak-to-peak AC noise on VREF must not exceed ±2% VREF(DC).
4. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ ^{t}CK/2.
   Undershoot: VIL(AC) ≥ -0.5V for t ≤ ^{t}CK/2.
   During normal operation, VDDQ must not exceed VDD.
   Control input signals may not have pulse widths less than ^{t}CK/2 or operate at frequencies exceeding ^{t}CK (MAX).
5. VDDQ can be set to a nominal 1.5V + 0.1V or 1.8V + 0.1V supply.
6. IOH and IOL are defined as absolute values and are measured at VDDQ/2. IOH flows from the device, IOL flows into the device.

7. If MRS bit A8 is 0, use RQ = 250Ω in the equation in lieu of presence of an external impedance matched resistor.
8. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed ±2% of the DC value. Thus, from VDDQ/2, VREF is allowed ±2%VDDQ/2 for DC error and an additional ±2%VDDQ/2 for AC noise. This measurement is to be taken at the nearest VREF bypass capacitor.
9. VTT is expected to be set equal to VREF and must track variations in the DC level of VREF.
10. On-die termination may be selected using mode register bit 9 (see Figure 8 on page 18). A resistance RTT from each data input signal to the nearest VTT can be enabled. RTT = 150Ω (±10%) at 70°C T_C.
11. For VOL and VOH, refer to the RLDRMA II HSpice or IBIS driver models.

Table 23: AC Electrical Characteristics and Operating Conditions
+0°C ≤ Tc ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V, unless otherwise noted

Description	Conditions	Symbol	Min	Max	Units
Input high (Logic 1) voltage	Matched impedance mode	VIH	VREF + 0.2	VDDQ + 0.3	V
Input low (Logic 0) voltage	Matched impedance mode	VIL	VSSQ - 0.3	VREF - 0.2	V

Table 24: Capacitance

Description	Conditions	Symbol	Min	Max	Units
Address/Control input capacitance	T_A = 25°C; f = 1 MHz	CI	1.5	2.5	pF
I/O capacitance (DQ, DM, QK)		CO	3.5	5.0	pF
Clock capacitance		CCK	2.0	3.0	pF

Figure 39: Output Test Conditions

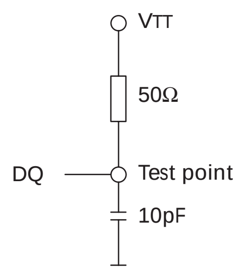


Figure 40: Input Waveform

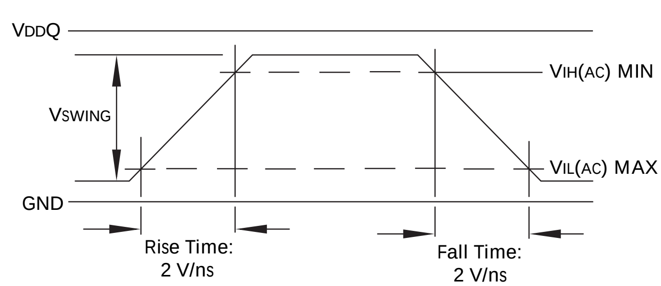


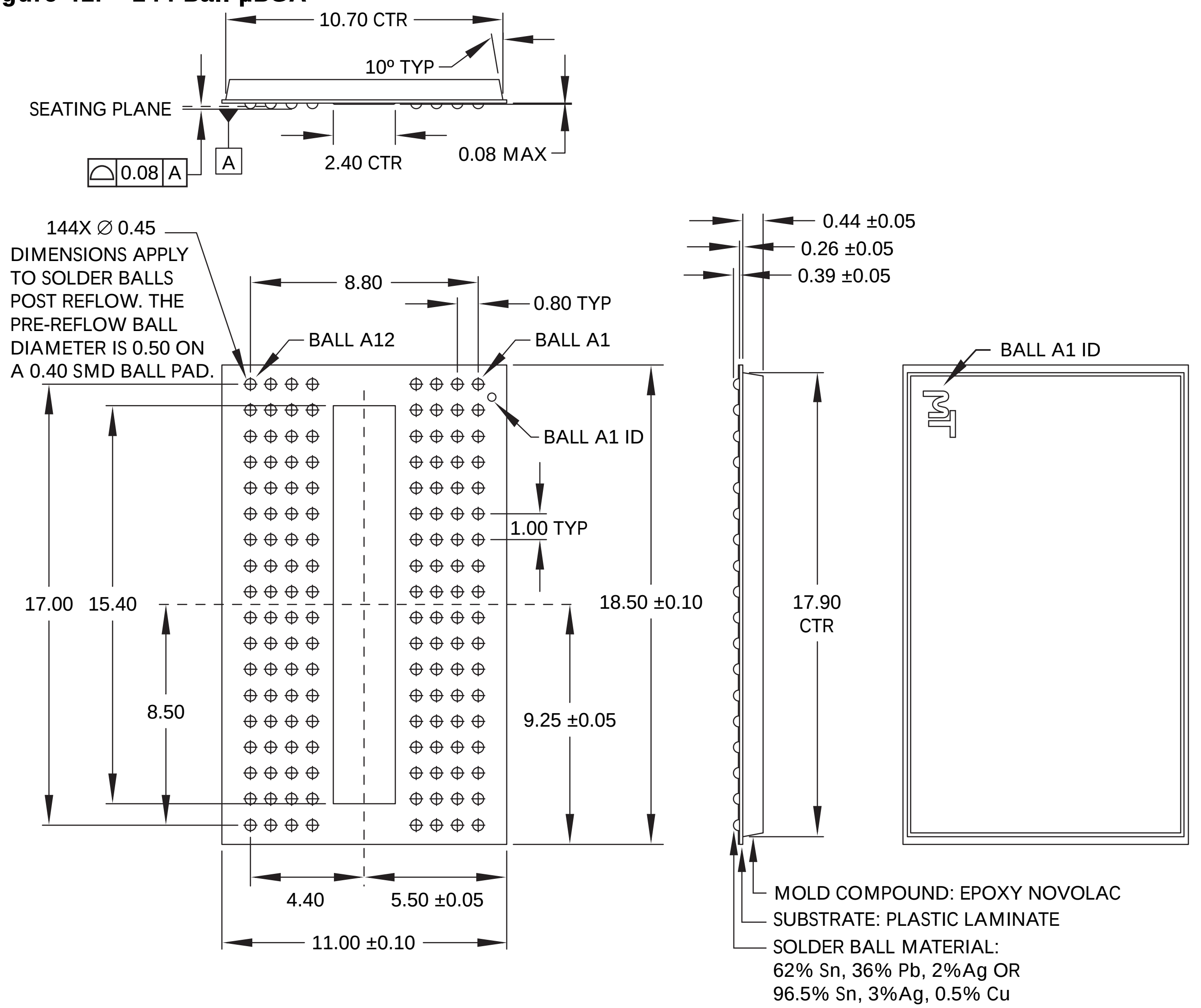
Table 25: IDD Operating Conditions and Maximum Limits
Notes 1–6 on page 47

Description	Condition	Symbol	Max			Units
			-25	-33	-5	
Standby current	tCK = Idle All banks idle, no inputs toggling	ISB1 (VDD) x36	48	48	48	mA
		ISB1 (VDD) x18/x9	48	48	48	
		ISB1 (VEXT)	26	26	26	
Active standby current	CS# = 1 No commands, half bank/address/data change once every four clock cycles	ISB2 (VDD) x36	288	233	189	mA
		ISB2 (VDD) x18/x9	288	233	189	
		ISB2 (VEXT)	26	26	26	
Operational current	BL = 2, sequential bank access, bank transitions once every tRC, half address transitions once every tRC, read followed by write sequence, continous data during WRITE commands.	IDD1 (VDD) x36	374	343	292	mA
		IDD1 (VDD) x18/x9	348	305	255	
		IDD1 (VEXT)	41	36	36	
Operational current	BL = 4, sequential bank access, bank transitions once every tRC, half address transitions once every tRC, read followed by write sequence, continous data during WRITE commands.	IDD 2 (VDD) x36	418	389	339	mA
		IDD2 (VDD) x18/x9	362	319	269	
		IDD2 (VEXT)	48	42	42	
Operational current	BL = 8, sequential bank access, bank transitions once every tRC, half address transitions once every tRC, read followed by write sequence, continous data during WRITE commands.	IDD 3 (VDD) x36	NA	NA	NA	mA
		IDD3 (VDD) x18/x9	408	368	286	
		IDD3 (VEXT)	55	48	48	
Burst refresh current	Eight bank cyclic refresh, continous address/ data, command bus remains in refresh for all eight banks.	IREF1 (VDD) x36	685	545	375	mA
		IREF1 (VDD) x18/x9	680	530	367	
		IREF1 (VEXT)	133	111	105	
Distributed refresh current	Single bank refresh, sequential bank access, half address transitions once every tRC, continous data.	IREF2 (VDD) x36	326	281	227	mA
		IREF2 (VDD) x18/x9	325	267	221	
		IREF2 (VEXT)	48	42	42	
Operating burst write current example	BL = 2, cyclic bank access, half of address bits change every clock cycle, continuous data, measurement is taken during continuous WRITE.	IDD2W (VDD) x36	990	914	676	mA
		IDD2W (VDD) x18/ x9	970	819	597	
		IDD2W (VEXT)	100	90	69	
Operating burst write current example	BL = 4, cyclic bank access, half of address bits change every two clocks, continuous data, measurement is taken during continuous WRITE.	IDD4W (VDD) x36	882	790	567	mA
		IDD4W (VDD) x18/ x9	779	609	439	
		IDD4W (VEXT)	88	77	63	
Operating burst write current example	BL = 8, cyclic bank access, half of address bits change every four clock cycles, continuous data, measurement is taken during continuous WRITE.	IDD8W (VDD) x36	NA	NA	NA	mA
		IDD8W (VDD) x18/ x9	668	525	364	
		IDD8W (VEXT)	60	51	40	
Operating burst read current example	BL = 2, cyclic bank access, half of address bits change every clock cycle, measurement is taken during continuous READ.	IDD2R (VDD) x36	920	850	628	mA
		IDD2R (VDD) x18/x9	902	761	555	
		IDD2R (VEXT)	100	90	69	
Operating burst read current example	BL = 4, cyclic bank access, half of address bits change every two clocks, measurement is taken during continuous READ.	IDD4R (VDD) x36	764	734	527	mA
		IDD4R (VDD) x18/x9	724	566	408	
		IDD4R (VEXT)	88	77	63	
Operating burst read current example	BL = 8, cyclic bank access, half of address bits change every four clock cycles, measurement is taken during continuous READ.	IDD8R(VDD) x36	NA	NA	NA	mA
		IDD8R (VDD) x18/x9	621	488	338	
		IDD8R (VEXT)	60	51	40	

Notes:
1. IDD specifications are tested after the device is prop erly initialized. +0°C ≤ Tc ≤ +95°C; +1.7V ≤ VDD ≤ +1.9V, +2.38V ≤ VEXT ≤ +2.63V, +1.4V ≤ VDDQ ≤ +1.6V, VREF = VDDQ/2.
2. ^{t}CK = ^{t}DK = MIN, ^{t}RC = MIN.
3. Input slew rate is specified in Table 22, DC Electrical Characteristics and Operating Conditions, on page 44.
4. Definitions for IDD conditions:
   a. LOW is defined as VIN ≤ VIL(AC) MAX.
   b. HIGH is defined as VIN ≤ VIH(AC) MAX.
   c. Stable is defined as inputs remaining at a HIGH or LOW level.
   d. Floating is defined as inputs at VREF = VDDQ/2.
   e. Continous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
   f. Continous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
   g. Sequential bank access is defined as the bank address incrementing by one ever ^{t}RC.
   h. Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 4 this is every other clock.
5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more tha n once per clock cycle.
6. IDD parameters are specified with ODT disabled.

Package Dimensions

Figure 41: 144-Ball µBGA



Notes: 1. All dimensions in millimeters.

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Rev. J 8/05

- Updated Table 25, IDD Operating Conditions and Maximum Limits, on page 46.
- Added operating temperature ranges.
- Updated package drawing to include unleaded information.
- Updated template.

Rev H 11/04

- Production status.

Rev G 09/04

- Added updated note to BS table
- QK, QK# description updated (Page 10).
- JTAG logic levels update (Pages 10, 35).
- Timing parameters (Power-up sequence in Figure 7 updated (Page 14).
- Clock Considerations “DLL auto reset” removed (Page 15).
- Figure 8 Vid(DC) and Vid(AC) updated (Page 16).
- Figure 16 QVLD signal corrected (Page 21).On-die termination text updated to include DM pin (Page 27).
- Measured temperature for RTT changed to 70°C TC (Pages 27, 41).
- Figure 27 QVLD signal corrected (Page 27).
- Figure 33 text and notes updated to correct Address bits (Page 31).
- Power-up sequence in Figure 34 updated (Page 31).
- Measured temperatures and range changed to +0°C ≤ TC ≤ +95°C (Pages 37, 38, 41,42, 43).
- TAP DC parameters (VOL1, VOL2, VOH1, VOH2) updated (Page 38).
- I/O Capacitance updated (Page 42).
-