

Motorola NetRAMs

Networking Dual-Ported Memory for the Communications Market

Motorola's NetRAM devices are designed to meet an optimal price and performance point for dual-port applications. These devices enable data to flow quickly so Local Area Network (LAN) and Wide Area Network (WAN) devices can devote more of their resources to application performance

Product Description

The NetRAM family is offered in 1, 4, and 8 Mb densities. The NetRAM allows the user to concurrently perform reads or writes in combination on the two data ports. The two address ports determine the read or write locations for their respective data ports.

The synchronous design allows for precise control with the use of a single external clock. Chip enables, addresses, input data, and write enables for each port are registered on the rising edge of the clock. The output enable for each port is asynchronous in nature.

For the case when the addresses for each port are the same, certain protocols are followed. If both ports are read, the reads occur normally. If one port is writing and the other is being read, the read from the array will occur before the new data is written. If both ports are writing, only the data from Port-Y will be written to the array.

Functional additions have been made to successive generations of the NetRAM to allow the user more flexibility in design. The 4 Mb device offers two chip enables for each port over the single pair of chip enables for each 1 Mb device. The 8 Mb NetRAM adds a third chip enable per port and byte write capability.

Product Highlights

- Single Clock Operation
- Self-Timed Write
- Pipelined Read Operation
- Two Bi-Directional Data Buses
- Asynchronous Output Enables

Applications

- ATM
- Routers
- Cell / Frame Buffers
- RAID Systems
- Ethernet Switches
- Cellular Base Stations
- SNA Switches



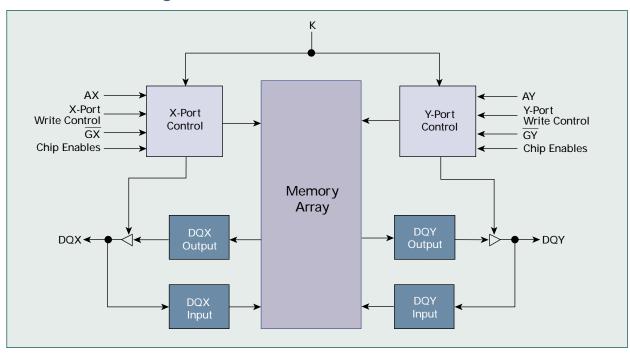
NetRAM Family Summary

| Density | 1 Mb | 4 Mb | 8 Mb |
|---------------------------|---------------------------------|------------------------|-------------------------------|
| Configuration | 32K x 36 and 64K x 18 | 128K x 36 | 256K x 36 |
| PowerSupply | 3.3V ± 5% | 3.3V ± 5% | 3.3V ± 5% and 2.5V ± 200mV |
| Write Operation | Self-Timed Early Write | Self-Timed Early Write | Self-Timed Early Write |
| Read Operation | Pipelined | Pipelined | Pipelined |
| Deselect | Dual Cycle | Dual Cycle | Dual Cycle |
| Port-to-Port Pass Through | Yes | Yes | No |
| Byte Write Capability | No | No | Yes |
| Operating Frequency | 66, 83, 100 MHz | 100, 133 MHz | 100 MHz |
| Package | 176 TQFP (100 TQFP for x 18) | 176 TQFP | 209 MAPBGA |



Freescale Semiconductor, Inc.

NetRAM Block Diagram



Contact Information

Motorola offers data sheets, application notes and models for Fast Static RAM products. In addition, more information is provided for these products at:

http://mot-sps.com/products

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center: phone: 800-521-6274 or

http://www.motorola.com/semiconductors

^{© 2000} Motorola, Inc. All rights reserved. Printed in the U.S.A. Motorola, the 🕙, and Digital DNA and the Digital DNA logo are registered trademarks of Motorola, Inc. This document contains information on a new product under development. Specifications and information herein are subject to change without notice.