Features

- **1024 x 1024 Pixels with Memory Zone**
- **Up to 30 Images/Second**
- **Built-in Antiblooming Device Providing an Electric Shutter Function**
- **Pixel: 14 µm x 14 µm**
- **Image Zone: 14.34 x 14.34 mm^2**
- **Two Outputs at 20 MHz Each**
- **Readout Through 1 or 2 Outputs**
- **Possible Binning 2 x 2**
- **Optical Shield Against Parasitic Reflexions and Stray Light**
- **A/R Window in 400 - 700 nm Bandwidth**

Description

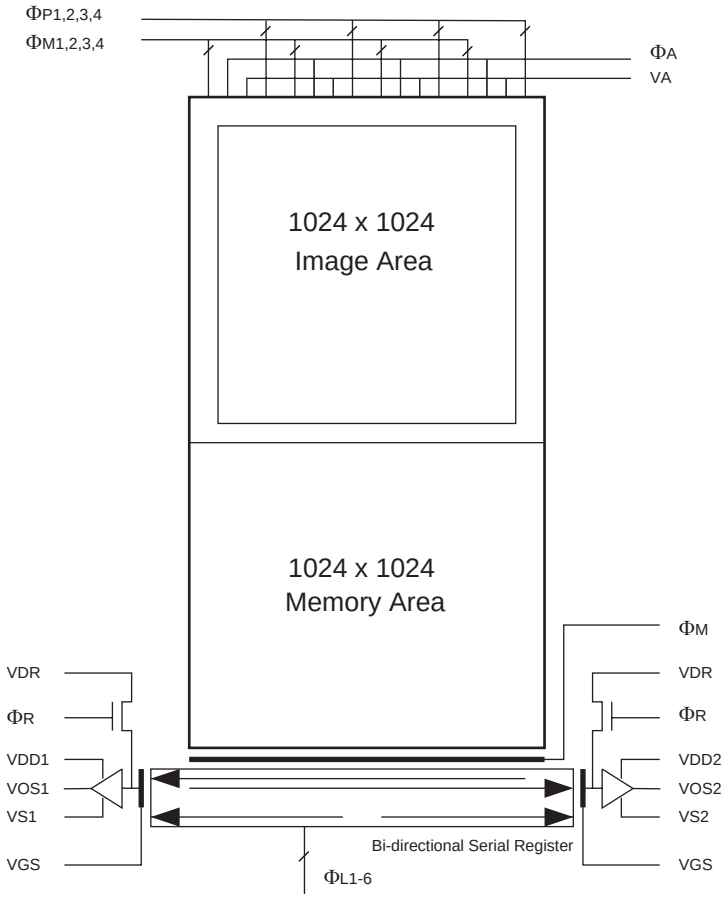
The TH7888A is particularly designed for high data rate applications (up to 30 pictures/second in 1024 x 1024 progressive scan format) in the medical and industrial fields. This area array image sensor consists of a 1024 x 1024 pixels (14 µm x 14 µm) image zone associated with a memory zone (masked with an optical shield). To increase the data rate, two separate outputs are provided, which can be used for parallel readout (the readout frequency is up to 20 MHz/output, leading to a total readout frequency of 40 MHz). These two outputs allow three readout modes (single or dual port). The TH7888A is designed with an antiblooming structure which provides an electronic shutter capability. Moreover, the 2 x 2 binning mode is available on this sensor, providing an image size of 512 x 512 pixels with 28 µm x 28 µm pixels. The TH7888A package is sealed with a specific anti-reflective window optimized in the 400 - 700 nm spectrum bandwidth on the sealed version.

Area Array CCD Image Sensor (1024 x 1024 Pixels with Antiblooming)

TH7888A

Rev. 1999A–IMAGE–09/03

Figure 1. TH7888A General Sensor Organization



Functional Overview

Extra dark lines are provided for use as dark references or for smearing digital correction.

Extra dark pixels are provided for dark line reference clamping. Each frame consists of 1056 video lines:

- 1 dummy line
- 12 useful dark reference lines (with optical shield)
- 3 isolation lines
- 1024 useful lines
- 3 isolation lines
- 12 dark reference lines (with optical shield)
- 1 dummy line

Each video line is made up of 546 or 1058 elements, depending on the readout mode (single or dual port mode):

- 12 inactive prescan elements
- 1 isolation prescan element
- 16 useful dark references (with optical shield)
- 5 isolation elements
- 512 or 1024 useful video pixels

Pin Description

Figure 2. Pin Overview

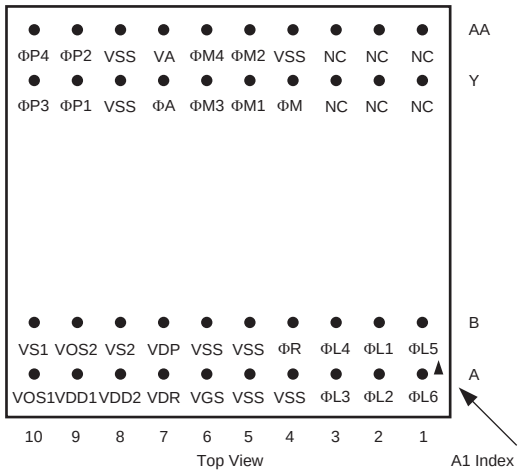


Table 1. Pin Description

Pin Number	Symbol	Designation
Y9	ΦP1	Image zone clocks
AA9	ΦP2	
Y10	ΦP3	
AA10	ΦP4	
Y5	ΦM1	Memory zone clocks
AA5	ΦM2	
Y6	ΦM3	
AA6	ΦM4	
Y4	ΦM	Memory to register clock
B2	ΦL1	Readout register clocks
A2	ΦL2	
A3	ΦL3	
B3	ΦL4	
B1	ΦL5	
A1	ΦL6	
A9	VDD1	Output amplifier drain supply
A8	VDD2	
B10	VS1	Output amplifier source supply
B8	VS2	
B7	VDP	Protection drain bias
A6	VGS	Register output gate bias
A10	VOS1	Video outputs
B9	VOS2	
B4	ΦR	Reset clock

Table 1. Pin Description (Continued)

Pin Number	Symbol	Designation
Y7	ΦA	Antiblooming gate clock
A7	VDR	Reset bias
AA7	VA	Antiblooming diode bias
A4, A5, B5, B6	VSS	Substrate bias
Y8, AA4, AA8	VSS	

Geometrical Characteristics

Figure 3. Pixel Layout

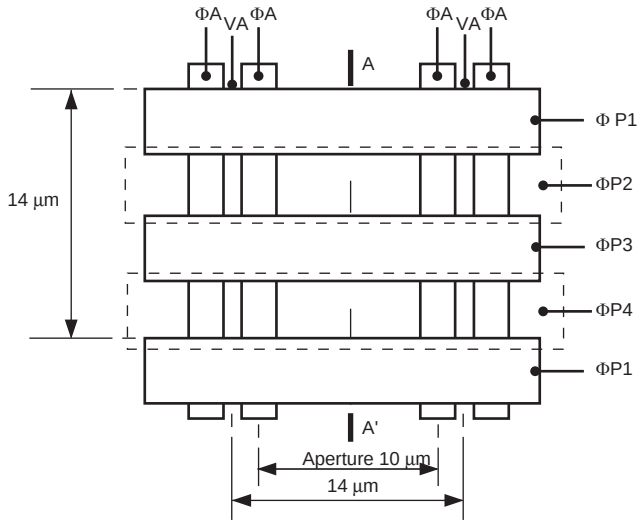
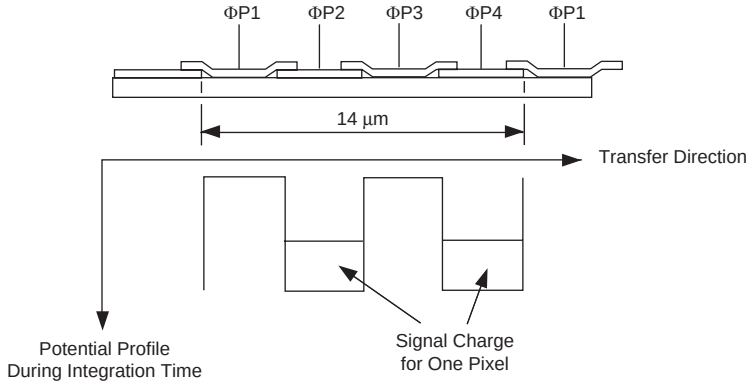


Figure 4. AA Cross Section



Absolute Maximum Ratings*

Storage Temperature	-55°C to +150°C
Operating Temperature	-40°C to +85°C
Thermal Cycling	15°C/mn
Maximum Applied Voltages:	
• Pins: Y9, AA9, Y10, AA10, Y5, AA5, Y6, AA6, Y4, B2, A2, A3, B3, B1, A1, B4, A6	-0.3 V to 15 V
• Pins: A9, A8, B10, B8, B7, A7, AA7	-0.3 V to 15.5 V
• Pin: Y7	-0.3 V to 12 V
• Pins: A4, A5, B5, B6, Y8, AA4, AA8	0 V (ground)

*NOTICE: *Stresses above those listed under absolute maximum ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Operating range defines the limits within which functionality is guaranteed. Electrical limits of applied signals are given in the operating conditions section.

Operating Precautions

Shorting the video outputs to any pin, even temporarily, can permanently damage the on-chip output amplifier.

Operating Conditions

Table 2. DC Characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output amplifier drain supply	VDD1, VDD2	14.5	15	15.5	V
Protection drain bias	VDP	14.5	15	15.5	V
Reset bias	VDR	14.5	15	15.5	V
Antiblooming diode bias	VA	14.5	15	15.5	V
Register output gate bias	VGS	2.2	2.5	2.8	V
Output amplifier source supply	VS1(2), VS2		0		V
Ground(1)	VSS(2)		0		V

Notes: 1. Ground: note that the package metal back is grounded.
2. In dynamic mode, to avoid possible damage to the device, the addition of a Schottky diode is recommended (for example; diode reference BAR 43S) between VS1 and VSS ground in order to increase the potential on VS1, thus avoiding any direct mode diode current during clock transitions.

Readout Mode

The serial readout register is operated in a two-phase transfer mode. However, there are 6 separate command electrodes that should be connected differently, depending on the required readout mode. The following table gives the connections to be made for each mode.

Table 3. Readout Modes

Readout Modes / Drive Clocks (Signals)	1 Output, VOS 1	1 Output, VOS2 (Mirror Effect)	2 Outputs (Parallel)
ΦL1	Pins B2, B3, B1	Pins B2, A3, A1	Pins B2, B3, A1
ΦL2	Pins A2, A3, A1	Pins A2, B3, B1	Pins A2, A3, B1

Table 4. Timing Parameters

Definition	Symbol	Comments
Vertical transfer period	T_V	Nominal value = 800 nm
Vertical transfer subdivision	T_O	Tv = 8 x To
Rise time	tr	For vertical transfer clocks (between 10% and 90% of the transition time)
Fall time	tf	
Readout register clock transition time	t1	
Reset clock transition time	t2	
Delay between output reset signal and reset clock	td	

Timing Diagrams

The following diagrams describe the 20 MHz readout frequency and 1.25 MHz vertical transfer frequency.

Figure 5. Frame Timing Diagram

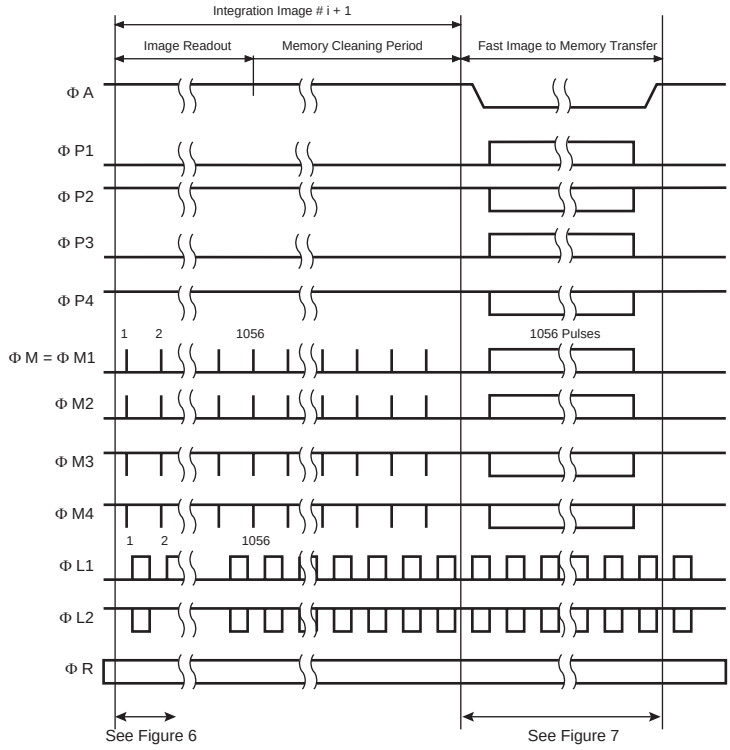
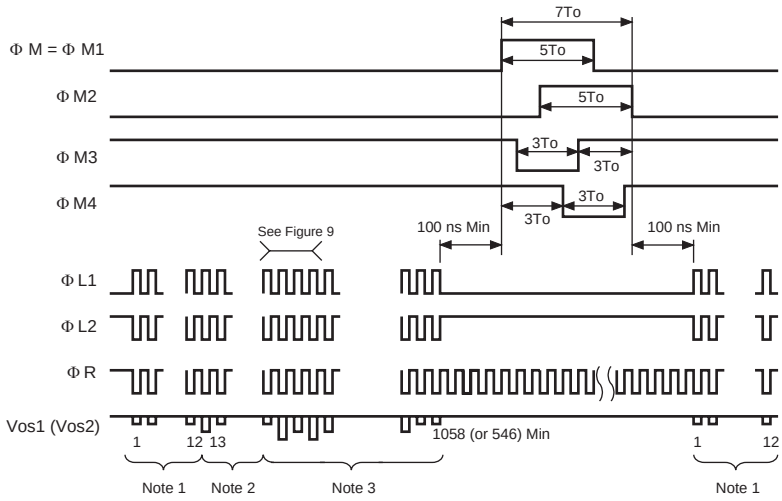


Figure 6. Line Timing Diagram



Notes:
1. 12 pre-scan elements
2. 1 isolation element, 16 dark reference pixels, 5 isolation elements
3. 1024 useful video pixels (single output readout mode), 512 useful video pixels (dual output readout mode)

Figure 7. Vertical Transfer During Image to Memory Zone Transfer

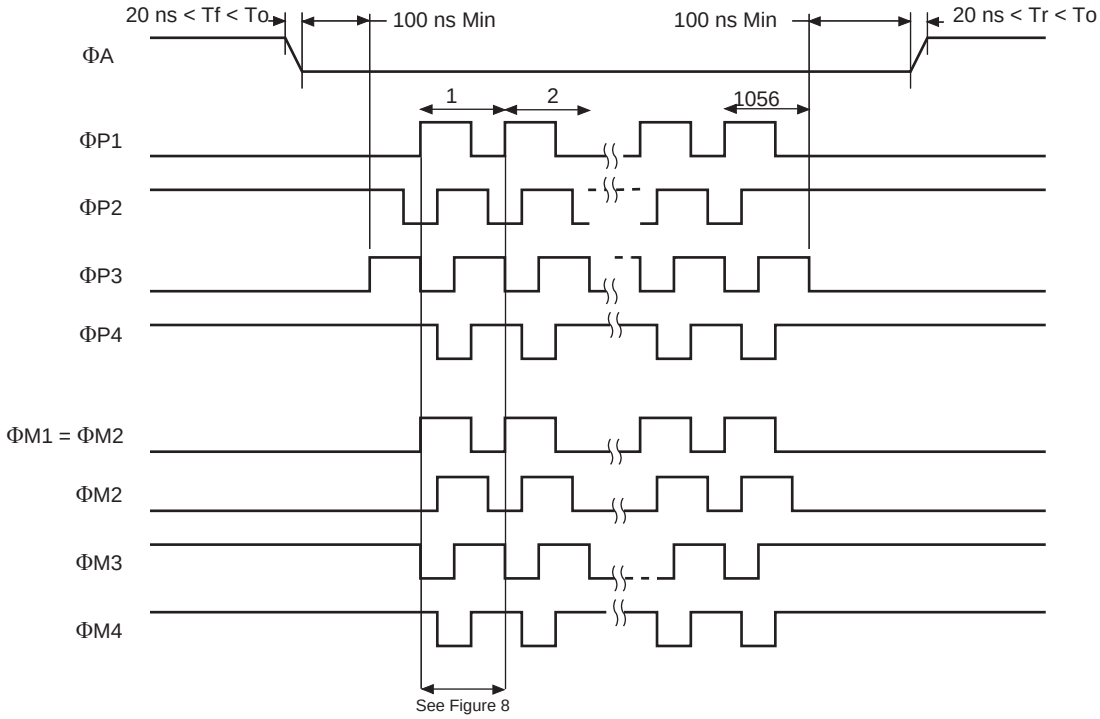
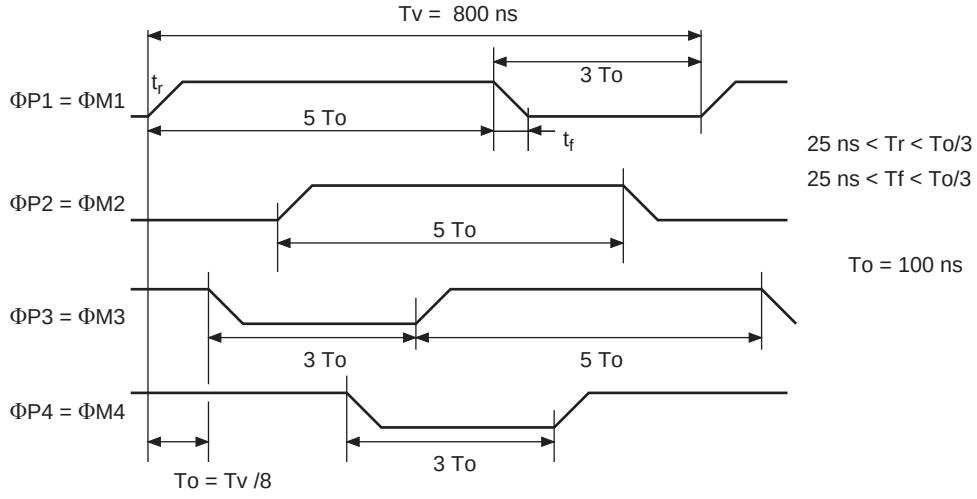
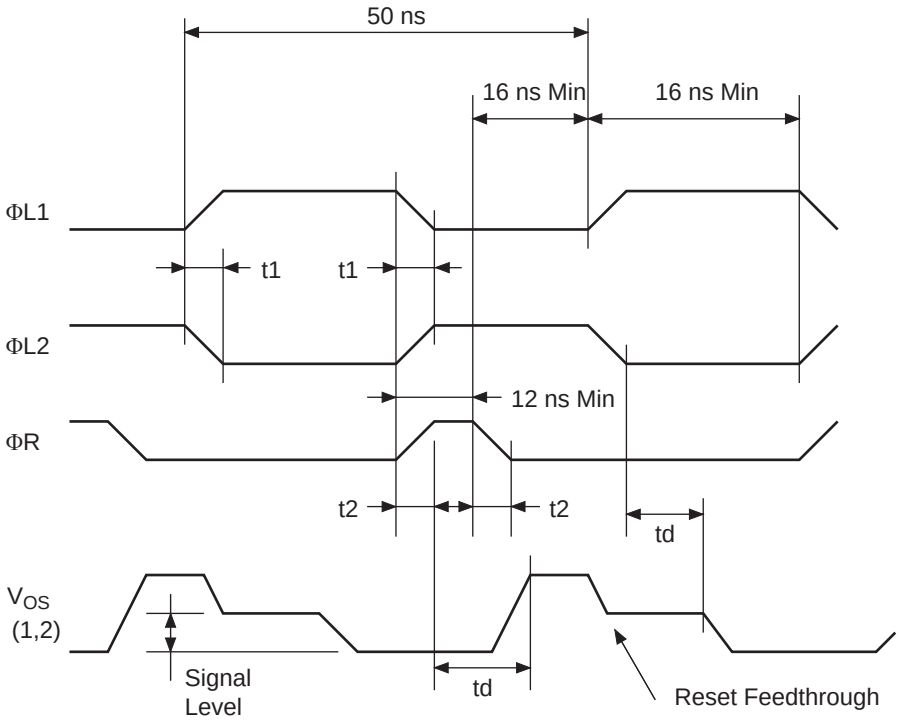


Figure 8. Transfer Period from Image Zone to Memory Zone (ΦP and ΦM for 1.25 Vertical Transfer Frequency FV = 1: Tv)



Note: Tr = Rise time
Tf = Fall time
To = Vertical transfer time subdivision
Tv = Vertical transfer period.

Figure 9. Output Diagram for Readout Register and Reset Clock 20 MHz Applications
Crossover of Complementary Clocks (ΦL1, ΦL2). Between 30% and 70% of Maximum Amplitude.

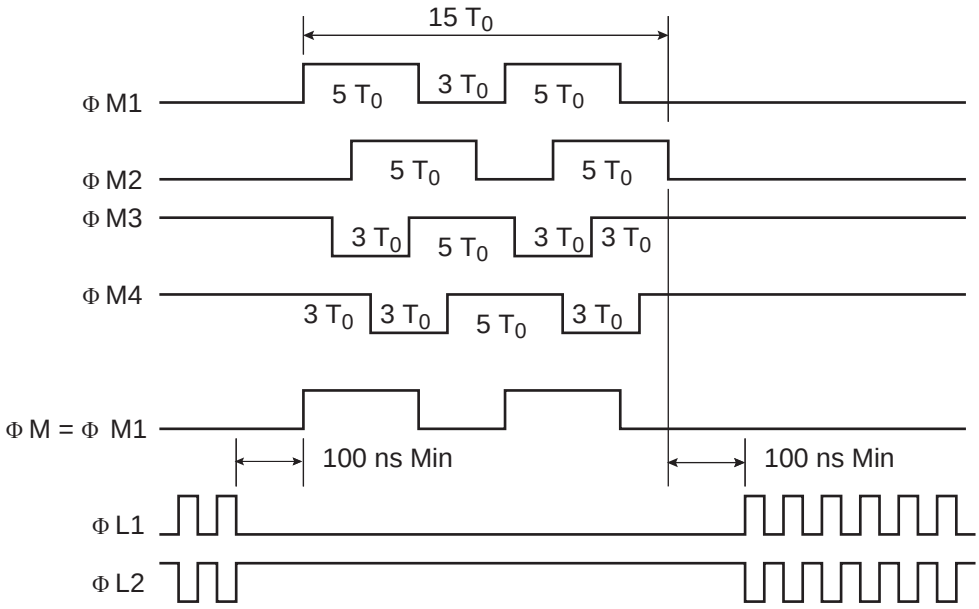


Note: t1 = 7 ns typical
t2 = 5 ns typical
td = 8 ns typical delay time

Binning Mode Operation

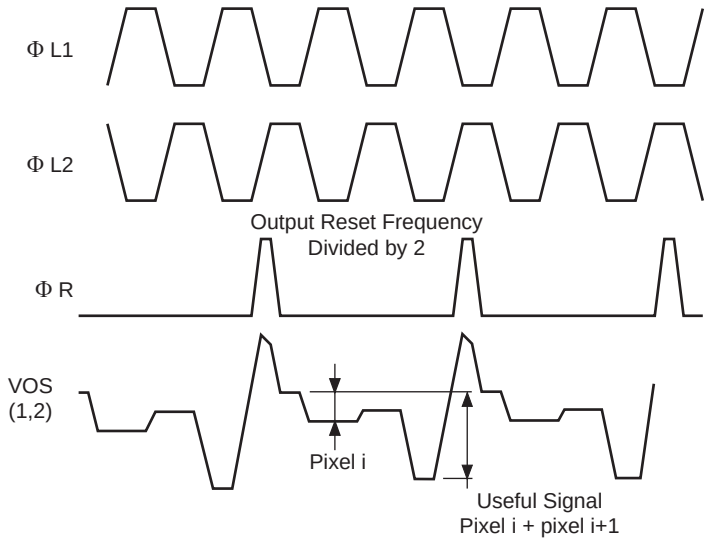
In binning mode operation, the image is composed of 512 x 512 pixels (28 µm x 28 µm each).

Figure 10. Summation in the Readout Register of Two Adjacent Lines



Note: To view fall and rise times see Figure 8 on page 8

Figure 11. Summation of Two Adjacent Pixels



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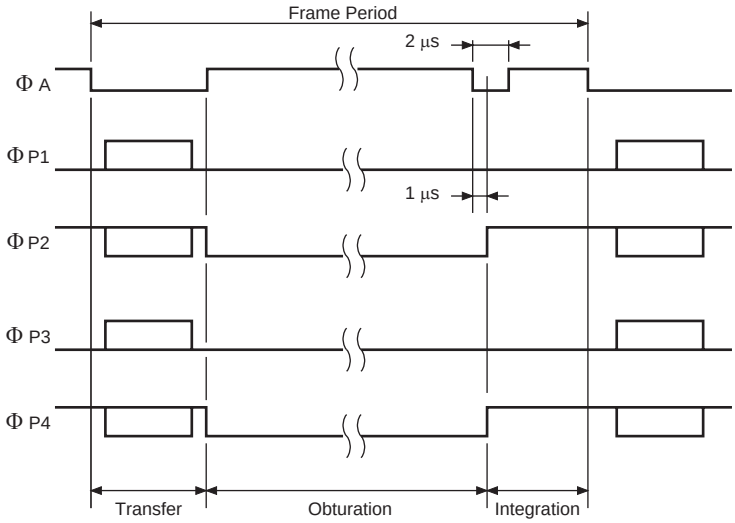
Exposure Time Reduction

The TH7888A provides an exposure time control (electronic shutter) function.

The exposure time reduction is achieved by pulsing all the ΦPi gates to 0 V to continuously remove all the photogenerated electrons through antiblooming drain VA.

Figure 12. Timing Diagram for Electronic Shutter



Note: To view fall and rise times see Figure 6 on page 7

Table 5. Drive Clock Characteristics

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Image zone clocks	ΦP1, 1, 3, 4					Typical input capacitance
High level		7.5	8	8.5	V	15 nF
Low level		0	0.5	0.8	V	See Figure 12
Memory zone clocks	ΦM1, 2, 3, 4					Typical input capacitance
High level		7.5	8	8.5	V	15.5 nF
Low level		0	0.5	0.8	V	See Figure 12
Memory register clocks	ΦM					Typical input capacitance
High level		8.5	9	9.5	V	10 pF
Low level		0	0.5	0.8	V	
Antiblooming gate	ΦA					Typical input capacitance
High level (integration)		3	4	7	V	14 nF
Low level (transfer)		0	0.5	0.8	V	See Figure 12 and Figure 14
Reset gate	ΦR					Typical input capacitance
High level		10	12	13	V	10 pF
Low level		0	2	3	V	
Readout register clocks	ΦL1, 2					
High level		8.5	9	9.5	V	
Low level		0	0.5	0.8	V	
Maximum readout register frequency	F_H	20	–	–	MHz	See Figure 9
Maximum image zone to memory zone Transfer frequency	F_V	1.7	–	–	MHz	See Figure 14

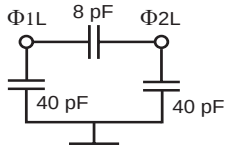


Figure 13. Drive Clocks Capacitance Network

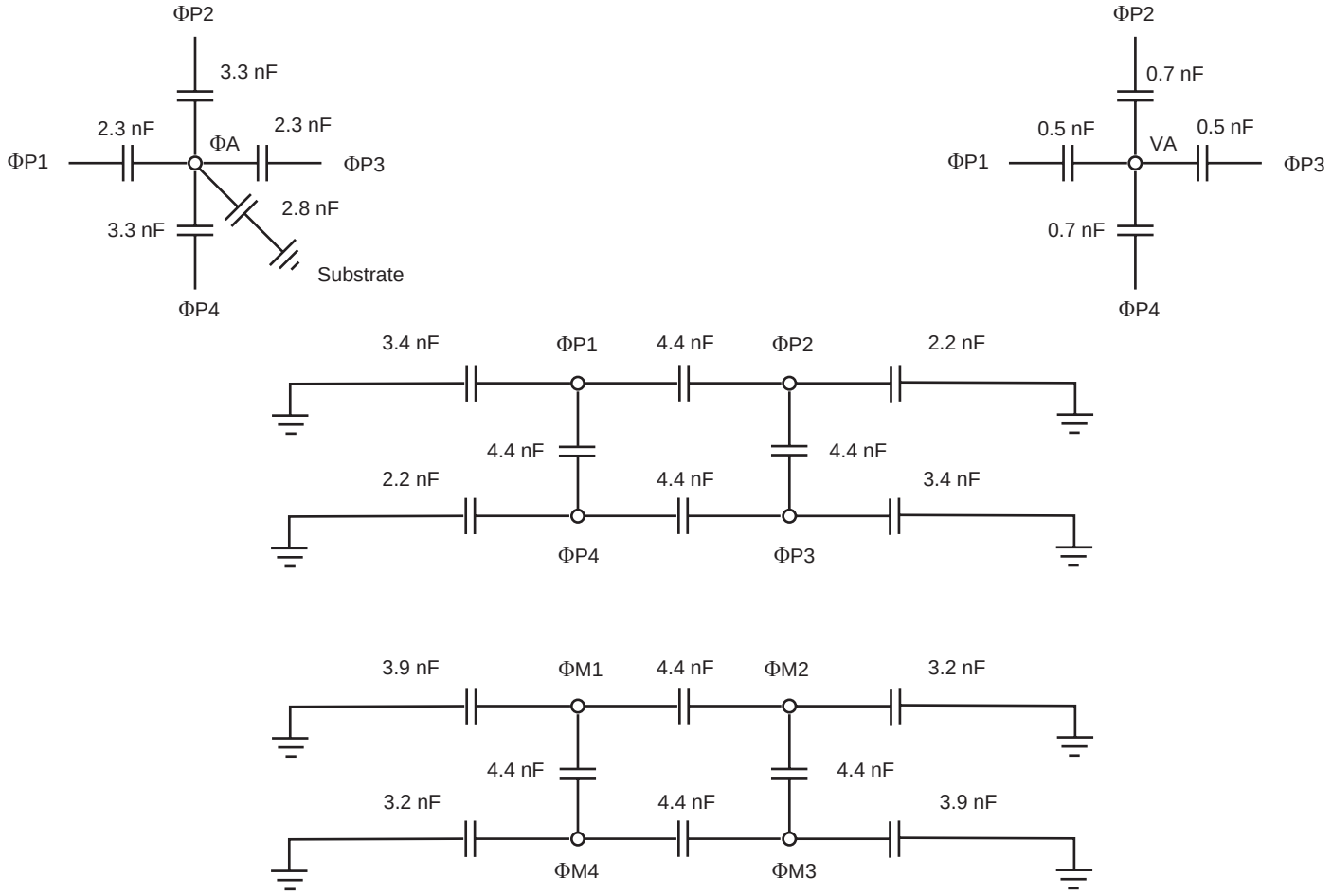


Table 6. Static and Dynamic Electrical Characteristics

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Output amplifier supply current	I_{DD}		10	15	mA	per amplifier
Output impedance	Z_S	200	225	250	Ω	
DC output level	V_{REF}		11		V	
Output conversion factor	CVF	5.5	6	6.5	µV/e-	

Electro-optical Performance

- General conditions:
  Temp = 25°C (package temperature)
  Light source: 2854 K with 2 mm BG38 filter (unless specified) + F/3.5 optical aperture.
  30 images per second mode (Ti = 33 ms) under typical operating conditions
- Readout mode: 2 outputs
- Values exclude dummy elements and blemishes

Table 7. Performance Description and Values

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Output register saturation level	V_{SAT} reg	–	2.6	–	V	
Pixel saturation level	V_{SAT}	1.6	1.9	3	V	(1)
Pixel saturation charge (electron per pixel)	Q_{SAT}	–	320	–	ke-	
Responsivity at 640 nm Responsivity with BG38 filter	R	– 3	6.5 4	– –	V/(µJ/cm^2) V/(µJ/cm^2)	
Quantum efficiency at 640 nm	QE	–	15	–	%	See Figure 17
Photo response non uniformity (1σ)	PRNU	–	0.4	1.7	%Vos	
Dark signal non uniformity (1σ)	DSNU	–	0.28	0.4	mV	(2)
Average dark signal	V_{DS}	–	2	3	mV	(3)
		–	4	5.6	mV	(4)
Temporal RMS noise in darkness (last line)	V_N	–	200	–	µV	(5)
Dynamic range	D	–	80	–	dB	(6)
Horizontal modulation transfer function at 500 nm	MTF	–	70	–	%	(7)
Vertical charge transfer inefficiency (per stage)	VCTI	–	–	$2.5.10^{-5}$	–	(8)
Horizontal charge transfer inefficiency (per stage)	HCTI	–	–	5.10^{-5}	–	(9)

Notes:
1. Pixel saturation (full well) as a function of vertical transfer frequency (see Figure 14 on page 15) and antiblooming adjustment (see Figure 15 on page 15).
2. After substraction of dark signal slope due to memory readout time.
3. First line level referenced from inactive prescan elements (12 samples).
4. Last line level referenced from inactive prescan elements (12 samples).
5. Measured with Correlated Double Sampling (CDS) including 160 µV readout noise and dark current noise in general test conditions.
6. Saturation to RMS noise in darkness ratio.
7. At Nyquist frequency.
8. VSAT/2 measurement and 417 kHz vertical transfer frequency.
9. VSAT/2 measurement and 10 MHz horizontal transfer frequency.

Figure 14. Saturation Level by Full Well with Antiblooming Off (ΦA High = 0 V) Versus the Vertical Transfer Frequency

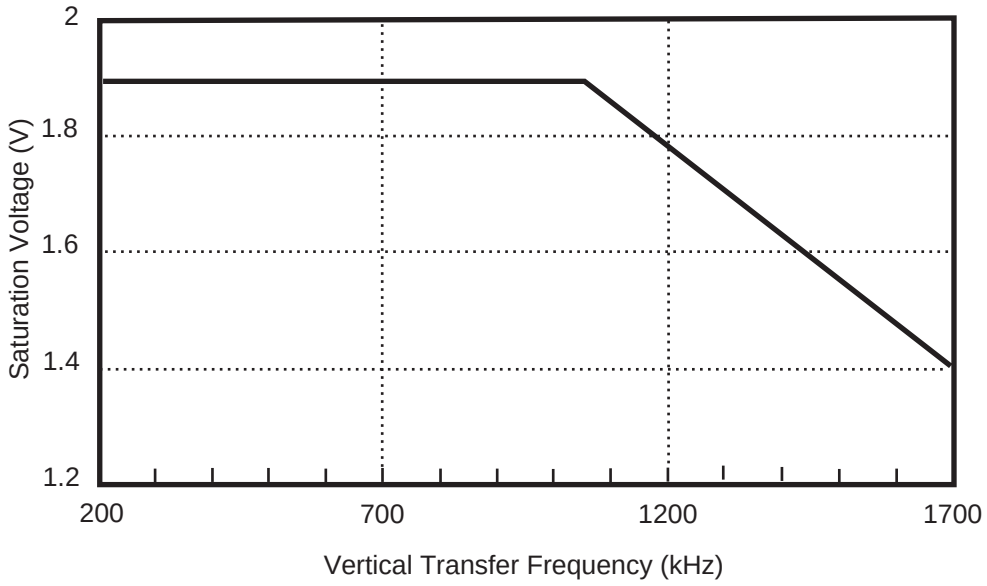


Figure 15. Saturation Level Limitation by the Antiblooming Effect on the Pixel (Typical Operating Conditions)

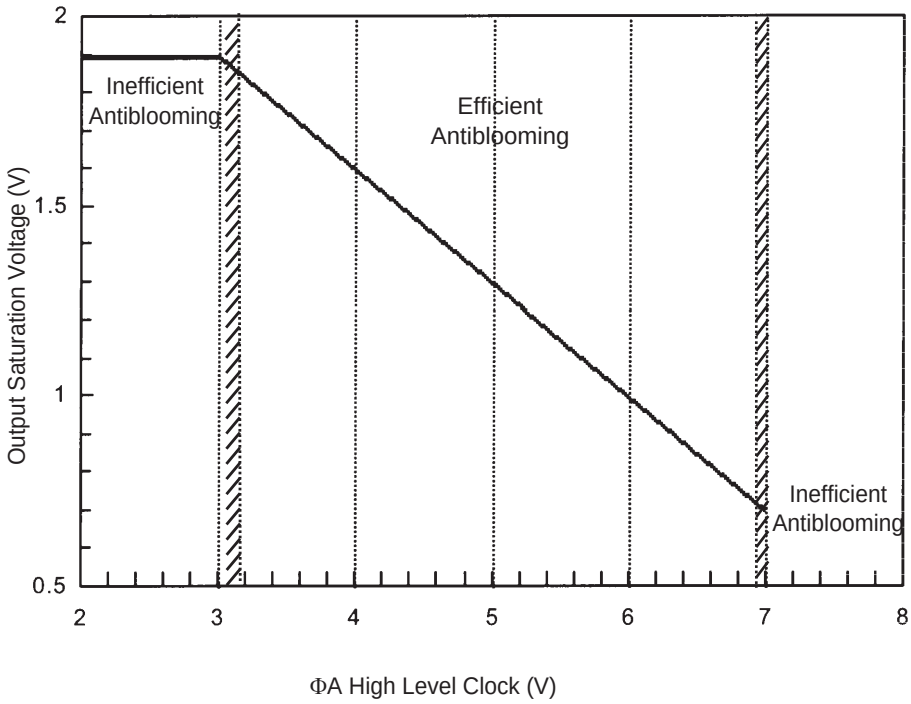
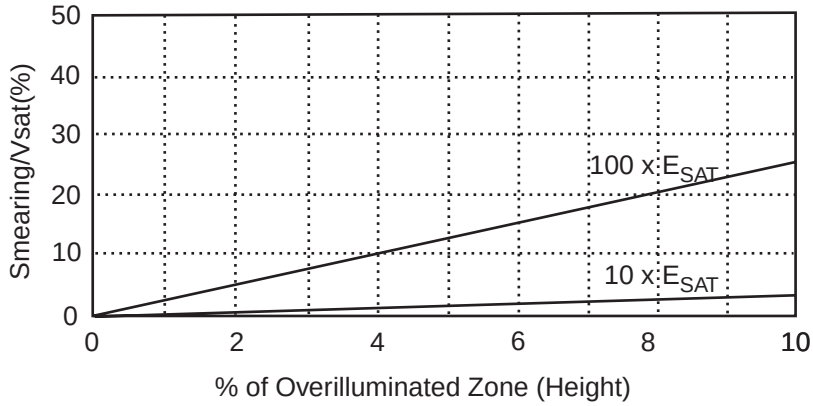


Figure 16. Smearing Effect



N_{ESAT} = number of times E_{SAT}

$$\frac{V_{SMEARING}}{V_{SAT}} = N_{ESAT} \times \frac{T_V}{T_I} \times H$$

with $E_{SAT} = V_{SAT}$/responsivity
(typical illumination conditions)

- Ti = integration time
- Tv = image to memory transfer time

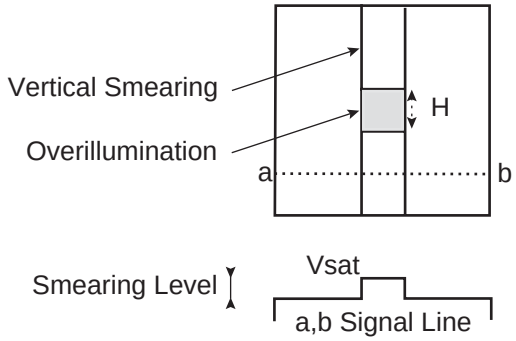


Figure 17. Spectral Response with A/R Window (Typical Case)

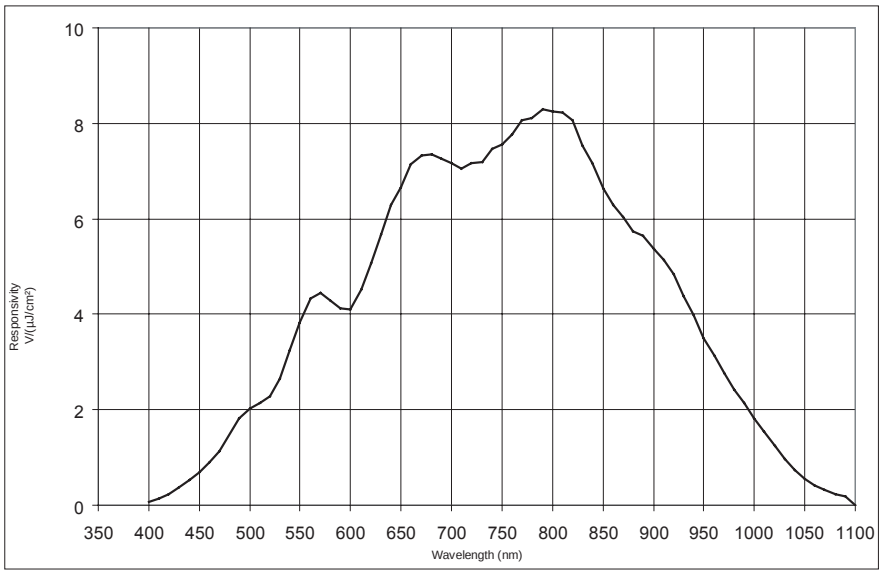


Image Quality Grade

Blemish Maximum area of 2 x 2 defective pixels.

Clusters Less than 7 contiguous defects in a column.

Columns More than 7 contiguous defects in a column.

General Conditions

Room Temperature .....25°C

Frequency 30 images/s(under typical operating conditions)

Considered image zone .....1024 x 1024

Light Source 2854K with BG38 filter + F/3.5 optical aperture

At Vos = 0.7 Vsat

Type	White	Black
Blemishes/clusters	α > 20% $\overline{V}$os	$\|\alpha\|$ > 30% $\overline{V}$os
Columns	α > 10% $\overline{V}$os	$\|\alpha\|$ > 10% $\overline{V}$os

In Darkness

Blemishes/clusters	α > 10 mV (*)
Columns	α > 5 mV (*)
(*) reference is Vo: average darkness signal	

Number of Defects

Total pixel numbers affected by blemishes and clusters 100

Maximum number of clusters.....10

Maximum number of columns.....5

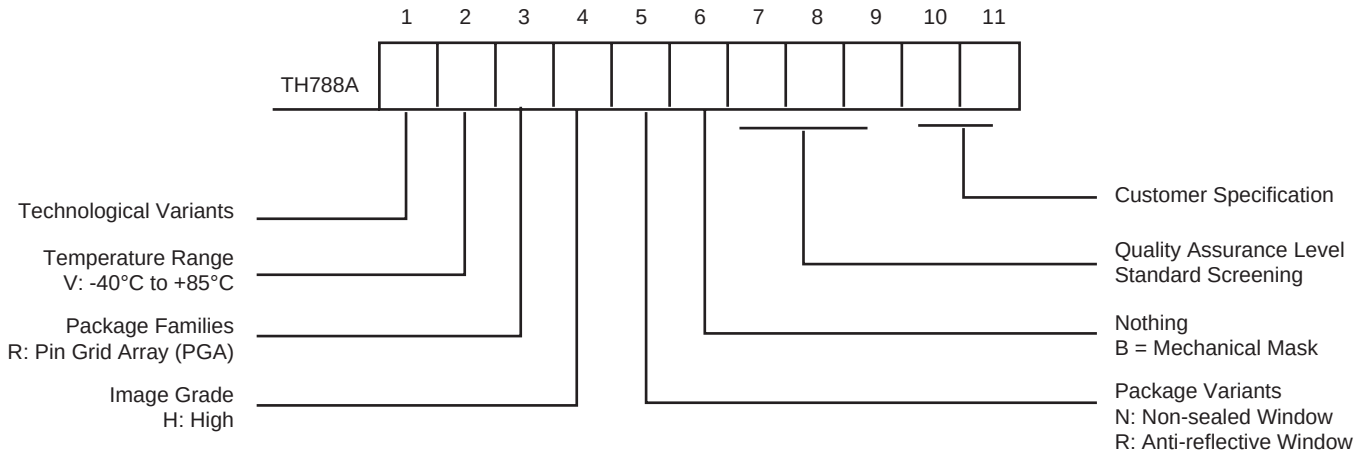
α: amplitude of video signal of defect with respect to mean output voltage $\overline{V}os$

Ordering Codes

TH7888AVRHRB: sealed version

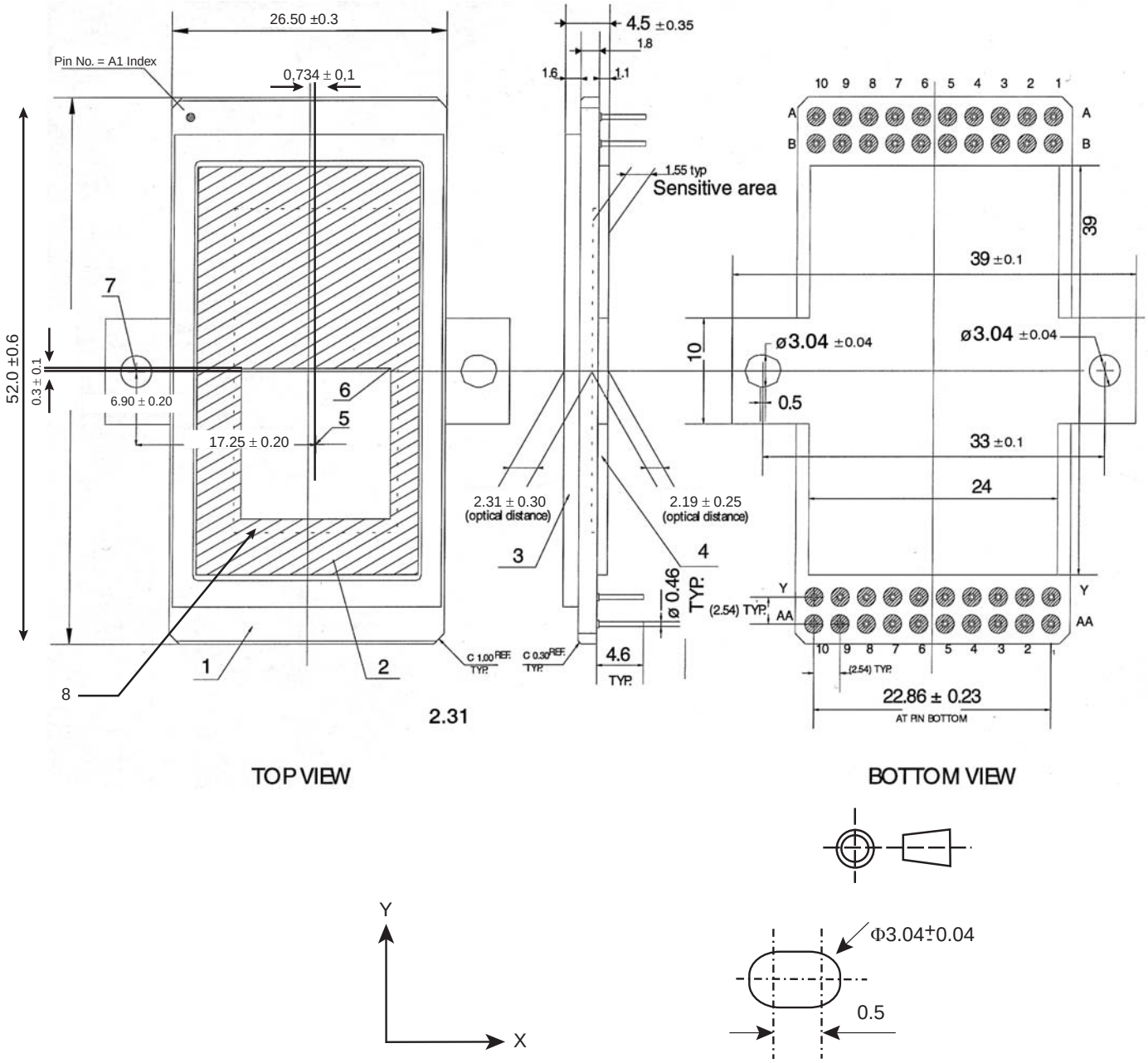
TH7888AVRHN: unsealed version

Figure 18. Ordering Information Key



Package Outline

Figure 19. Package Drawing for 40-lead PGA



Notes:
1. All values are in mm.
2. Black alumina 40-lead PGA package
3. Black optical mask (only on sealed version)
4. 400 nm – 700 nm AR coated window (R < 1% per side). Only on sealed version
5. Metal back, (CuW – copper tungsten) gold plated. Electrically grounded (VSS)
6. Optical center
7. First useful pixel (readout through Vos1)
8. Mechanical reference
9. Photosensitive area dimensions 14,392(X) x 14,358(Y)

Parameter	Mechanical Distance	Optical Distance	Unit
Z_{top}	2.82 ± 0.31	2.31 ± 0.30	mm
Z_{bottom}	1.68 ± 0.15	2.19 ± 0.25	mm

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