3547860 FERRANTI ELECTRIC INC

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T-51-09-05

Triple 4-bit video D-A converter

ADVANCE PRODUCT INFORMATION

ZN454CJ

FEATURES

- 3 video DAC's - Ideal for colour graphics
- Fast, 8ns settling time
- Update rates to 100MHz
- Low glitch energy
- ¼LSB linearity error
- On-chip reference source
- Composite sync and blank inputs
- TTL compatible inputs
- Generates standard video signal output across a doubly terminated 75Ω load
- 28 pin DIL package

DESCRIPTION

The ZN454CJ consists of three 4-bit D-A converters, providing a colour palette of 4096 possible display colours. The required logic translators, control logic, a reference voltage source and reference amplifier are also integrated on-chip.

Each D-A converter accepts 4-bit digital video data and SYNC/BLANK signals directly from a TTL source and produces a composite video output to directly drive a 75Ω line terminated by a 75Ω load at both ends.

The ZN454CJ is ideally suited for pixel colour generation in graphics display systems requiring 4-bit colour resolution. The high linearity of each DAC ensures excellent colour contrast and the fast update rate allows the device to be interfaced to monitors with a resolution of up to 1024 × 1280 pixels assuming a standard refresh rate of 60Hz.

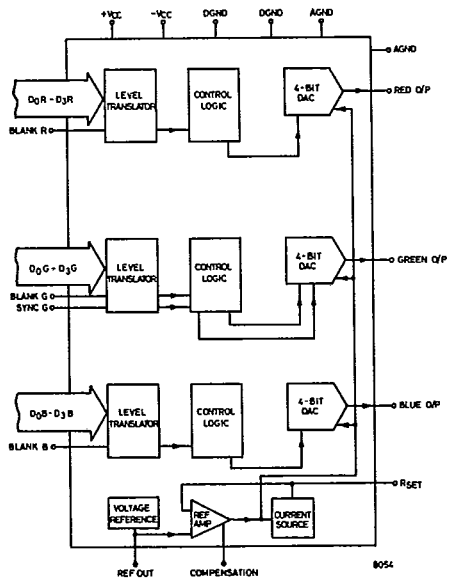

Fig. 1 System diagram

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ABSOLUTE MAXIMUM RATINGS

Supply voltage $+V_{CC}$	+6V
$-V_{CC}$	−6V
Logic input voltage	$+V_{CC}$
Operating temperature range	0 to +70°C
Storage temperature range	−55 to +125°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C, V_{CC} = ±5V, R_L = 37.5Ω and R_{SET} = 180Ω unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolution		4	–	–	Bits	
LSB weight (current)			1.13		mA	Note 1
LSB weight (voltage)			43		mV	Note 1
ACCURACY						
Linearity error			±0.25	±0.5	LSB	
Differential linearity error				±0.5	LSB	Note 2
Offset error			−5.0	−15.0	mV	
Gain error				±5	% of nom. FSR	
SPEED PERFORMANCE – GREY SCALE OUTPUT						
Rise/Fall times (voltage)			3	5	ns	10-90% of final value
Settling time (voltage)			8		ns	Note 3
Maximum update rate			100		MHz	Note 4
Slew rate			180		V/μs	10-90% of final value
Glitch energy			60		pV-s	Note 5
TEMPERATURE COEFFICIENT						
Offset			10		ppm/°C	measured with internal reference
Gain			500		ppm/°C	measured with internal reference
DATA, SYNC & BLANK INPUTS						
Logic compatibility			TTL			
High level input voltage	V_{IH}	2.0	–	–	V	
Low level input voltage	V_{IL}	–	–	0.8	V	
High level input current	$I_{IH(1)}$	–	–	+20	μA	V_{CC} = max, V_{in} = 5.5V
	$I_{IH(2)}$	–	–	±10	μA	V_{CC} = max, V_{in} = 2.4V
Low level input current	I_{IL}	–	–	−1.6	mA	V_{CC} = max, V_{in} = 0.4V

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ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Coding (see Fig. 2)			Complementary binary			
OUTPUT – GREY SCALE						
Voltage range			0.64		V	Note 1
Current range			17		mA	Note 1
OUTPUT – COMPOSITE SYNC						
Voltage range			286		mV	
Current range			7.6		mA	
OUTPUT – COMPOSITE BLANKING						
Voltage range			71		mV	
Current range			1.9		mA	
OUTPUT VOLTAGE COMPLIANCE		0		1.5	V	
INTERNAL VOLTAGE REFERENCE						
Output voltage	V_{REF}		−1.22		V	
Output voltage tolerance				±3.0	%	
Output voltage T.C.			200		ppm/°C	0 to 70°C
POWER SUPPLY REQUIREMENTS						
Supply voltage	$+V_{CC}$	4.5	5.0	5.5	V	
	$-V_{CC}$	−4.5	−5.0	−5.5	V	
Supply current	$+I_{CC}$		35	50	mA	
	$-I_{CC}$		170	185	mA	

NOTES

Note 1 LSB and full-scale output levels adjustable with R_{SET}.

Note 2 Monotonicity guaranteed over full operating temperature range.

Note 3 The settling time was measured as the time between the start of the output rising/falling edge to where the output entered and remained within ± ½LSB of the final value. The value quoted is for a transition from reference white to reference black and vice versa, and does not include the inherent input propagation delay (2-3ns). See section describing settling time measurement.

Note 4 The maximum update rate is limited by the full-scale settling time to rated accuracy.

Note 5 Measurement of glitch energy is discussed in a later section of this data sheet.

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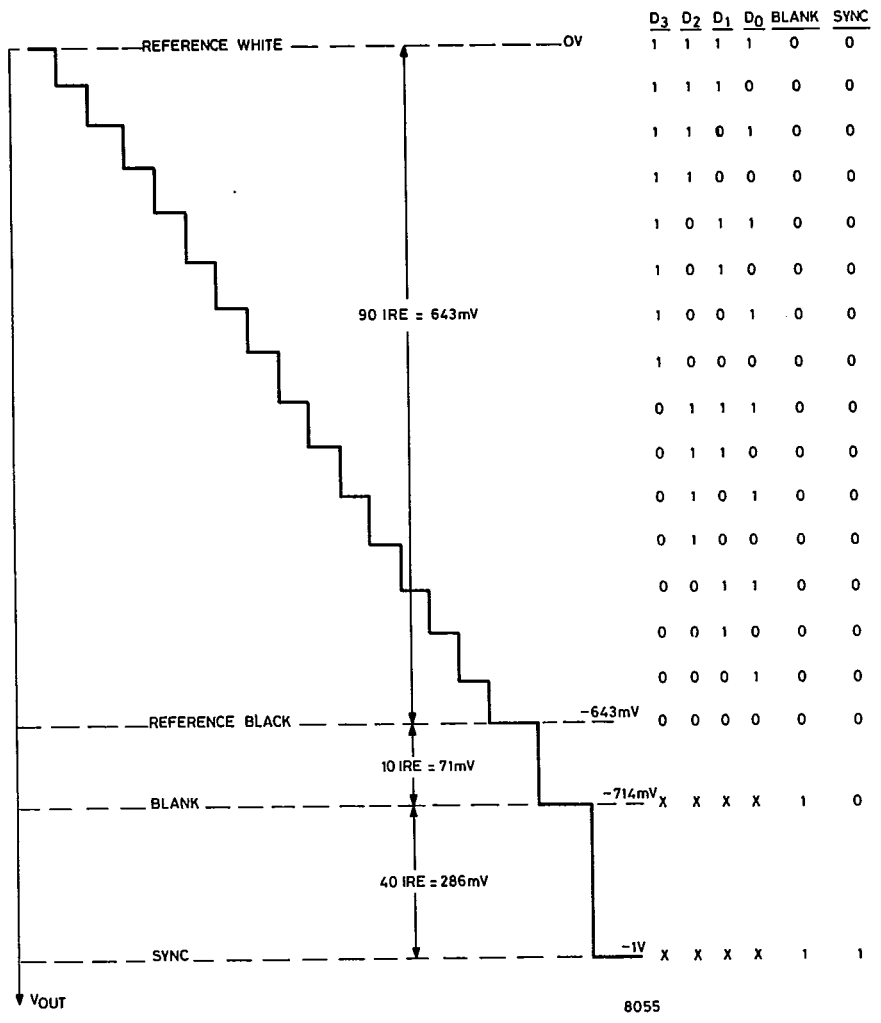

D_3	D_2	D_1	D_0	BLANK	SYNC
1	1	1	1	0	0
1	1	1	0	0	0
1	1	0	1	0	0
1	1	0	0	0	0
1	0	1	1	0	0
1	0	1	0	0	0
1	0	0	1	0	0
1	0	0	0	0	0
0	1	1	1	0	0
0	1	1	0	0	0
0	1	0	1	0	0
0	1	0	0	0	0
0	0	1	1	0	0
0	0	1	0	0	0
0	0	0	1	0	0
0	0	0	0	0	0
X	X	X	X	1	0
X	X	X	X	1	1

Fig. 2 Typical composite video output waveform

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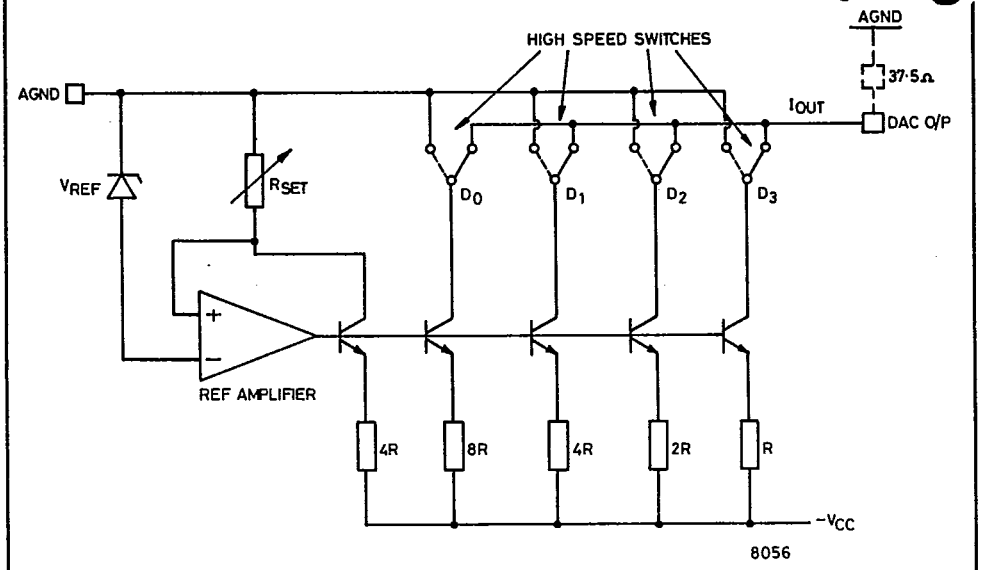

Fig. 3 Current source array (schematic)

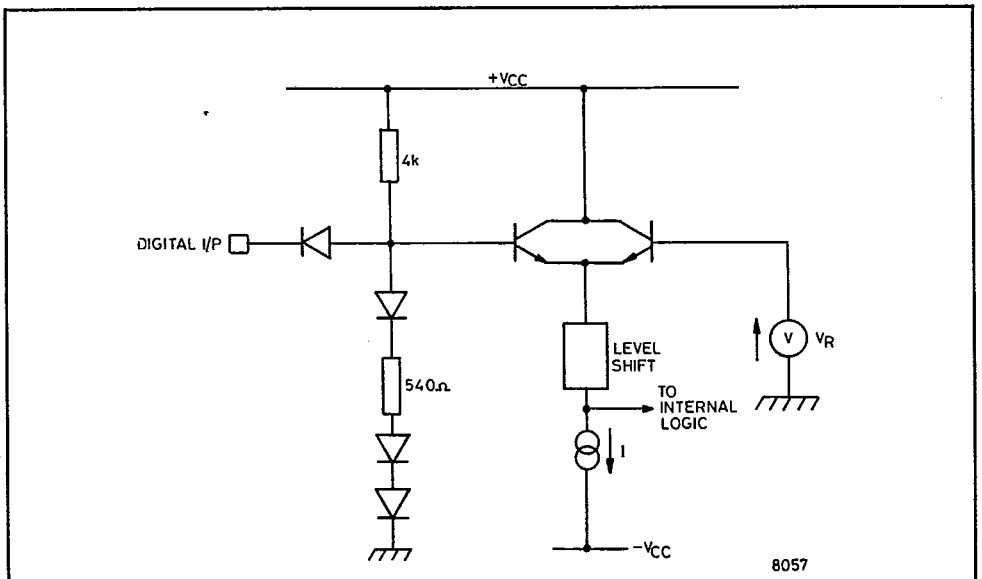

Fig. 4 Equivalent circuit of sync, blank and data inputs

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GENERAL CIRCUIT OPERATION

Each D-A converter of the ZN454CJ uses high speed switches to steer current from precision current sources to either analogue ground or to the analogue output - as governed by the digital inputs (see Fig. 3). The analogue output voltage is now obtained from these weighted current sources producing the desired voltage drop across the 37.5Ω load impedance. The gain of the D-A converters is adjustable via R_{SET}.

Since the ZN454CJ utilises current output DAC's the output impedance is inherently high. Thus a 75Ω resistance is required (adjacent to each DAC output) to shunt this high impedance and provide the correct impedance for driving a 75Ω line terminated in 75Ω at the monitor. The desired 1V p-p composite signal will now be developed across this effective 37.5Ω output impedance.

The grey scale output current of each DAC has 16 levels from 0 → −17mA nominally (see Fig. 2). This develops 16 levels of output voltage from 0 → −643mV across the specified 37.5Ω load impedance. The "REFERENCE WHITE" level (0V) corresponds to the digital input code 1111 and the "REFERENCE BLACK" (−643mV) to 0000.

A logic "1" on the BLANK input overrides the data inputs and drives the output to 71mV more negative than the "REFERENCE BLACK" level. This corresponds to the "BLANKING" (or "blacker-than-black") level.

Activating the SYNC input (logic "1") with the BLANK input "high" drives the output to 286mV more negative than the "BLANKING" level. This voltage (nominally −1V) corresponds to the "SYNC" level.

GAIN ADJUSTMENT (R_{SET})

R_{SET} provides a means of adjusting the current in the weighted current sources. An amplifier compares the voltage developed across R_{SET}, with the reference voltage. If R_{SET} is increased/decreased the amplifier output causes the current through R_{SET} to decrease/increase (to bring the voltage across R_{SET} back in line with the reference voltage). This also causes the current in each of the current sources to decrease/increase (see Fig. 3). In this manner the magnitude of the output waveform can be varied to obtain the desired levels.

DIGITAL INPUTS

The digital inputs are high speed level translators (see Fig. 4).

The ZN454CJ requires very few external components for normal operation. Fig. 5 illustrates the external component connections.

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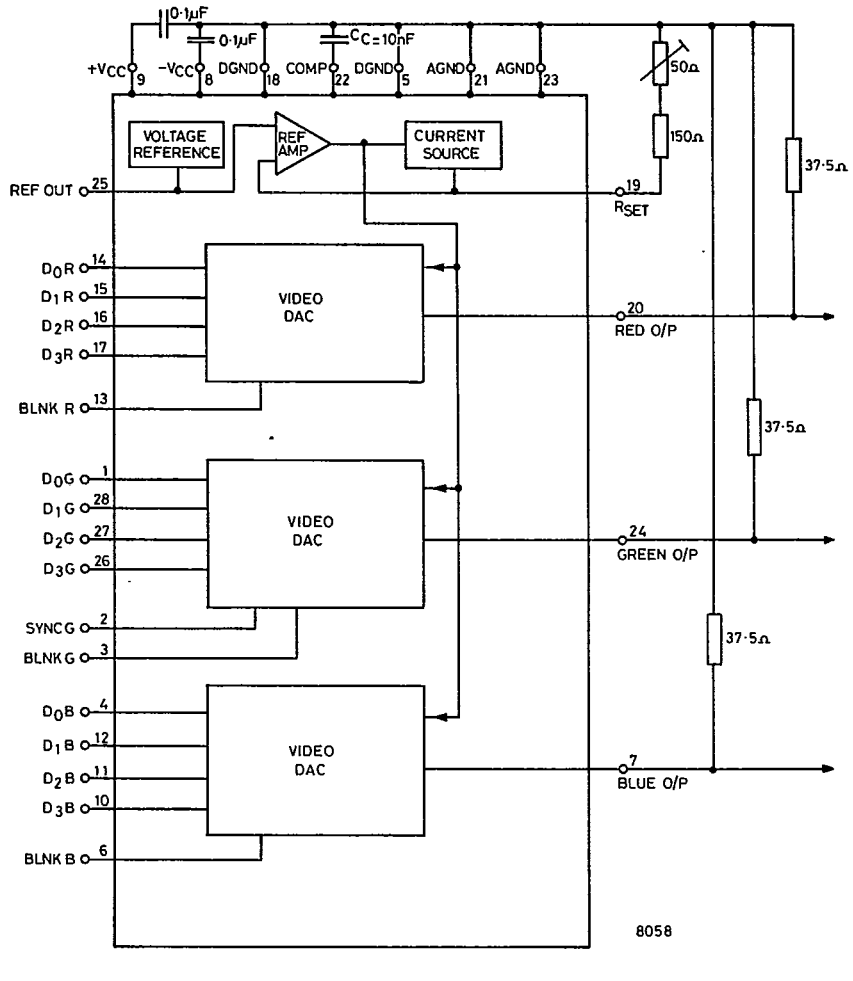

Fig. 5 System diagram showing external component connections

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LAYOUT CONSIDERATIONS

When using the ZN454CJ, as with any other device of this kind, certain precautions must be taken to obtain the best performance.

Some of the requirements are:

- A ground plane board providing a good earth and with good power supply connections, to keep noise to a minimum.
- Good decoupling - especially around all the fast switching circuits - including a 0.1μF capacitor from both the +5 and −5V supplies positioned close to the ZN454CJ. The ground connections for these capacitors should be adjacent.
- Some physical separation between the digital input tracks to minimise crosstalk.
- Matched digital input signal paths to avoid introducing any unnecessary time skew between the inputs. This would cause glitches on the DAC outputs with changing codes. Also the outputs from the driving device will have to be well matched for the same reason.
- 75Ω resistors close to the DAC outputs, to provide the correct impedance for driving 75Ω lines.

SETTLING TIME AND GLITCH ENERGY MEASUREMENT

In a finished design the ZN454CJ would be soldered directly into the board to obtain the best performance possible. However for evaluation purposes a socket really needs to be used. This will give some degradation in performance but useful results can still be obtained.

Measurement of settling time and glitch energy is not a straightforward task and all of the recommendations previously noted must be adhered to. If these parameters are to be measured using an oscilloscope, great care must be taken to avoid corrupting the analogue outputs e.g. conventional probes cannot simply be clipped onto the outputs as this would cause reflections giving rise to errors. Instead the ZN454CJ needs a 75Ωtermination near the chip, a 75Ω cable - also grounded close to the chip - connecting to a 75Ω lead through termination at the oscilloscope. Optimum cable length is about 6" but it may need trimming around this. Also the oscilloscope obviously needs to have sufficient bandwidth to cope with the rise and fall times encountered.

The digital circuits driving the DAC's must not introduce too much noise, or time skew between the bit inputs. This can considerably affect the results. However, a convenient way of minimising these problems for evaluation purposes, is to drive the digital inputs directly from a pulse generator. Full-scale transitions of the grey scale can now be monitored by wiring the I/P's to a given DAC in parallel (terminating in 50Ω) and clocking with the pulse generator. Each output can now be examined in turn. The circuit diagram is as in Fig. 5 except that the sync and blank inputs will be tied low. The 37.5Ω terminations on the DAC output, and the digital input signals are provided as described above. Fig. 6 shows an actual full-scale (grey scale) output transition measured using the above procedure, giving a settling time of 5.12ns.

Glitch energy measurements, at the major transition for example, can also be measured by driving the digital inputs directly from a pulse generator but it will need to have well matched complementary outputs. Also the lead lengths from the generator to the digital inputs will have to be well matched (and terminated in 50Ω). This is so because this measurement is especially critical of any time skew between the input signals. Indeed even an ideal DAC would produce glitches if there were timing differences between these changing input signals. These time skew errors which would manifest themselves as exaggerated glitches on the DAC output, are referred to the point at which the input signals cross the digital input thresholds ($\triangleq$1.5V nom.). Thus the characteristics of the driving signals will have some effect on the amplitude of the glitches, which may be minimised by careful design. The circuit arrangement for measuring the glitch energy is as above but with the digital inputs being switched through different codes. Fig. 7 shows an actual mid-scale glitch, measured using the above procedure.

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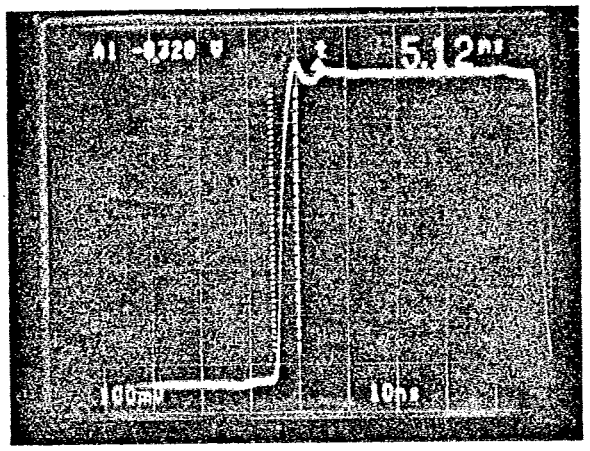

Fig. 6 Full-Scale Output Transition - Settling Time

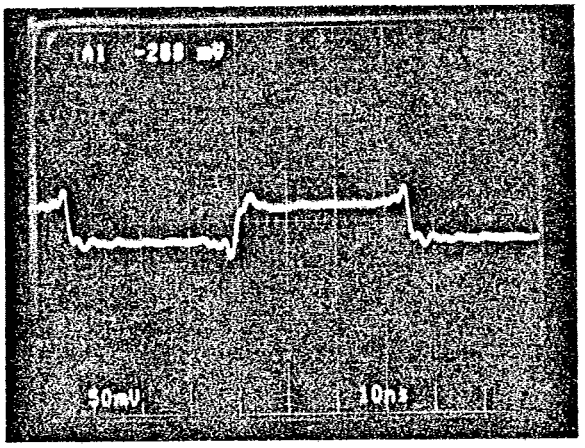

Fig. 7 Mid-Scale Output Glitch

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GLOSSARY OF VIDEO TERMS

Raster scan
The method of sweeping a CRT one line at a time to generate and display images.

Composite video signal
The VIDEO signal plus the BLANK and SYNC signals.

Video signal
The portion of the composite VIDEO SIGNAL which varies in grey scale levels between "reference white" and "reference black" - this is the portion which is visually observed.

Sync signal
The portion of the video waveform that synchronises the raster scanning process.

Grey scale
The discrete levels between and including "reference white" and "reference black" - there are 16 levels for a 4-bit DAC.

Blanking level
The level separating the SYNC portion from the VIDEO portion. Usually referred to as the FRONT PORCH or BACK PORCH, this is the level which will shut off the electron guns resulting in the blackest possible display.

Sync level
The negative peak level of the sync signal.

Reference black level
The maximum negative level of the VIDEO signal.

Reference white level
The maximum positive level of the VIDEO signal.

PIN CONNECTIONS