Dual, Precision JFET High-Speed Operational Amplifier

OP249

FEATURES

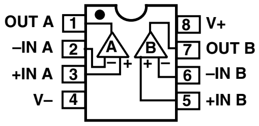
- **Fast Slew Rate: 22 V/µs Typ**
- **Settling Time (0.01%): 1.2 µs Max**
- **Offset Voltage: 300 µV Max**
- **High Open-Loop Gain: 1000 V/mV Min**
- **Low Total Harmonic Distortion: 0.002% Typ**
- **Improved Replacement for AD712, LT1057, OP215, TL072, and MC34082**

APPLICATIONS

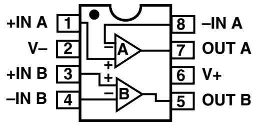
- **Output Amplifier for Fast D/As**
- **Signal Processing**
- **Instrumentation Amplifiers**
- **Fast Sample/Holds**
- **Active Filters**
- **Low Distortion Audio Amplifiers**
- **Input Buffer for A/D Converters**
- **Servo Controllers**

PIN CONNECTIONS

8-Lead Cerdip (Z Suffix), 8-Lead Plastic Mini-DIP (P Suffix)



8-Lead SO (S Suffix)



GENERAL DESCRIPTION

The OP249 is a high speed, precision dual JFET op amp, similar to the popular single op amp, the OP42. The OP249 outperforms available dual amplifiers by providing superior speed with excellent dc performance. Ultrahigh open-loop gain (1 kV/mV minimum), low offset voltage, and superb gain linearity makes the OP249 the industry's first true precision, dual high speed amplifier.

With a slew rate of 22 V/µs typical and a fast settling time of less than 1.2 µs maximum to 0.01%, the OP249 is an ideal choice for high speed bipolar D/A and A/D converter applications. The excellent dc performance of the OP249 allows the full accuracy of high resolution CMOS D/As to be realized.

Symmetrical slew rate, even when driving large load, such as, 600 Ω or 200 pF of capacitance and ultralow distortion, make the OP249 ideal for professional audio applications, active filters, high speed integrators, servo systems, and buffer amplifiers.

The OP249 provides significant performance upgrades to the TL072, AD712, OP215, MC34082, and the LT1057.

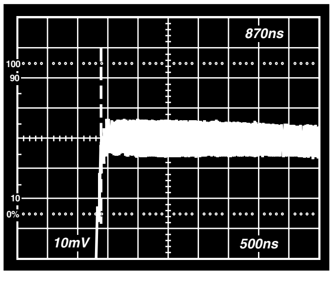


Figure 1. Fast Settling (0.01%)

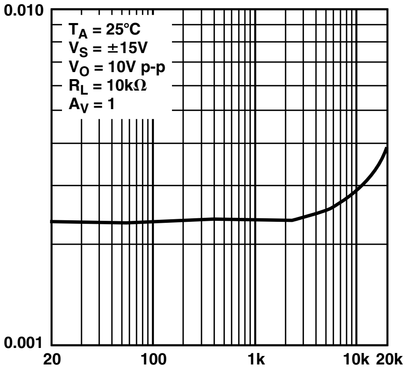


Figure 2. Low Distortion $A_V = 1$, $R_L = 10\ k\Omega$

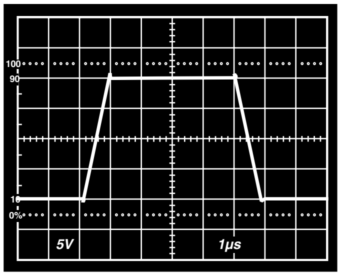


Figure 3. Excellent Output Drive, $R_L = 600\ \Omega$

REV. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

OP249–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

				OP249A			OP249F		
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Offset Voltage	V_{OS}			0.2	0.5		0.2	0.7	mV
Long Term Offset Voltage	V_{OS}	(Note 1)			0.8			1.0	mV
Offset Stability				1.5			1.5		μV/Month
Input Bias Current	I_B	V_{CM} = 0 V, T_J = 25°C		30	75		30	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V, T_J = 25°C		6	25		6	25	pA
Input Voltage Range	IVR	(Note 2)		12.5			12.5		V
			±11			±11			V
				–12.5			–12.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	80	90		80	90		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		12	31.6		12	50	μV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 2 kΩ	1000	1400		500	1200		V/mV
Output Voltage Swing	V_O	R_L = 2 kΩ		12.5			12.5		V
			±12.0			±12.0			V
				–12.5			–12.5		V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground		36			36		mA
			±20		±50	±20		±50	mA
				–33			–33		mA
Supply Current	I_{SY}	No Load, V_O = 0 V		5.6	7.0		5.6	7.0	mA
Slew Rate	SR	R_L = 2 kΩ, C_L = 50 pF	18	22		18	22		V/μs
Gain-Bandwidth Product	GBW	(Note 3)	3.5	4.7		3.5	4.7		MHz
Settling Time	t_S	10 V Step 0.01%[4]		0.9	1.2		0.9	1.2	μs
Phase Margin	θ_0	0 dB Gain		55			55		Degrees
Differential Input Impedance	Z_{IN}			$10^{12}\|6$			$10^{12}\|6$		Ω‖pF
Open-Loop Output Resistance	R_O			35			35		Ω
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2			2		μV p-p
Voltage Noise Density	e_n	f_O = 10 Hz		75			75		nV/√Hz
		f_O = 100 Hz		26			26		nV/√Hz
		f_O = 1 kHz		17			17		nV/√Hz
		f_O = 10 kHz		16			16		nV/√Hz
Current Noise Density	i_n	f_O = 1 kHz		0.003			0.003		pA/√Hz
Voltage Supply Range	V_S		±4.5	±15	±18	±4.5	±15	±18	V

NOTES

[1] Long-term offset voltage is guaranteed by a 1000 HR life test performed on three independent wafer lots at 125°C with LTPD of three.

[2] Guaranteed by CMR test.

[3] Guaranteed by design.

[4] Settling time is sample tested.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

				OP249G		
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Offset Voltage	V_{OS}			0.4	2.0	mV
Input Bias Current	I_B	V_{CM} = 0 V, T_J = 25°C		40	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V, T_J = 25°C		10	25	pA
Input Voltage Range	IVR	(Note 1)		12.5		V
			±11			V
				–12.0		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	76	90		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		12	50	μV/V
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V; R_L = 2 kΩ	500	1100		V/mV
Output Voltage Swing	V_O	R_L = 2 kΩ		12.5		V
			±12.0			V
				–12.5		V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground		36		mA
			±20		±50	mA
				–33		mA
Supply Current	I_{SY}	No Load; V_O = 0 V		5.6	7.0	mA
Slew Rate	SR	R_L = 2 kΩ, C_L = 50 pF	18	22		V/μs
Gain Bandwidth Product	GBW	(Note 2)		4.7		MHz
Settling Time	t_S	10 V Step 0.01%		0.9	1.2	μs
Phase Margin	θ_0	0 dB Gain		55		Degree
Differential Input Impedance	Z_{IN}			$10^{12}\|6$		Ω‖pF

Parameter	Symbol	Conditions	OP249G Min	 Typ	 Max	Unit
Open Loop Output Resistance	R_O			35		Ω
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		μV p-p
Voltage Noise Density	e_n	f_O = 10 Hz		75		nV/√Hz
		f_O = 100 Hz		26		nV/√Hz
		f_O = 1 kHz		17		nV/√Hz
		f_O = 10 kHz		16		nV/√Hz
Current Noise Density	i_n	f_O = 1 kHz		0.003		pA/√Hz
Voltage Supply Range	V_S		±4.5	±15	±18	V

NOTES

[1] Guaranteed by CMR test.

[2] Guaranteed by design.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, –40°C ≤ T_A ≤ +85°C for F grades and –55°C ≤ T_A ≤ +125°C for A grade unless otherwise noted.)

Parameter	Symbol	Conditions	OP249A Min	 Typ	 Max	OP249F Min	 Typ	 Max	Unit
Offset Voltage	V_{OS}			0.12	1.0		0.5	1.1	mV
Offset Voltage Temperature Coefficient	TCV_{OS}			1	5		2.2	6	μV/°C
Input Bias Current	I_B	(Note 1)		4	20		0.3	4.0	nA
Input Offset Current	I_{OS}	(Note 1)		0.04	4		0.02	1.2	nA
Input Voltage Range	IVR	(Note 2)		12.5			12.5		V
			±11			±11			V
				–12.5			–12.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	76	110		80	90		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		5	50		7	100	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ; V_O = ±10 V	500	1400		250	1200		V/mV
Output Voltage Swing	V_O	R_L = 2 kΩ		12.5			12.5		V
			±12			±12			V
				–12.5			–12.5		V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±10		±60	±18		±60	mA
Supply Current	I_{SY}	No Load, V_O = 0 V		5.6	7.0		5.6	7.0	mA

NOTES

[1] T_J = 85°C for F Grades; T_J = 125°C for A Grade.

[2] Guaranteed by CMR test.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, –40°C ≤ T_A ≤ +85°C for unless otherwise noted.)

Parameter	Symbol	Conditions	OP249G Min	 Typ	 Max	Unit
Offset Voltage	V_{OS}			1.0	3.6	mV
Offset Voltage Temperature Coefficient	TCV_{OS}			6	25	μV/°C
Input Bias Current	I_B	(Note 1)		0.5	4.5	nA
Input Offset Current	I_{OS}	(Note 1)		0.04	1.5	nA
Input Voltage Range	IVR	(Note 2)		12.5		V
			±11			V
				–12.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	76	95		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		10	100	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ; V_O = ±10 V	250	1200		V/mV
Output Voltage Swing	V_O	R_L = 2 kΩ		12.5		V
			±12.0			V
				–12.5		V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±18		±60	mA
Supply Current	I_{SY}	No Load, V_O = 0 V		5.6	7.0	mA

NOTES

[1] T_J = 85°C.

[2] Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Input Voltage[2]	±18 V
Differential Input Voltage[2]	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	–65°C to +175°C
Operating Temperature Range	
OP249A (Z)	–55°C to +125°C
OP249E, F (Z)	–40°C to +85°C
OP249G (P, S)	–40°C to +85°C
Junction Temperature	
OP249 (Z)	–65°C to +175°C
OP249 (P, S)	–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
8-Lead Hermetic DIP (Z)	134	12	°C/W
8-Lead Plastic DIP (P)	96	37	°C/W
8-Lead SO (S)	150	41	°C/W

NOTES

[1] Absolute maximum ratings apply to packaged parts, unless otherwise noted.

[2] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

[3] θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE*

Model	Temperature Range	Package Descriptions	Package Options
OP249AZ	–55°C to +125°C	8-Lead Cerdip	Q-8
OP249FZ	–40°C to +85°C	8-Lead Cerdip	Q-8
OP249GP	–40°C to +85°C	8-Lead Plastic DIP	N-8
OP249GS*	–40°C to +85°C	8-Lead SO	SO-8
OP249GS-REEL	–40°C to +85°C	8-Lead SO	SO-8
OP249GS-REEL7	–40°C to +85°C	8-Lead SO	SO-8

NOTES

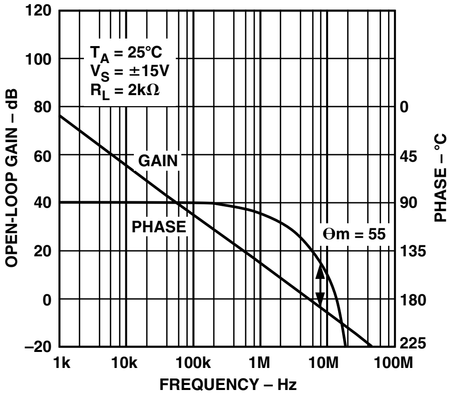
*For availability and burn-in information on SO and PLCC packages, contact your local sales office.

For Military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

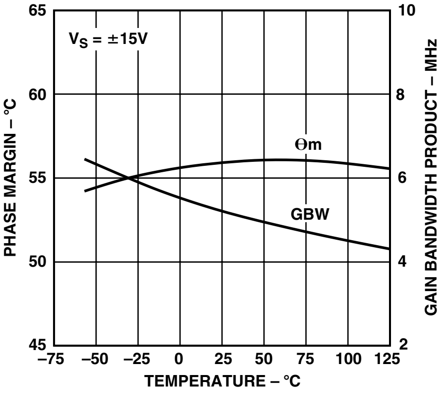
SMD Part Number	ADI Equivalent
5962-9151901M2A	OP249ARCMDA
5962-9151901MGA	OP249AJMDA
5962-9151901MPA	OP249AZMDA

CAUTION

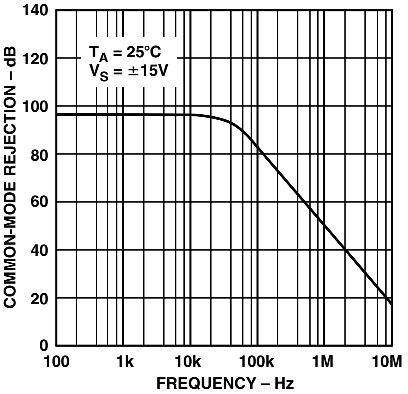
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP249 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



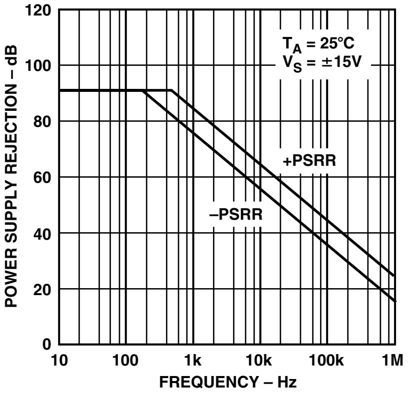
TPC 1. Open-Loop Gain, Phase vs. Frequency



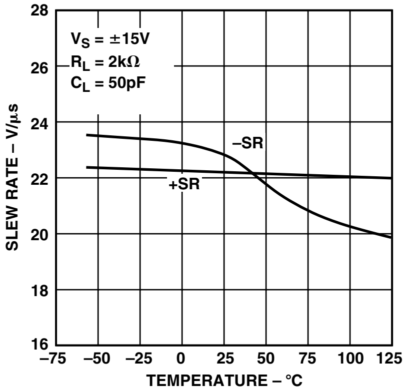
TPC 2. Gain Bandwidth Product, Phase Margin vs. Temperature



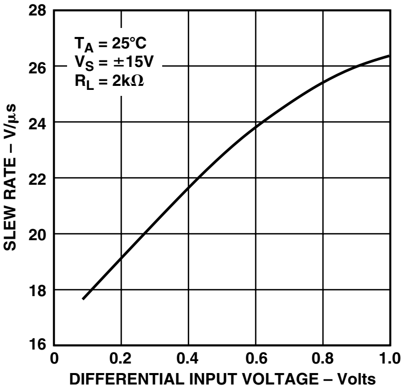
TPC 3. Common-Mode Rejection vs. Frequency



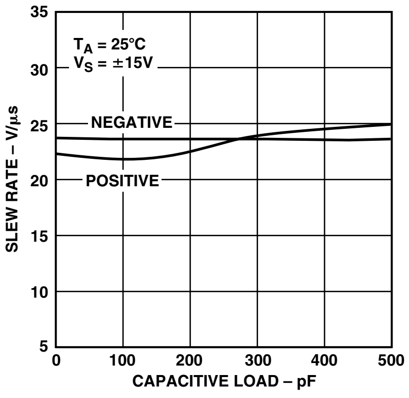
TPC 4. Power Supply Rejection vs. Frequency



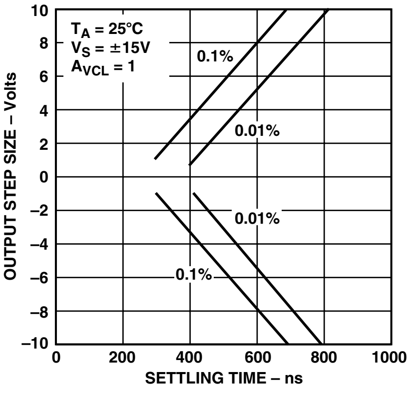
TPC 5. Slew Rate vs. Temperature



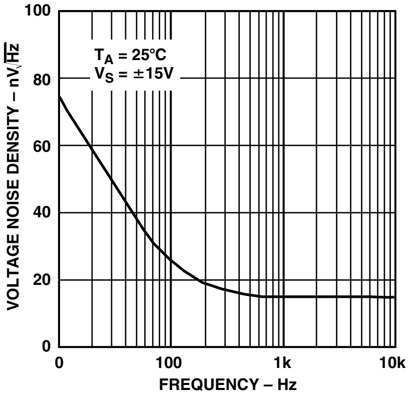
TPC 6. Slew Rate vs. Differential Input Voltage



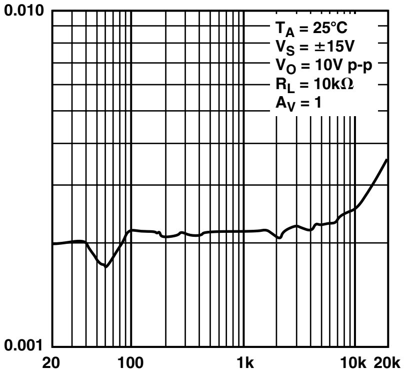
TPC 7. Slew Rate vs. Capacitive Load



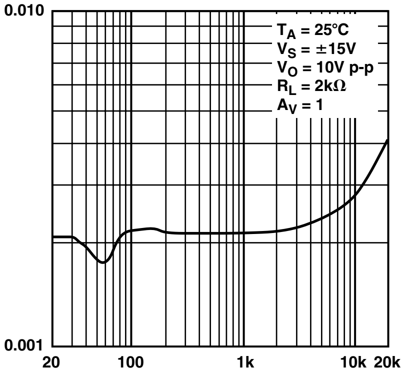
TPC 8. Settling Time vs. Step Size



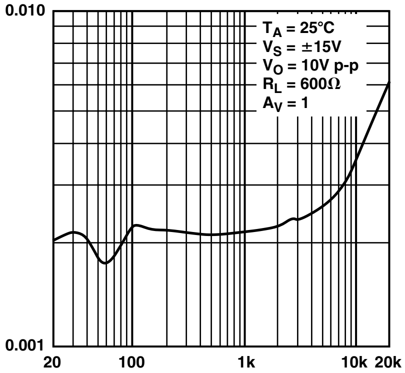
TPC 9. Voltage Noise Density vs. Frequency



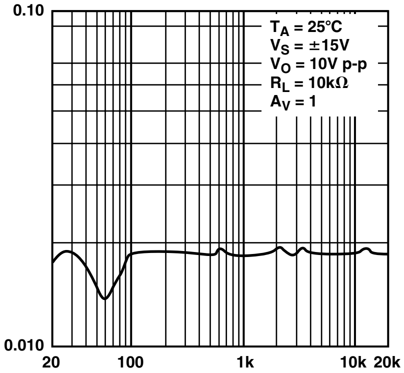
TPC 10. Distortion vs. Frequency



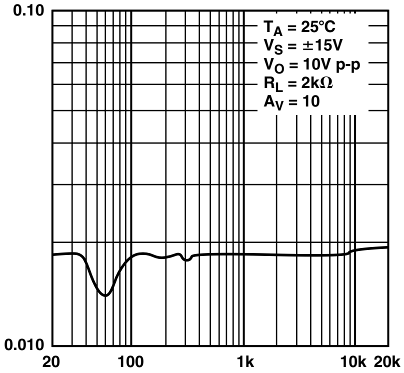
TPC 11. Distortion vs. Frequency



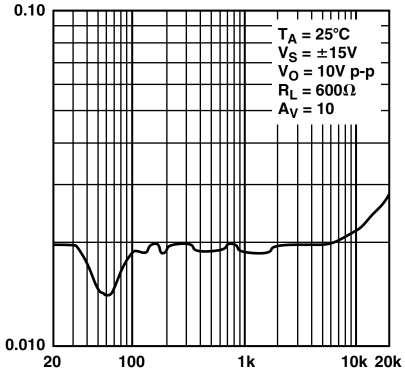
TPC 12. Distortion vs. Frequency



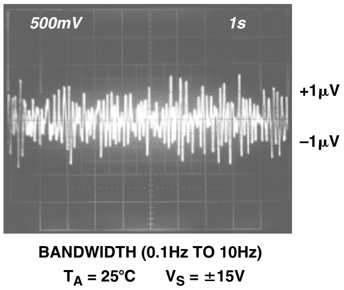
TPC 13. Distortion vs. Frequency



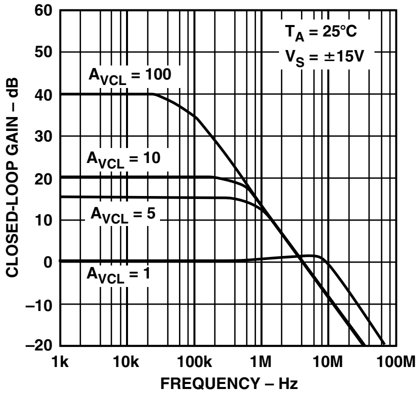
TPC 14. Distortion vs. Frequency



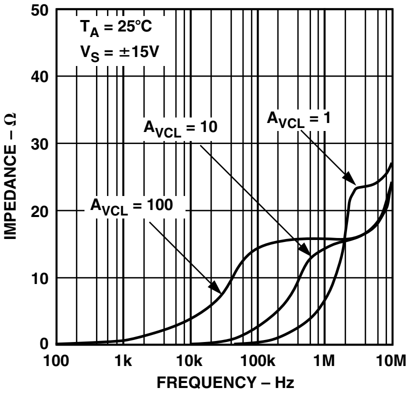
TPC 15. Distortion vs. Frequency



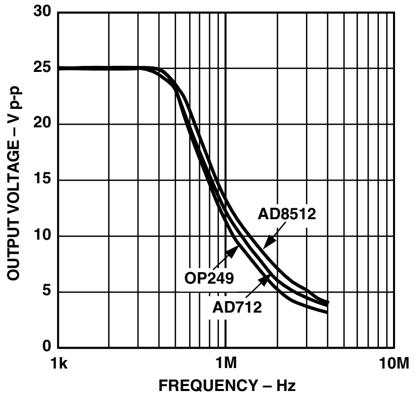
TPC 16. Low Frequency Noise



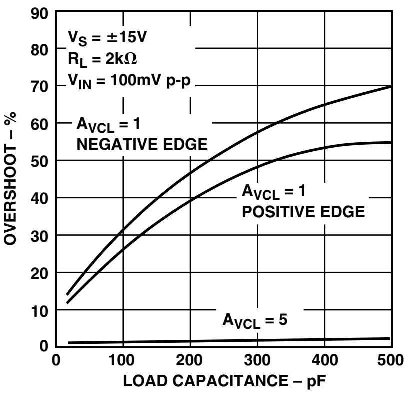
TPC 17. Closed-Loop Gain vs. Frequency



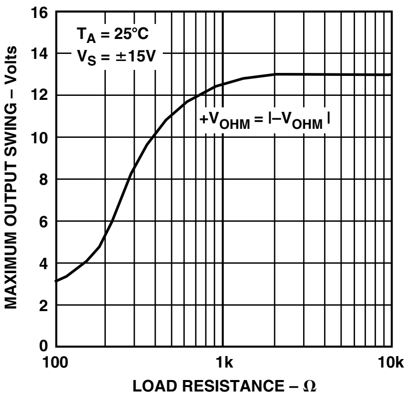
TPC 18. Closed-Loop Output Impedance vs. Frequency



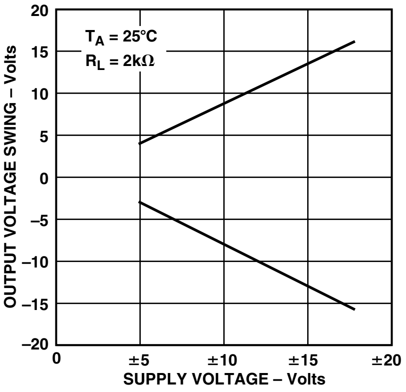
TPC 19. Output Voltage vs. Frequency



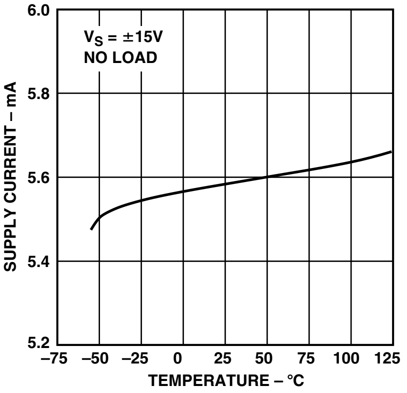
TPC 20. Small Overshoot vs. Load Capacitance



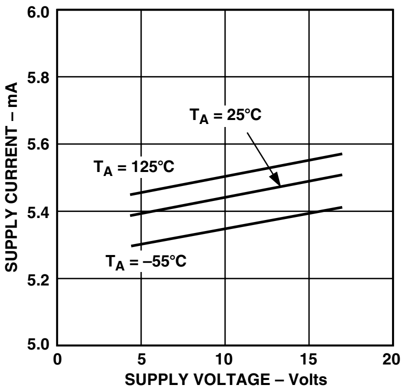
TPC 21. Maximum Output Voltage vs. Load Resistance



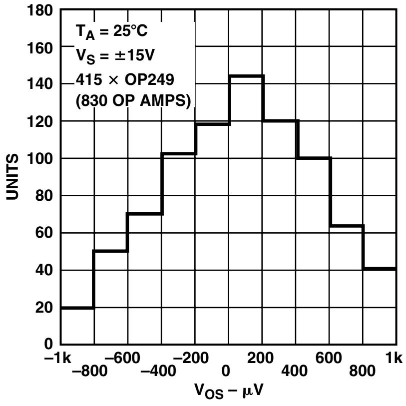
TPC 22. Output Voltage Swing vs. Supply Voltage



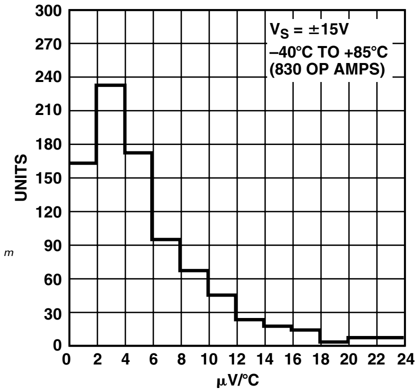
TPC 23. Supply Current vs. Temperature



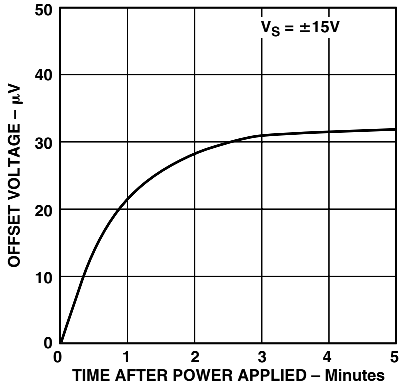
TPC 24. Supply Current vs. Supply Voltage



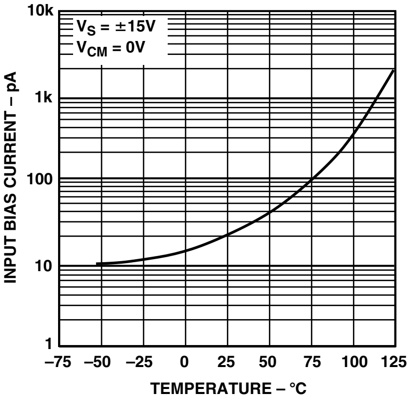
TPC 25. V_{OS} Distribution (P Package)



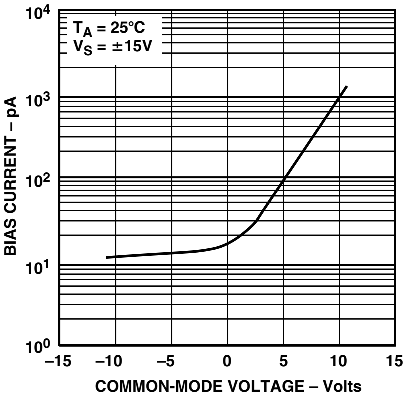
TPC 26. TCV_{OS} Distribution (P Package)



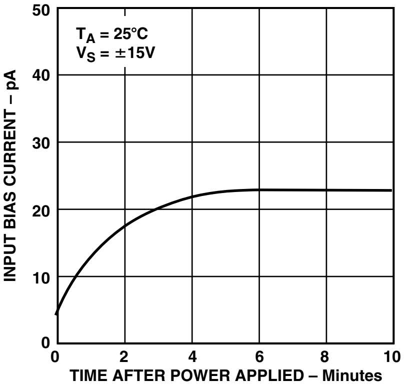
TPC 27. Offset Voltage Warm-Up Drift



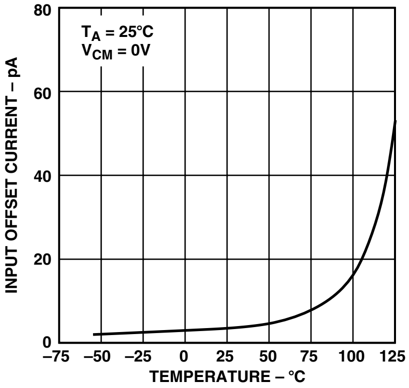
TPC 28. Input Bias Current vs. Temperature



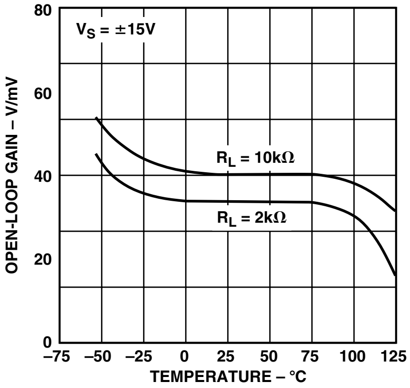
TPC 29. Bias Current vs. Common-Mode Voltage



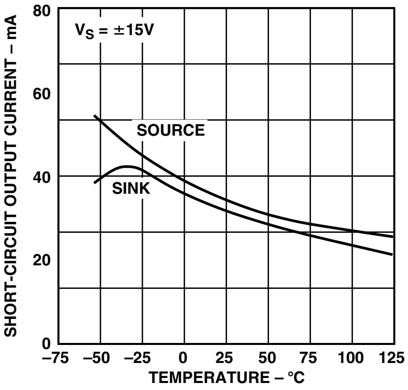
TPC 30. Bias Current Warm-Up Drift



TPC 31. Input Offset Current vs. Temperature



TPC 32. Open-Loop Gain vs. Temperature



TPC 33. Short-Circuit Output Current vs. Junction Temperature

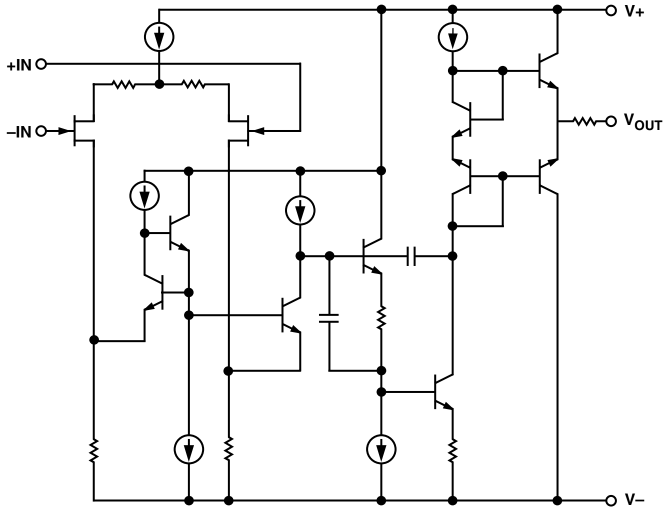


Figure 4. Simplified Schematic (1/2 OP249)

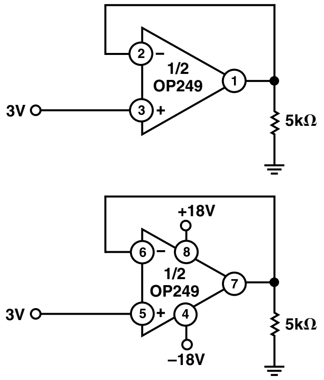
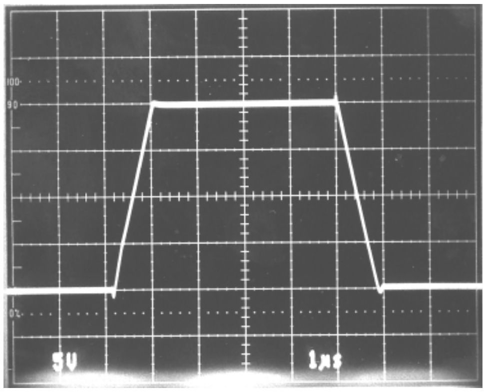


Figure 5. Burn-In Circuit

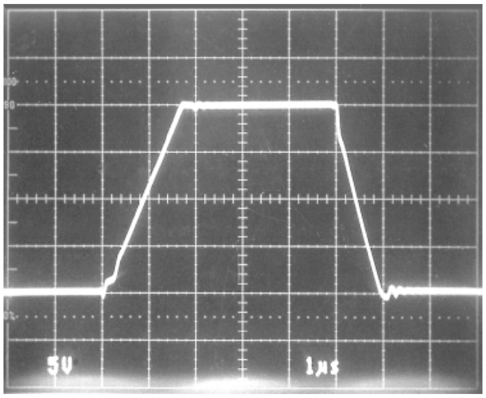
APPLICATIONS INFORMATION

The OP249 represents a reliable JFET amplifier design, featuring an excellent combination of dc precision and high speed. A rugged output stage provides the ability to drive a 600 Ω load and still maintain a clean ac response. The OP249 features a large signal response that is more linear and symmetric than previously available JFET input amplifiers—compare the OP249's large-signal response, as illustrated in Figure 6, to other industry standard dual JFET amplifiers.

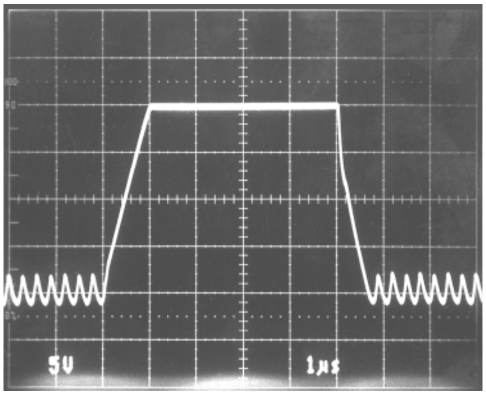
Typically, JFET amplifier's stewing performance is simply specified as just a number of volts/µs. There is no discussion on the quality, i.e., linearity, symmetry, etc., of the stewing response.



A) OP249



B) LT1057



C) AD712

Figure 6. Large-Signal Transient Response, $A_V = 1$, $V_{IN} = 20$ V p-p, $Z_L = 2$ kΩ//200 pF, $V_S = \pm 15$ V

The OP249 was carefully designed to provide symmetrically matched slew characteristics in both the negative and positive directions, even when driving a large output load.

An amplifier's slewing limitation determines the maximum frequency at which a sinusoidal output can be obtained without significant distortion. It is, however, important to note that the nonsymmetric stewing typical of previously available JFET amplifiers adds a higher series of harmonic energy content to the resulting response—and an additional dc output component. Examples of potential problems of nonsymmetric slewing behavior could be in audio amplifier applications, where a natural low distortion sound quality is desired, and in servo or signal processing systems where a net dc offset cannot be tolerated. The linear and symmetric stewing feature of the OP249 makes it an ideal choice for applications that will exceed the full-power bandwidth range of the amplifier.

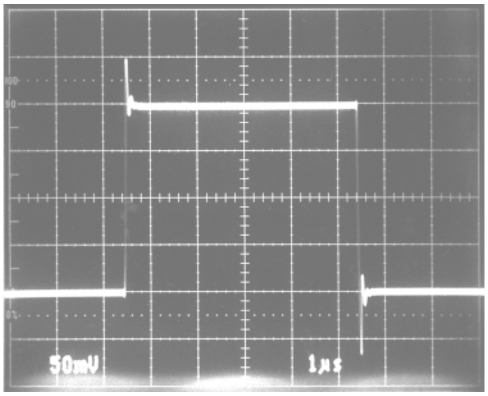


Figure 7. Small-Signal Transient Response, $A_V = 1$, $Z_L = 2\ k\Omega \| 100\ pF$, No Compensation, $V_S = \pm 15\ V$

As with most JFET-input amplifiers, the output of the OP249 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up condition.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier. A 0.1 µF and a 10 µF capacitor should be placed between each supply pin and ground.

OPEN-LOOP GAIN LINEARITY

The OP249 has both an extremely high open-loop gain of 1 kV/mV minimum and constant gain linearity. This feature of the OP249 enhances its dc precision, and provides superb accuracy in high closed-loop gain applications. Figure 8 illustrates the typical open-loop gain linearity—high gain accuracy is assured, even when driving a 600 Ω load.

OFFSET VOLTAGE ADJUSTMENT

The inherent low offset voltage of the OP249 will make offset adjustments unnecessary in most applications. However, where a lower offset error is required, balancing can be performed with simple external circuitry, as illustrated in Figures 9 and 10.

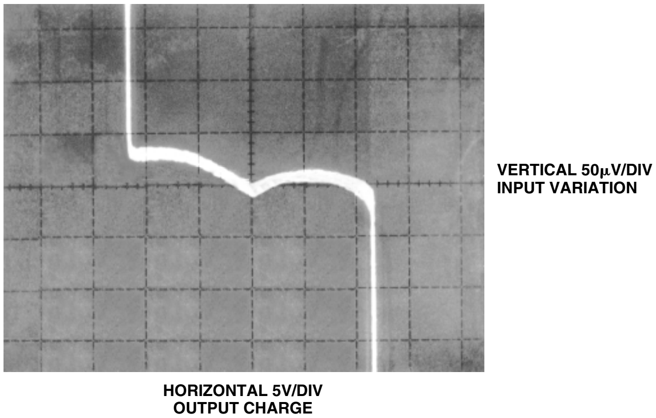


Figure 8. Open-Loop Gain Linearity. Variation in Open-Loop Gain Results in Errors in High Closed-Loop Gain Circuits. $R_L = 600\ \Omega$, $V_S = \pm 15\ V$

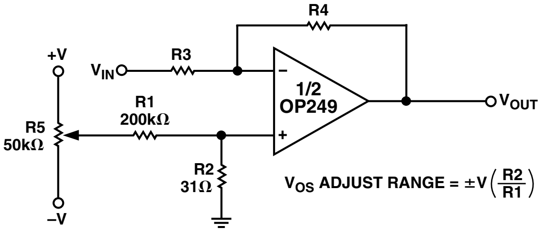


Figure 9. Offset Adjust for Inverting Amplifier Configuration

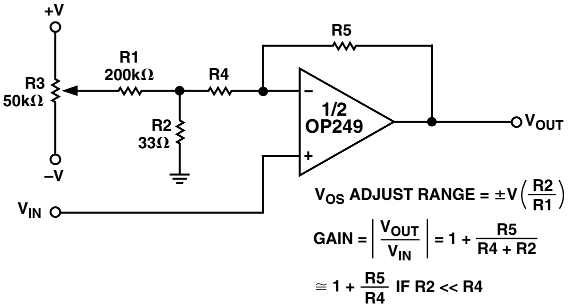


Figure 10. Offset Adjust for Noninverting Amplifier Configuration

In Figure 9, the offset adjustment is made by supplying a small voltage at the noninverting input of the amplifier. Resistors R1 and R2 attenuates the pot voltage, providing a ±2.5 mV (with $V_S = \pm 15$ V) adjustment range, referred to the input. Figure 10 illustrates offset adjust for the noninverting amplifier configuration, also providing a ±2.5 mV adjustment range. As indicated in the equations in Figure 10, if R4 is not much greater than R2, there will be a resulting closed-loop gain error that must be accounted for.

SETTLING TIME

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. The error bands on the output are 5 mV and 0.5 mV, respectively, for 0.1% and 0.01% accuracy.

Figure 11 illustrates the OP249's typical settling time of 870 ns. Moreover, problems in settling response, such as thermal tails and long-term ringing are nonexistent.

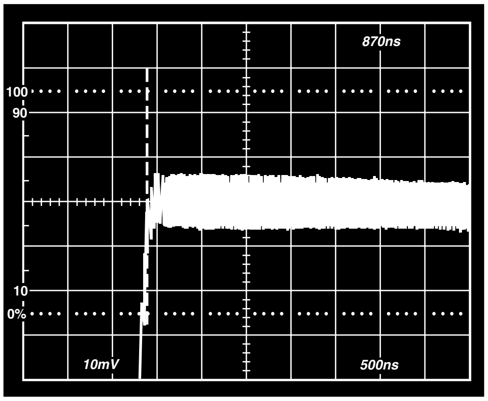


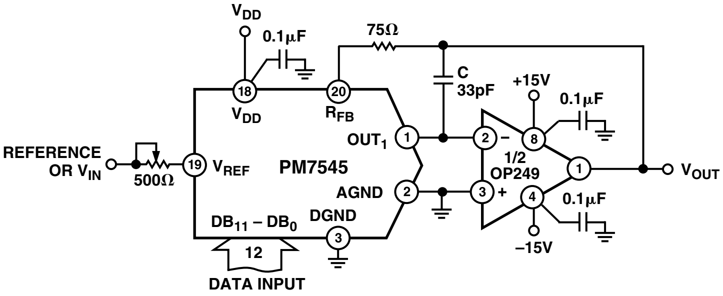
Figure 11. Settling Characteristics of the OP249 to 0.01%

DAC OUTPUT AMPLIFIER

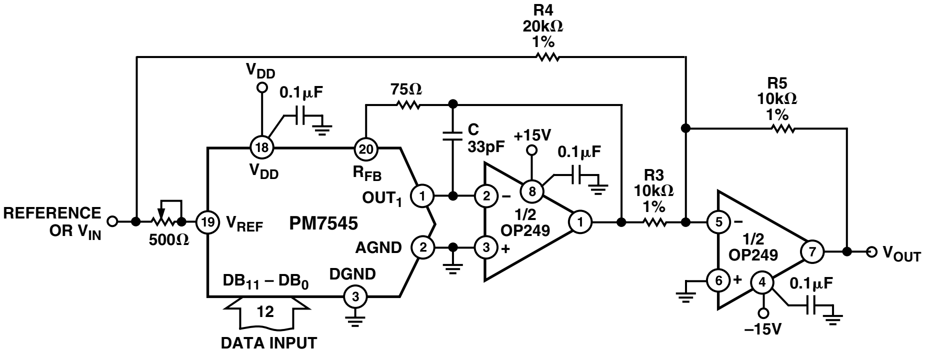
Unity-gain stability, a low offset voltage of 300 µV typical, and a fast settling time of 870 ns to 0.01%, makes the OP249 an ideal amplifier for fast digital-to-analog converters.

For CMOS DAC applications, the low offset voltage of the OP249 results in excellent linearity performance. CMOS DACs, such as the PM-7545, will typically have a code-dependent output resistance variation between 11 kΩ and 33 kΩ. The change in output resistance, in conjunction with the 11 kΩ feedback resistor, will result in a noise gain change. This causes variations in the offset error, increasing linearity errors. The OP249 features low offset voltage error, minimizing this effect and maintaining 12-bit linearity performance over the full-scale range of the converter.

Since the DAC's output capacitance appears at the operational amplifiers inputs, it is essential that the amplifier is adequately compensated. Compensation will increase the phase margin, and ensure an optimal overall settling response. The required lead compensation is achieved with Capacitor C in Figure 12.

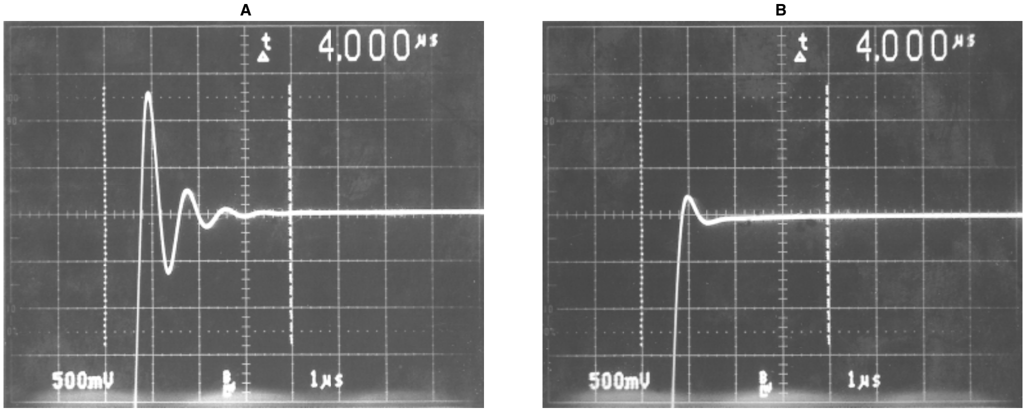


a. Unipolar Operation



b. Bipolar Operation

Figure 12. Fast Settling and Low Offset Error of the OP249 Enhances CMOS DAC Performance



C = 5pF
RESPONSE IS GROSSLY UNDERDAMPED,
AND EXHIBITS RINGING

C = 15pF
FAST RISE TIME CHARACTERISTICS, BUT AT EXPENSE
OF SLIGHT PEAKING IN RESPONSE

Figure 13. Effect of Altering Compensation from Circuit in Figure 12a—PM7545 CMOS DAC with 1/2 OP249, Unipolar Operation. Critically Damped Response Will Be Obtained with C ≈ 33 pF.

Figure 13 illustrates the effect of altering the compensation on the output response of the circuit in Figure 12a. Compensation is required to address the combined effect of the DAC's output capacitance, the op amp's input capacitance and any stray capacitance. Slight adjustments to the compensation capacitor may be required to optimize settling response for any given application.

The settling time of the combination of the current output DAC and the op amp can be approximated by:

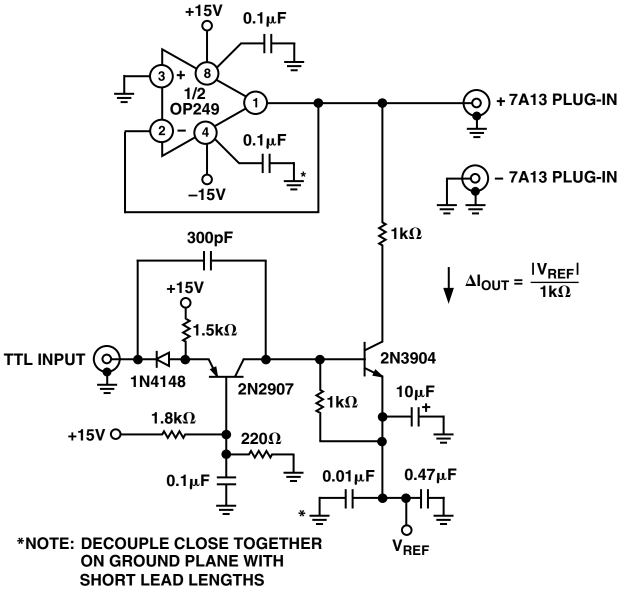
$$t_S\ TOTAL = \sqrt{(t_S\ DAC)^2 + (t_S\ AMP)^2}$$

The actual overall settling time is affected by the noise gain of the amplifier, the applied compensation, and the equivalent input capacitance at the amplifier's input.

DISCUSSION ON DRIVING A/D CONVERTERS

Settling characteristics of operational amplifiers also include an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 14 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1 mA. As seen in Figure 15, the OP249 has extremely fast recovery of 274 ns (to 0.01%), for a 1 mA load transient. The performance makes it an ideal amplifier for data acquisition systems.



*NOTE: DECOUPLE CLOSE TOGETHER
ON GROUND PLANE WITH
SHORT LEAD LENGTHS

Figure 14. Transient Output Impedance Test Fixture

The combination of high speed and excellent dc performance of the OP249 makes it an ideal amplifier for 12-bit data acquisition systems. Examining the circuit in Figure 16, one amplifier in the OP249 provides a stable –5 V reference voltage for the V_{REF} input of the ADC912. The other amplifier in the OP249 performs high speed buffering of the A/D's input.

Examining the worst case transient voltage error (Figure 17) at the Analog In node of the A/D converter: the OP249 recovers in less than 100 ns. The fast recovery is due to both the OP249's wide bandwidth and low dc output impedance.

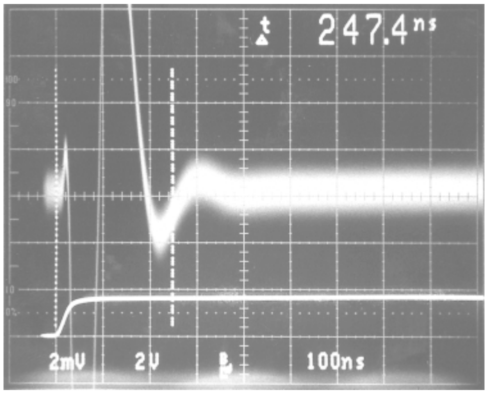


Figure 15. OP249's Transient Recovery Time from a 1 mA Load Transient to 0.01%

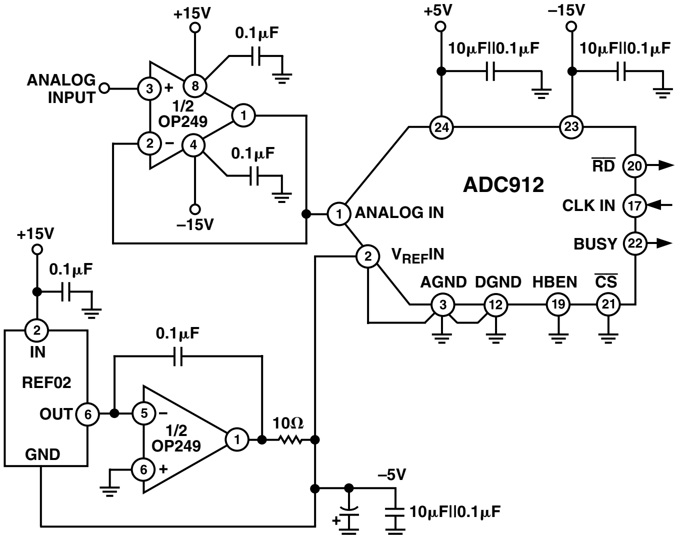


Figure 16. OP249 Dual Amplifiers Provide Both Stable –5 V Reference Input, and Buffers Input to ADC912

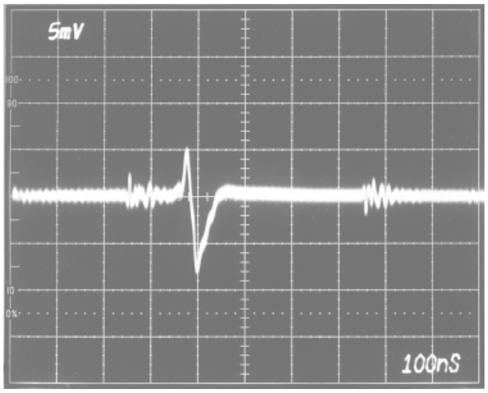


Figure 17. Worst-Case Transient Voltage, at Analog In, Occurs at the Half-Scale Point of the A/D. OP249 Buffers the A/D Input from Figure 16, and Recovers in Less than 100 ns.

OP249 SPICE MACRO-MODEL

Figures 18 and Table I show the node and net list for a SPICE macromodel of the OP249 The model is a simplified version of the actual device and simulates important dc parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase response and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP249. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response of the OP249. In this way, the model presents an accurate ac representation of the actual device. The model assumes an ambient temperature of 25°C.

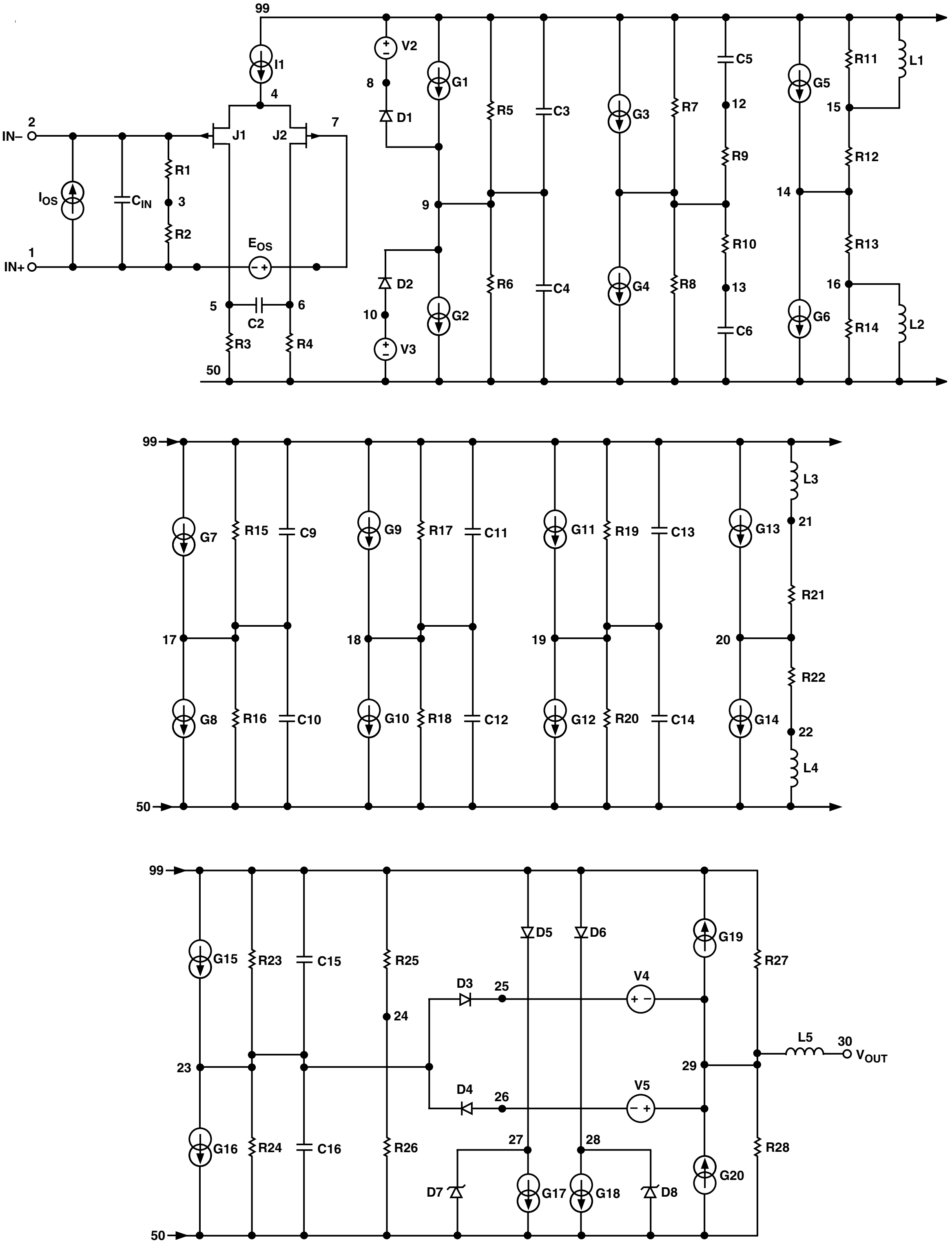


Figure 18. Macro-Model

Table I. SPICE Net List

OP249 MACRO-MODEL

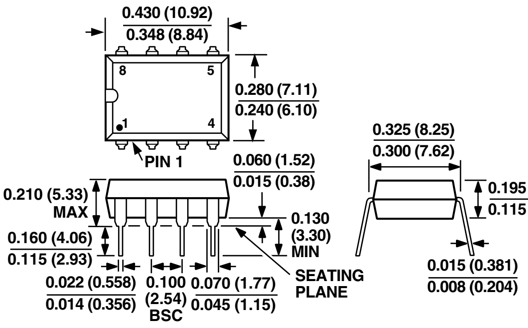
```
• subckt OP249 1 2 30 99 50
*
INPUT STAGE & POLE AT 100MHz
*
r1   2    3        5E11
r2   1    3        5E11
r3   5    50       652.3
r4   6    50       652.3
cin  1    2        5E-12
c2   5    6        1.22E-12
i1   99   4        1E-3
ios  1    2        3.1E-12
eos  7    1        poly(1) 20 24 150E-6 1
j1   5    2    4   jx
j2   6    7    4   jx
*
* SECOND STAGE & POLE AT 12.2Hz
*
r5   9    99       326.1E6
r6   9    50       326.1E6
c3   9    99       40E-12
c4   9    50       40E-12
g1   99   9        poly(1) 5 6 4.25E-3 1.533E-3
g2   9    50       poly(1) 6 5 4.25E-3 1.533E-3
v2   99   8        2.9
v3   10   50       2.9
d1   9    8        dx
d2   10   9        dx
*
* POLE-ZERO PAIR AT 2MHz/4.0MHz
*
r7   11   99       1E6
r8   11   50       1E6
r9   11   12       1E6
r10  11   13       1E6
c5   12   99       37.79E-15
c6   13   50       37.79E-15
g3   99   11       9  24 1E-6
g4   11   50       24 9  1E-6
*
* ZERO-POLE PAIR AT 4MHz/8MHz
*
r11  99   15       IE6
r12  14   15       1E6
r13  14   16       1E6
r14  50   16       1E6
I1   99   15       19.89E-3
I2   50   16       19.89E-3
g5   99   14       11 24 1E-6
g6   14   50       24 11 1E-6
*
* POLE AT 20MHz
*
r15  17   99       1E6
r16  17   50       1E6
c9   17   99       7.96E-15
c10  17   50       7.96E-15
g7   99   17       14 24 1E-6
g8   17   50       24 14 1E-6
*
* POLE AT 50MHz
*
r17  18   99       1E6
r18  18   50       1E6
c11  18   99       3.18E-15
c12  18   50       3.18E-15
g9   99   18       17 24 1E-6
g10  18   50       24 17 1E-6
*
* POLE AT 50MHz
*
r19  19   99       1E6
r20  19   50       1E6
c13  19   99       3.18E-15
c14  19   50       3.18E-15
g11  99   19       18 24 1E-6
g12  19   50       24 18 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 60kHZ
*
r21  20   21       1E6
r22  20   22       1E6
I3   21   99       2.65
I4   22   50       2.65
g13  99   20       3  24 1.78E-11
g14  20   50       24 3  1.78E-11
*
* POLE AT 50MHZ
*
r23  23   99       1E6
r24  23   50       1E6
c15  23   99       3.18E-15
c16  23   50       3.18E-15
g15  99   23       19 24 1E-6
g16  23   50       24 19 1E-6
*
* OUTPUT STAGE
*
r25  24   99       135E3
r26  24   50       135E3
r27  29   99       70
r28  29   50       70
I5   29   30       4E-7
g17  27   50       23 29 14.3E-3
g18  28   50       29 23 14.3E-3
g19  29   99       99 23 14.3E-3
g20  50   29       23 50 14.3E-3
v4   25   29       .4
v5   29   26       .4
d3   23   25       dx
d4   26   23       dx
d5   99   27       dx
d6   99   28       dx
d7   50   27       dy
d8   50   28       dy
*
MODELS USED
*
• model jx PJF(BETA=1.175E-3 VTO=-2.000 IS=21E-12)
• model dx   D(IS=1E-15)
• model dy   D(IS=1E-15 BV=50)
• ends OP249
```

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

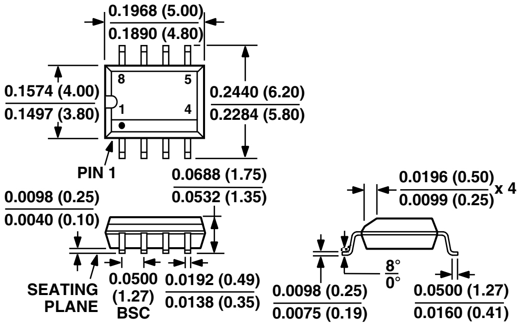
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

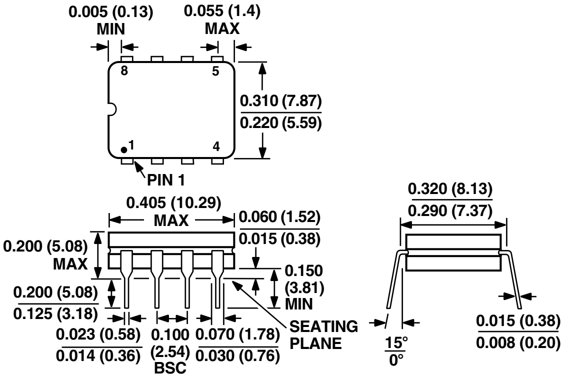
8-Lead Plastic DIP
(N-8)



8-Lead Narrow Body (SOIC)
(SO-8)



8-Lead Cerdip
(Q-8)



C00296a–0–1/02(E)

Revision History

Location	Page
9/01—Data Sheet changed from REV. D to REV. E.	
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Edits to PIN CONNECTIONS	1
Edits to ELECTRICAL CHARACTERISTICS	2, 3
Edits to ABSOLUTE MAXIMUM RATINGS	4
Edits to PACKAGE TYPE	4
Edits to ORDERING GUIDE	4
Deleted WAFER TEST LIMITS	5
Deleted DICE CHARACTERISTICS	5
Edits to TYPICAL PERFORMANCE CHARACTERISTICS	8
Edits to Macro-Model Figure	15
Edits to OUTLINE DIMENSIONS	17

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