Patent Number : 62706, 61007 (R.O.C)
Patent Pending : 83216083 (R.O.C)

GENERAL DESCRIPTION

The EM78056 is an 8-bit microprocessor with low-power, high speed CMOS technology. Integrated onto a single chip are on-chip watchdog timer (WDT), RAM, ROM, programmable real time clock/counter, power down mode, and tri-state I/O.

FEATURES

- Operating voltage range : 2.5V ~ 5.5V
- Available in temperature range: 0°C ~ 70°C.
- Optional instruction cycle period :
  Two oscillator clocks, or
  Four oscillator clocks
- Operating frequency range
  Two oscillator clocks per instruction cycle :

Crystal Type :	DC~12MHz	at 5V	DC~4MHz	at 3V
RC Type :	DC~4MHz	at 5V	DC~4MHz	at 3V

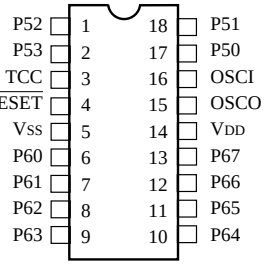
  Four oscillator clocks per instruction cycle :

Crystal Type :	DC~24MHz	at 5V	DC~6MHz	at 3V
RC Type :	DC~4MHz	at 5V	DC~4MHz	at 3V

- 1K x 13 on chip ROM.
- 9 special function registers.
- 33 x 8 general purpose register (SRAM).
- Two bi-directional tri-state I/O ports (12 I/O pins).
- 2 level stack for subroutine nesting.
- 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges.
- Programmable free running on-chip watchdog timer.
- Two R-option pins.
- Selectable oscillator options:
  XTAL1 type (High frequency), XTAL2 type (32.768 KHz), External clock input, RC type.
- 99.9% single instruction cycle commands.
- 18 pin DIP, 18 pin SOIC, 20 pin SSOP.

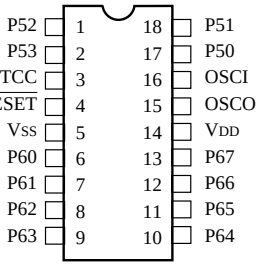
PIN ASSIGNMENTS

EM78056M



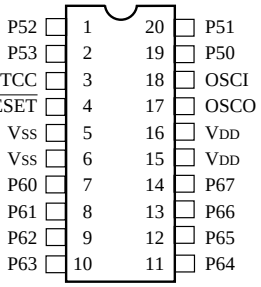
SOIC 18 PIN

EM78056P



DIP 18 PIN

EM78056S



SSOP 20 PIN

FUNCTIONAL BLOCK DIAGRAM

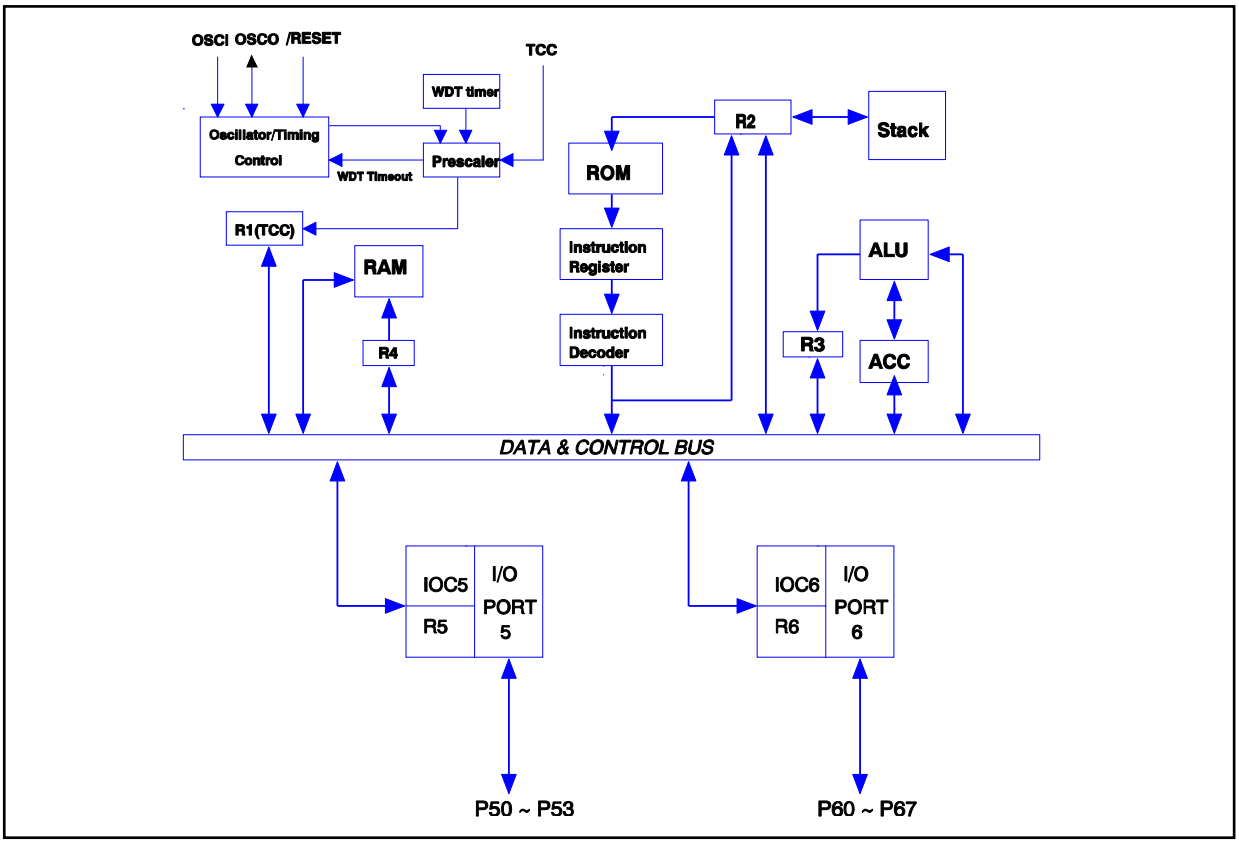


Fig. 2 Functional block diagram

PIN DESCRIPTIONS

Symbol	I/O	Function
OSCI	I	XTAL type : Crystal input terminal or external clock input pin. RC type: RC oscillator input pin.
OSCO	I/O	XTAL type: output terminal for crystal oscillator or external clock input pin. RC type: clock output with a period of one instruction cycle is put on this pin.
TCC	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to V_{DD} or V_{SS} if not in use.
$\overline{\text{RESET}}$	I	Schmitt trigger input pin. If this pin remains logic low, the controller is reset.
P50~P53	I/O	P50~P53 are bi-directional I/O ports. P50 and P51 are also the R-option pins.
P60~P67	I/O	P60~P67 are bi-directional I/O ports.
V_{DD}	-	Power supply pin.
V_{SS}	-	Ground pin.

FUNCTION DESCRIPTIONS

Operational Registers

R0 (Indirect Addressing Register)

- R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

R1 (TCC)

- Increased by an external signal edge applied to TCC pin, or by the instruction cycle clock.
- Written and read by the program as any other register.

R2 (Program Counter) & Stack

- R2 and hardware stack are 10-bit wide. The structure is depicted in Fig.3.
- Generates 1K x 13 on-chip ROM addresses to the relative programming instruction codes. One program page is 512 words long.
- R2 is set all "1"s upon a RESET condition.
- "JMP" instruction allows the direct loading of the lower 9 program counter bits. Thus, “JMP” allows jmup to any loaction on one page.
- “CALL” instruction loads the lower 9 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be any loaction on one page.
- “RET” (“RETL k”,“RETI”) instruction loads the program counter with the contents at the top of stack.
- “MOV R2,A” allows the loading of an address from the A register to the lower 8-bits of PC, and the ninth bit (A8) of PC is cleared.
- “ADD R2,A” allows a relative address be added to the current PC, and the ninth bit of PC is cleared.
- Any instruction which writes to R2 (e.g. “ADD R2,A”,“MOV R2,A”,“BC R2,6”, ...)(except “TBL”) will cause the ninth bit (A8) of PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- “TBL” allows a relative address be added to the current PC (R2+A→R2), and content of the ninth bit (A8) of PC is not changed. Thus, the computed jump can be on the second 256 locations on one program page.
- The most significant bit (A9) will be loaded with the content of bit PS in the status register (R3) upon the execution of a “JMP”, “CALL”, or any instruction which writes to R2.
- All instructions are single instruction cycle (fclk/2) except that the instructions which write to R2 need one more instruction cycle.

R3 (Status Register)

7	6	5	4	3	2	1	0
GP1	GP0	PS	T	P	Z	DC	C

Bit 0 (C) Carry flag
Bit 1 (DC) Auxiliary carry flag
Bit 2 (Z) Zero flag. Set to “1” if the result of an arithmetic or logic operation is zero.
Bit 3 (P) Power down bit. Set to 1 during power on or by a “WDTC” command and reset to 0 by a “SLEP” command.
Bit 4 (T) Time-out bit. Set to 1 by the “SLEP” and “WDTC” command, or during power up and reset to 0 by WDT timeout.

Bit 5 (PS) Page select bit.
0 : Page 0 (Address: 000~1FF)
1 : Page 1 (Address: 200~3FF)
PS is used to preselect a program memory page. When executing a JMP, CALL, or other instruction causes program counter to be changed (e.g. MOV R2,A), PS is loaded into the tenth bit of the program counter, selecting one of the available program memory pages. Note that RET (RETL, RETI) instrunction does not change the PS bit. That is, the return will be always to the page from where the subroutine was called, regardless of the current setting of PS bit.
Bits 6~7 General purpose read/write bits.

R4 (RAM Select Register)

- Bits 0 ~ 5 are used to select up to 40 registers (address: 00~27) in the indirect addressing mode. Refer to Register R0.
- Bits 6 ~ 7 are not used. (Read as "1")
- If no indirect addressing is used, the RSR can be used as a 6-bit wide general purpose read/write register.
- See the configuration of the data memory in Fig. 4.

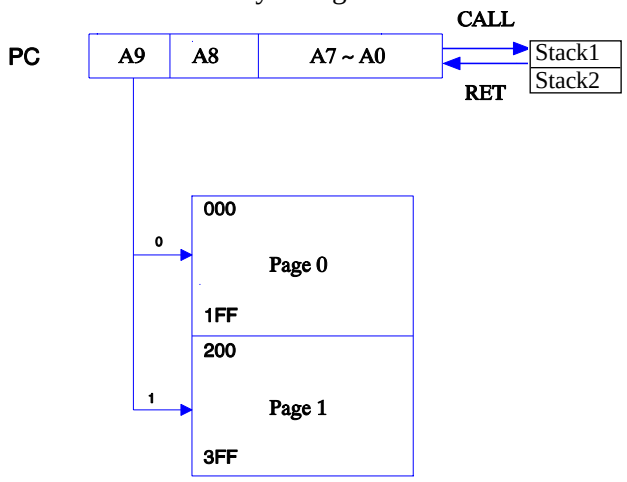


Fig. 3 Program counter organization

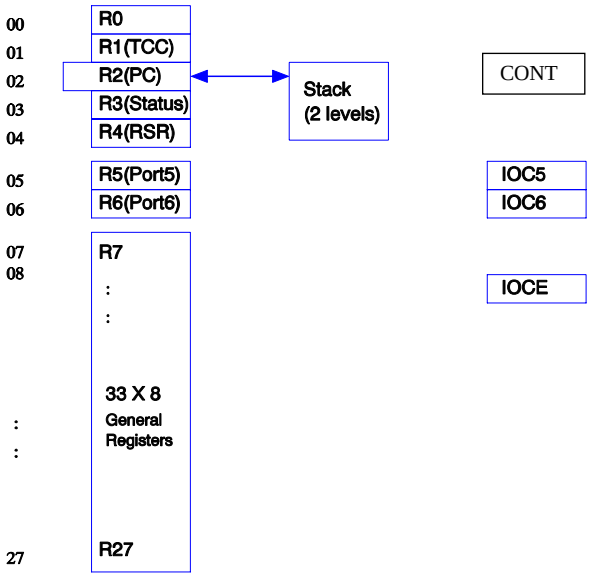


Fig. 4 Data memory configuration

R5 ~ R6 (Port 5 ~ Port 6)

- R5 and R6 are I/O registers.
- Only low order 4 bits are used in R5. The high order 4 bits of R5 will be read as "0".

R7 ~ R27 (General Purpose Register)

- R7 ~ R27 are the 33×8 general purpose registers.

Special Purpose Registers

A (Accumulator)

- Internal data transfer, or instruction operand holding.
- It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
-	-	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB) Prescaler assignment bit.
0: TCC
1: WDT
Bit 4 (TE) TCC signal edge.
0: increment from low to high transition on TCC pin
1: increment from high to low transition on TCC pin
Bit 5 (TS) TCC signal source
0: internal instruction cycle clock
1: transition on TCC pin
Bits 6~7 Not used.

- CONT register is readable and writable.

IOC5 ~ IOC6 (I/O Port Control Register)

- "1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.
- Only low order 4 bits are used in IOC5.

- IOC5 and IOC6 registers are readable and writable.

IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
WTE	-	-	ROC	-	-	-	-

Bit 7 (WTE) Control bit used to enable Watchdog timer.
WTE bit is used only if the CODE Option bit WTC is "1". If WTC bit is "1", then WDT is disabled/enabled by WTE bit.
0: Disable WDT
1: Enable WDT
WTE bit is not used if the CODE Option bit WTC is "0". That is, if WTC bit is "0", WDT is always disabled no matter what the WTE bit is.
WTE bit is readable and writable.

Bit 4 (ROC) ROC is used for the R-option. Setting ROC to “1” will enable the status of R-option pins (P50~P51) to be read by the controller. Clearing ROC will disable the R-option function. If the R-option function is used, the user must connect the P51 pin or/and P50 pin to VSS by a 430KΩ external resistor (Rex). If Rex is connected/disconnected, the status of P50(P51) will be read as “0”/“1” when ROC is set to “1”. Refer to Fig. 8. ROC bit is readable and writable.

Bits 0 ~ 3, 5~6 Not used.

TCC/WDT & Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. The prescaler will be cleared by instructions which write to TCC each time, when assigned to TCC mode. The WDT and prescaler, when assigned to WDT mode, will be cleared by the WDTC and SLEP instructions. Fig. 5 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 in every instruction cycle (without prescaler). Refer to Fig. 5, CLK=Fosc/2 or CLK=Fosc/4 is depended on the CODE Option bit CLKS. CLK=Fosc/2 if CLKS bit is "0", and CLK=Fosc/4 if CLKS bit is "1". If TCC signal source is from external clock input, TCC will increase by 1 on every falling edge or rising edge of TCC pin.
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WTE bit of IOCE register. With no presacler, the WDT time-out period is approximately 18 ms.

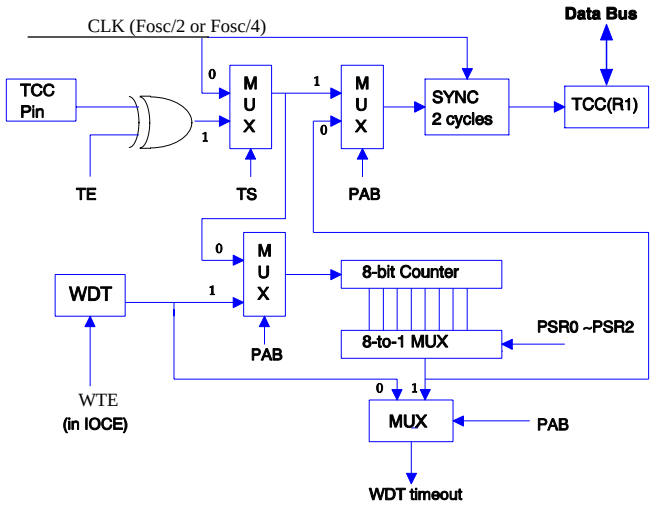


Fig. 5 Block diagram of TCC and WDT

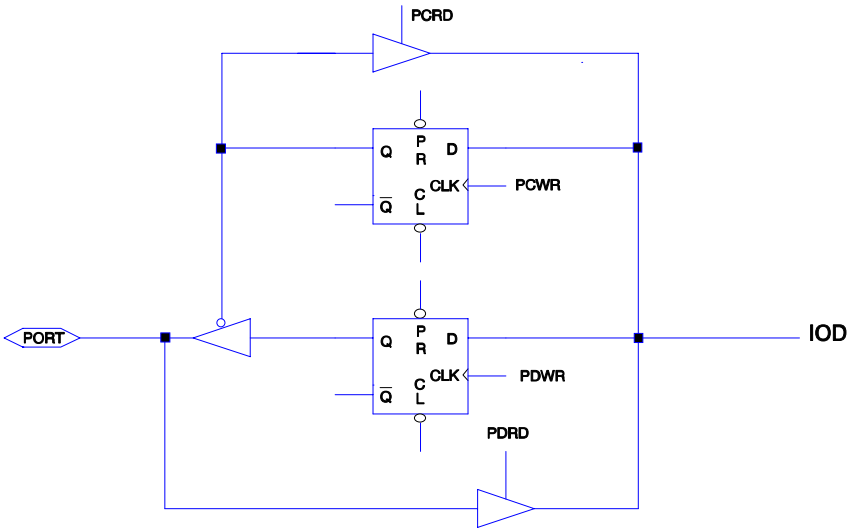


Fig. 6 The circuit of I/O port and I/O control register

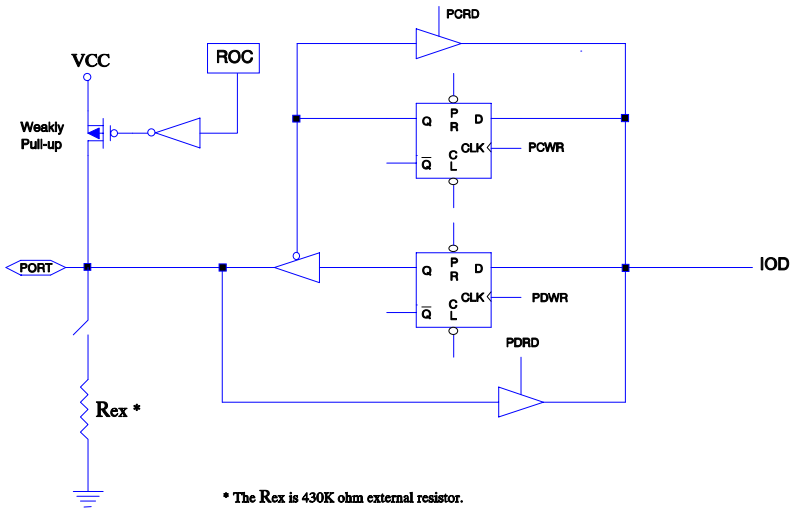


Fig. 7 The circuit of I/O port (P50,P51) with R-option

I/O Ports

The I/O registers, Port 5 ~ Port 6, are bi-directional tri-state I/O ports. Each I/O pin can be defined as “input” or “output” pin by the I/O control register (IOC5 ~ IOC6) under program control. P50~P51 are also the R-option pins which are enabled by software. While R-option function is used, P50~P51 are recommended to be used as output pins. During the period of R-option being enabled, P50~P51 must be programmed as input pins. If external resistor is connected to P50(P51) for R-option function, the current consumption should be noticed in the applications that low power are concerned.
The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig. 6.

RESET and Wake-up

The RESET can be caused by
(1) Power on reset
(2) /RESET pin input “low”, or
(3) WDT timeout (if enabled).

The device will be kept in a RESET condition for a period of approx. 18ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all “1”.
- The upper 3 bits of R3 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- Bits 0~5 of CONT register are set to "1".
- Bit 7 of IOCE register is set to “1” and Bit 4 of IOCE is cleared.

The sleep mose (power down mode) can be entered by executing the SLEP instruction. While entering sleep mode, the WDT (if enabled) is cleared but keeping running. The controller can be awakened by
(1) external reset input on /RESET pin, or
(2) WDT time-out (if enabled).
The two cases will cause the controller reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up).

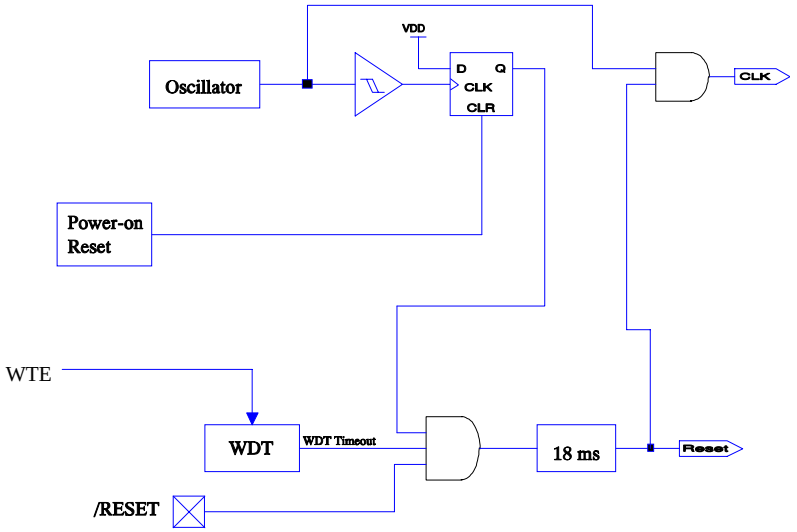


Fig. 8 Block diagram of Reset of controller

Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction execution "MOV R2,A", "TBL", "ADD R2,A", or instructions of arithmetic or logic operation on R2 (e.g. "BS (BC) R2,b", "CLR R2",....). In this case, the execution takes two instruction cycles.

Under some condition, if the specification of the instruction cycle is not suitable for some applications, they can be modified as follows:
(A) one instruction cycle consists of 4 oscillator periods.
(B) "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") is tesed to be true are executed within two instruction cycles. The instructions that write to the program counter also take two instruction cycles.
The Case(A) is selected by the CODE Option bit (CLKS). One instruction cycle consists of two oscillator clocks if CLKS bit is low, or consists of four oscillator clocks if CLKS bit is high. The Case(B) is selected by the CODE Option bit (CYES). The execution of those instructions listed in Case (B) takes one instruction cycle if CYES bit is low, or takes two instruction cycles if CYES bit is high.
Case(A) and Case(B) are independent options, that is, they can be selected individually. Note that once 4 oscillator periods within one instruction cycle is selected in Case(A), the internal clock source to TCC is CLK=Fosc/4 instead of Fosc/ 2 that is shown in Fig. 5.

In addition, the instruction set has the following features:
(1) Every bit of any register can be set, cleared, or tested directly.
(2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.
The symbol "R" represents a register designator which specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 9-bit constant or literal value.

INSTRUCTION BINARY	HEX	HNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0010	0012	RET	[TOP of stack] → PC	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z

INSTRUCTION BINARY	HEX	HNEMONIC	OPERATION	STATUS AFFECTED
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 000k kkkk kkkk	1kkk	CALL k	PC+1 → [SP],(Page, k) → PC	None
1 010k kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

<Note 1> This instruction can operate on IOC5~IOC6, IOCE only.

CODE Option Register

The EM78056 has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

7	6	5	4	3	2	1	0
-	-	LVDD	WTC	HLF	MS	CLKS	CYES

Bit 0 (CYES): Instruction cycle option for special instruction.
0: one cycle
1: two cylcles
Refer to Section on Instruction Set.
Bit 1 (CLKS): Instruction period option.
0: two oscillator periods
1: four oscillator periods
Refer to Section on Instruction Set.
Bit 2 (MS): Oscillator type selection.
0: RC type
1: XTAL type (XTAL1 and XTAL2)
Bit 3 (HLF): XTAL frequency selection.
0: XTAL2 type (Low frequency, 32.768KHz)
1: XTAL1 type (High frequency)
This bit is useful only when Bit 2 (MS) is “1”. When MS is “0”, HLF must be “0”.
Bit 4(WTC): WDT option.
0: WDT is enable. Control bit WTE in IOCE is unused.
1: WDT is enabled. WDT can be disabled/enabled by software programming. Control bit WTE in IOCE is used to disable/enable WDT.
Bit 5(LVDD): Low power control.
0: LVDD must be"0" on the application that VDD>4.5V, and there are appoximately 60μA DC current.
1: LVDD can be "1" only on the application that VDD<4V, and it can save approximately 15μA DC current.
Bit 6: Not used, must be “1”.
Bit 7: Not used, must be “0”.

ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}		0°C to 70°C
Storage temperature	T_{STR}		-65°C to 150°C
Input voltage	V_{IN}		-0.3V to +6.0V
Output voltage	V_O		-0.3V to +6.0V

DC ELECTRICAL CHARACTERISTIC (T_A=0°C ~ 70°C, V_{DD}=5.0V, V_{SS}=0V)

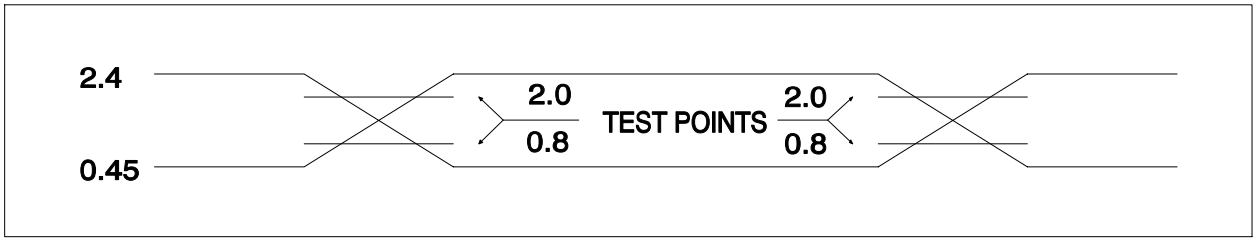
Parameter	Sym.	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current for input pins	I_{IL}	V_{IN} = V_{DD}, V_{SS}			±1	μA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Threshold Voltage	V_{IHT}	$\overline{\text{RESET}}$, TCC	2.0			V
Input Low Threshold Voltage	V_{ILT}	$\overline{\text{RESET}}$, TCC			0.8	V
Clock Input High Voltage	V_{IHX}	OSCI	3.5			V
Clock Input Low Voltage	V_{ILX}	OSCI			1.5	V
Output High Voltage (Port 5,6)	V_{OH}	I_{OH} = -12.0mA	2.4			V
Output Low Voltage (Port 5,6)	V_{OL}	I_{OL} = 12.0mA			0.4	V
Power down current	I_{SB}	All input and I/O pins at V_{DD}, output pin floating, WDT enabled			10	μA
Operating supply current	I_{CC1}	$\overline{\text{RESET}}$='High', Fosc=12MHz (MS="1", CLKS="0", HLF="1"), output pin floating			4	mA
Operating supply current	I_{CC2}	$\overline{\text{RESET}}$='High', Fosc=4MHz (MS="1", CLKS="0", HLF="1"), output pin floating			2	mA
Operating supply current (VDD=3V)	I_{CC3}	$\overline{\text{RESET}}$='High', Fosc=32KHz (MS="1", CLKS="0", HLF="0"), output pin floating, WDT disabled		15	30	μA

AC ELECTRICAL CHARACTERISTICS (T_A=0°C ~ 70°C, V_{DD}=5.0V, V_{SS}=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time (CLKS="0")	Tins	XTAL Type	167		DC	ns
		RC Type	500		DC	ns
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Device reset hold time	Tdrh	Ta = 25°C		18		ms
Watchdog timer period	Twdt	Ta = 25°C		18		ms

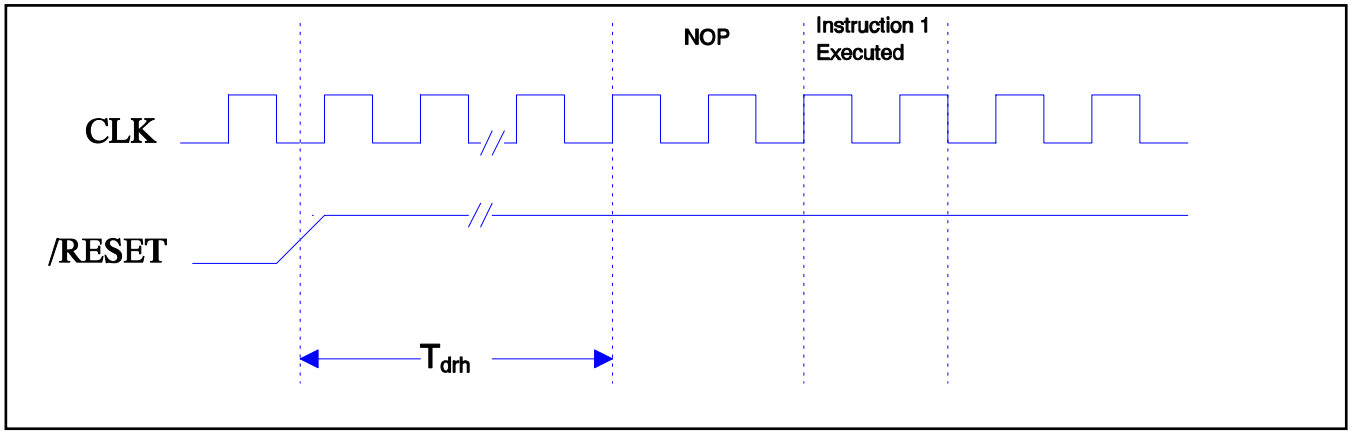
Note 1: N= selected prescaler ratio.

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing (CLKS="0")



TCC Input Timing (CLKS="0")