RC7101

Low Skew Buffers

100MHz SDRAM Clock Buffers

Features

- 18 skew controlled outputs
- Supports up to four SDRAM DIMMs
- Skew between any two outputs is less than 250 pS
- I^2C Serial Interface for programming options
- Multiple power and ground pins for noise reduction
- Single 3.3V power supply
- 48 Pin SSOP package

Applications

- SDRAM Clock Buffers for Intel's 440BX chip set

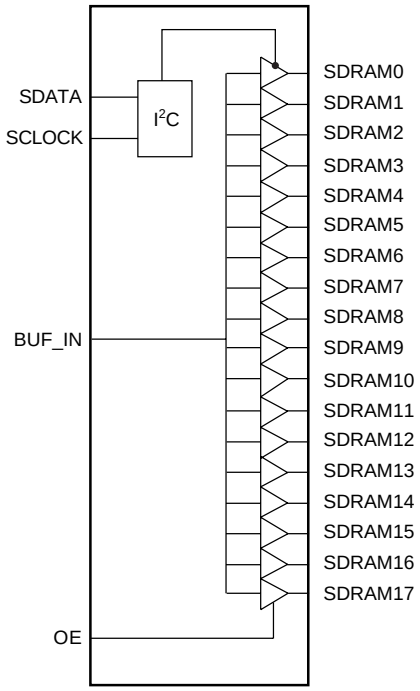
Description

The RC7101 is a low voltage eighteen output clock buffer which supports 4 DIMMs. The skew between any two outputs is less than 250 pS and the buffers can be individually enabled or disabled by programming via the I^2C serial interface. The SDATA and SCLK serial inputs both have internal pull-up resistors.

An Output Enable (OE) pin is also provided so that all the outputs can be tri-stated when held low. This pin is normally high and has an internal pull-up resistor.

OE	SDRAM0:3	SDRAM4:7	SDRAM8:11	SDRAM12:15	SDRAM16:17
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	BUF_IN	BUF_IN	BUF_IN	BUF_IN	BUF_IN

Block Diagram



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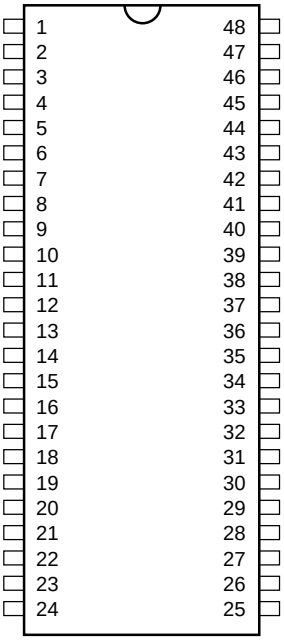
Pin Assignments



48 Pin SSOP

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	NC	13	SDRAM4	25	SCLOCK	37	VDD
2	NC	14	SDRAM5	26	VSS	38	OE
3	VDD	15	VSS	27	VSS	39	VSS
4	SDRAM0	16	VDD	28	SDRAM17	40	SDRAM12
5	SDRAM1	17	SDRAM6	29	VDD	41	SDRAM13
6	VSS	18	SDRAM7	30	VSS	42	VDD
7	VDD	19	VSS	31	SDRAM8	43	VSS
8	SDRAM2	20	VDD	32	SDRAM9	44	SDRAM14
9	SDRAM3	21	SDRAM16	33	VDD	45	SDRAM15
10	VSS	22	VSS	34	VSS	46	VDD
11	BUF_IN	23	VDD	35	SDRAM10	47	NC
12	VDD	24	SDATA	36	SDRAM11	48	NC

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Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
BUF_IN	11	IN	Input for clock buffers
SDRAM0:3	4, 5, 8, 9	OUT	SDRAM Byte 0 clock outputs
SDRAM4:7	13, 14, 17, 18	OUT	SDRAM Byte 1 clock outputs
SDRAM8:11	31, 32, 35, 36	OUT	SDRAM Byte 2 clock outputs
SDRAM12:15	40, 41, 44, 45	OUT	SDRAM Byte 3 clock outputs
SDRAM16:17	21, 28	OUT	SDRAM clock outputs
OE	38	IN	Output enable which will tri-state all the outputs when held low
SDATA	24	I/O	Serial Data Line
SCLOCK	25	IN	Serial Clock input
VDD	3, 7, 12, 16, 20, 29, 33, 37, 42, 46	Power	Power supply at 3.3V for SDRAM buffers
VDD	23	Power	Power supply at 3.3V for I^2C circuit
VSS	6, 10, 15, 19, 22, 27, 30, 34, 39, 43	Ground	Ground for SDRAM buffers
VSS	26	Ground	Ground for I^2C circuit
NC	1, 2, 47, 48	NC	No Connections.

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, V_{DD}	-0.5		5	V
Input Voltage	-0.5		V_{DD}+0.5	V
Output Applied Voltage	-0.5		V_{DD}+0.5	V
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
V_{DD}	3.135	3.3	3.465	V
Ambient Temperature	0		70	°C

Electrical Characteristics T_A = 0°C to 70°C, V_{DD} = 3.3V±5%

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}, Input low voltage		-0.3		0.8	V
V_{IH}, Input high voltage		2.0		V_{DD}+0.3	V
I_{IL}, Input low current (BUF_IN)				-25	µA
I_{IH}, Input high current (BUF_IN)				10	µA
I_{IL}, Input low current OE, SDATA, SCLOCK)				-50	µA
I_{IH}, Input high current (OE, SDATA, SCLOCK)				10	µA
V_{OL}, Output low voltag	I_{OL} = 23mA			0.4	V
V_{OH}, Output high voltage	I_{OH} = -30mA	2.6			V
I_{OL}, Output low current	V_{OL} = 0.8V	40			mA
I_{OH}, Output high current	V_{OH} = 2.0V			-54	mA
I_{DD}, Supply current	f = 100MHz				mA
I_{DD}, Supply current	f = 66MHz				mA
I_{DD}, Supply current	OE = 0				mA
C_{IN}, Input capacitance				5	pF
F_{IN}, Input frequency				150	MHz

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Switching Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
T_{PD}, Propagation delay	V_T = 1.5V	1		5	ns
T_R, Rise time	0.4 to 2.4V	0.5		1.5	ns
T_F, Fall time	2.4 to 0.4V	0.5		1.5	ns
T_D, Duty cycle	V_T = 1.5V	45		55	%
T_{EN}, Output enable time	V_T = 1.5V	1		8	ns
T_{DIS}, Output disable time	V_T = 1.5V	1		8	ns
T_{SK}, Skew	V_T = 1.5V			250	ps
Z_O, Output impedance			15		Ω

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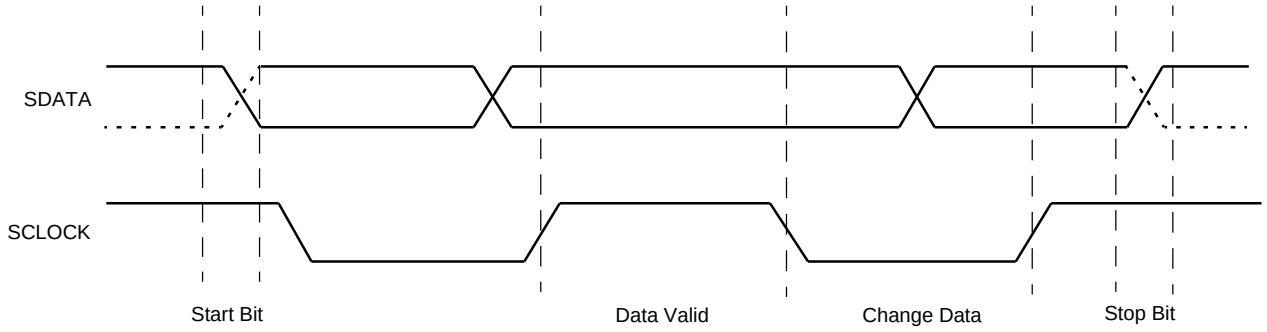
Serial Data Interface

Signaling Requirements for the I²C Serial Port

To initiate communications with the serial port, a start bit is invoked. The start bit is defined as the SDATA line is brought low while the SCLOCK is held high. Once the start bit is initiated, valid data can then be sent. Data is considered to be valid when the clock goes to and remains in the high state. The data can change when the clock goes low. To terminate the transmission, a stop bit is invoked. The stop bit occurs when the SDATA line goes from a low to a high state while the SCLOCK is held high. See Figure below.



The data transfer rate is 100kbits/s in the standard mode and 400kbits/s in the fast mode. The serial protocol uses block writes only. Bytes are written with the lowest first and the highest last with the ability to stop after any complete byte has been transferred. The clock driver is a slave/receiver only and is only capable of receiving data with the exception of sending acknowledgements. It is not capable of sending data.

Byte writing sequence

The buffer is accessed when the slave address byte is received. Each byte of data is followed by an acknowledge bit. The address bit sequence is 1 1 0 1 0 0 1 followed by the R/W# bit (0). Bits are written with the Most Significant Bit (MSB) first. The MSB Bit is bit 7 and the LSB is bit 0. The Byte writing sequence is as shown in the table below.

Byte Sequence	Byte name	Bit sequence 7	6	5	4	3	2	1	0
1	Slave address	1	1	0	1	0	0	1	0
2	Command Code	X	X	X	X	X	X	X	X
3	Byte Count	X	X	X	X	X	X	X	X
4	Data Byte 0	see table below							
5	Data Byte 1	see table below							
6	Data Byte 2	see table below							
7	Data Byte 3	X	X	X	X	X	X	X	X
8	Data Byte 4	X	X	X	X	X	X	X	X
9	Data Byte 5	X	X	X	X	X	X	X	X
10	Data Byte 6	X	X	X	X	X	X	X	X

Data Bytes 0 to 2 Map

Bit	Pin	Name	Description
Data Byte 0: SDRAM Active/Inactive Register (1 = enable, 0 = disable)			
7	18	SDRAM7	(ACTIVE/INACTIVE)
6	17	SDRAM6	(ACTIVE/INACTIVE)
5	14	SDRAM5	(ACTIVE/INACTIVE)
4	13	SDRAM4	(ACTIVE/INACTIVE)
3	9	SDRAM3	(ACTIVE/INACTIVE)
2	8	SDRAM2	(ACTIVE/INACTIVE)
1	5	SDRAM1	(ACTIVE/INACTIVE)
0	4	SDRAM0	(ACTIVE/INACTIVE)
Data Byte 1: SDRAM Active/Inactive Register (1 = enable, 0 = disable)			
7	45	SDRAM15	(ACTIVE/INACTIVE)
6	44	SDRAM14	(ACTIVE/INACTIVE)
5	41	SDRAM13	(ACTIVE/INACTIVE)
4	40	SDRAM12	(ACTIVE/INACTIVE)
3	36	SDRAM11	(ACTIVE/INACTIVE)
2	35	SDRAM10	(ACTIVE/INACTIVE)
1	32	SDRAM9	(ACTIVE/INACTIVE)
0	31	SDRAM8	(ACTIVE/INACTIVE)
Data Byte 2: SDRAM Active/Inactive Register (1 = enable, 0 = disable)			
7	28	SDRAM17	(ACTIVE/INACTIVE)
6	21	SDRAM16	(ACTIVE/INACTIVE)
5		reserved	reserved
4		reserved	reserved
3		reserved	reserved
2		reserved	reserved
1		reserved	reserved
0		reserved	reserved

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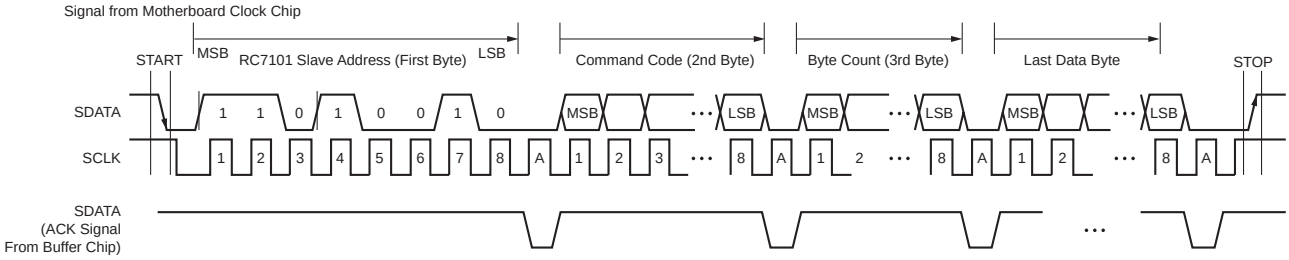
RC7101 I²C Interface Write Sequence



Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDATA at every 8th bit. The 8 bit data from SDATA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

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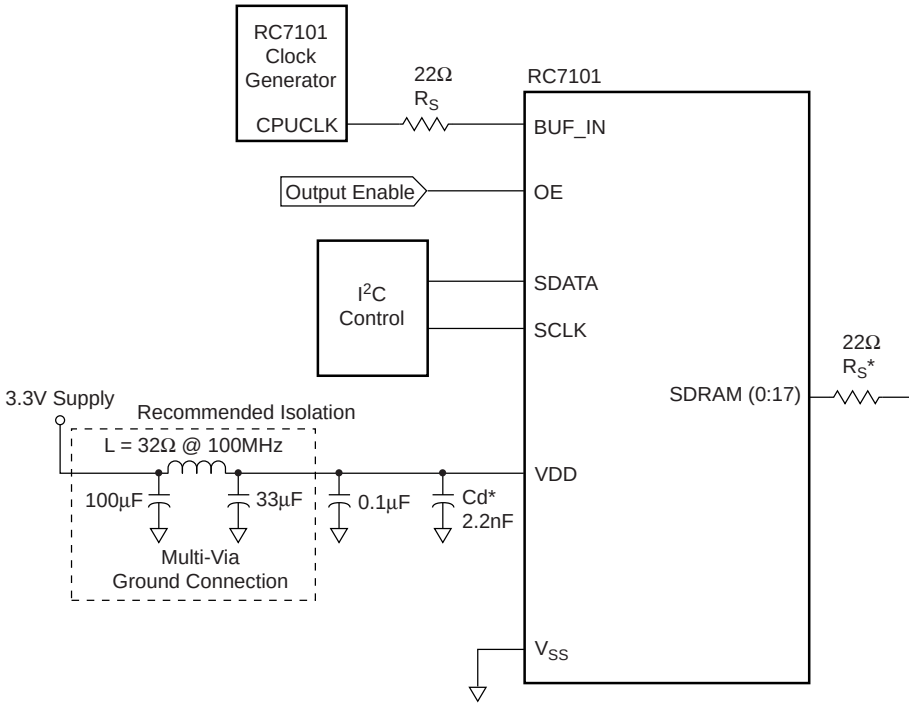
Application Circuit



*Each VDD pin should be separately decoupled with a 2.2nF capacitor.

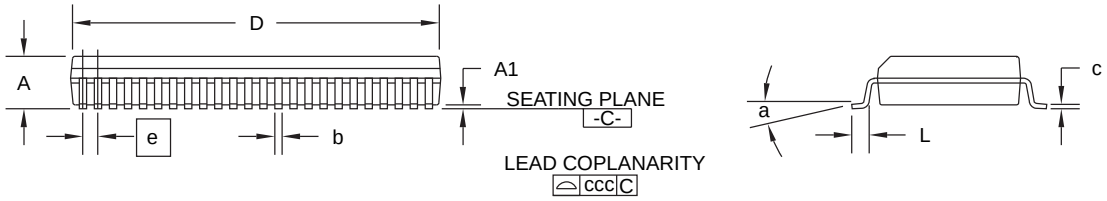
Mechanical Dimensions

48 pin SSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



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Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7101	0°C to 70°C		48 SSOP	RC7101

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