SUN MICROELECTRONICS

STP2200ABGA

July 1997

USC

DATA SHEET — Uniprocessor System Controller

DESCRIPTION

The Uniprocessor System Controller (USC) has a DRAM memory controller and functions to regulate the flow of requests and data on the UPA bus. It also controls the resets going to all UPA clients.

Features

- Controls up to eight standard SS-10/SS-20-type DRAM SIMMs
- Supports various memory SIMM organizations: 16 MB, 64 MB, and 256 MB as well as dual-stacked 128-MB SIMMs
- Controls and generates a number of resets for the system
- Programmed via a standard 8-bit asynchronous interface (EBus)
- JTAG interface allows full chip scan
- 225-pin ABGA package

Benefits

- Standard workstation memory
- Flexibility
- High integration
- Allows design of low-cost, low-chip-count embedded systems
- Ease of design and testability
- Low cost

The USC is used as the system controller of a complete Uniprocessor UltraSPARC system.

Note: *Instead of using the U2S, the USC can also be used with the UPA to PCI-bus; I/O interface controller (U2P)*

UPA Devices

Abbreviations		Part Number	Description
USC	SC_UP	STP 2200ABGA	Uniprocessor System Controller
RIC	RISC	STP2210QFP	Reset/Interrupt/Clock Controller
U2S	SYSIO	STP2220ABGA	UPA to SBus I/O interface controller
U2P	Psycho	STP2222ABGA	UPA to PCI bus I/O Interface controller
XBI	BMX	STP2230SOP	Crossbar Data Path

Note: *This data sheet refers to the UPA to System I/O interface. The UPA to PCI bus Interface controller (U2P) can be substituted where U2S appears.*

BLOCK AND TYPICAL APPLICATION DIAGRAMS

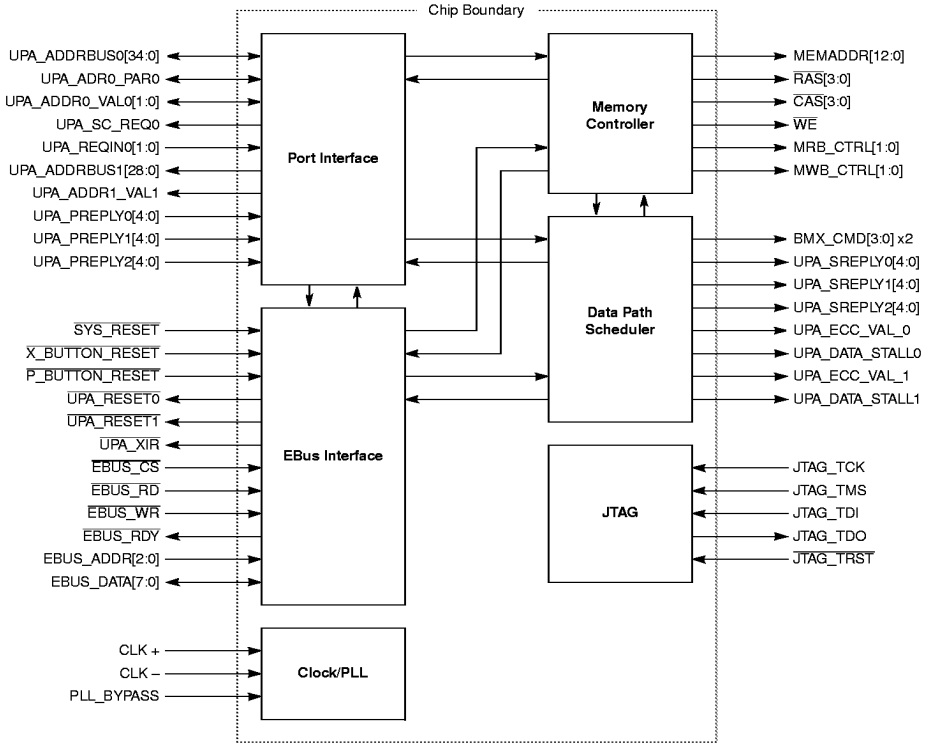


Figure 1. USC Block Diagram

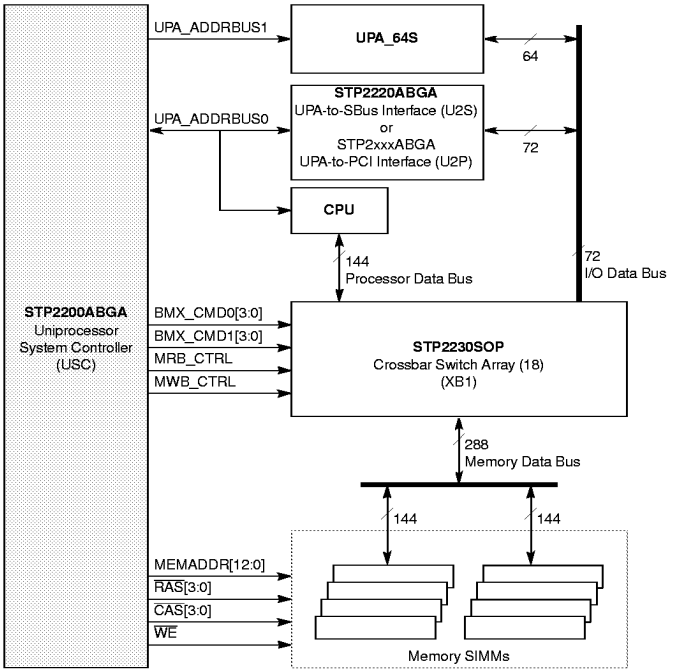


Figure 2. USC Typical Application Diagram

SIGNAL DESCRIPTIONS

UPA Interface Signals

Signal	I/O	Description
UPA_ADDRBUS0[34:0]	I/O	Address bus 0 (processor/U2S)
UPA_ADR0_PAR	I/O	Parity for address bus 0
UPA_ADDR0_VAL[1:0]	I/O	[0] = processor, [1] = U2S
UPA_SC_REQ0	O	USC request for address bus 0
UPA_REQIN0[1:0]	I	Client address bus 0 arbitration requests: [0] = processor, [1] = U2S
UPA_ADDRBUS1[28:0]	O	Address bus for UPA64S
UPA_ADDR1_VAL1	O	Address valid signal for UPA64S
UPA_SREPLY0_[4:0]	O	S_Reply for processor
UPA_SREPLY1_[4:0]	O	S_Reply for U2S
UPA_SREPLY2_[2:0]	O	S_Reply for UPA64S
UPA_PREPLY0_[4:0]	I	P_Reply from processor
UPA_PREPLY1_[4:0]	I	P_Reply from U2S
UPA_PREPLY2_[1:0]	I	P_Reply from UPA64S
$\overline{\text{UPA\_RESET0}}$	O	Reset for processor, tied to the U2S's $\overline{\text{UPA\_ARB\_RESET}}$
$\overline{\text{UPA\_RESET1}}$	O	Reset for U2S
$\overline{\text{UPA\_XIR}}$	O	XIR reset for processor only
UPA_ECC_VAL_0	O	ECC valid for processor
UPA_ECC_VAL_1	O	ECC valid for U2S
UPA_DATA_STALL0	O	Stall data to processor
UPA_DATA_STALL1	O	Stall data to U2S

Memory Interface Signals

Signal	I/O	Description
MEMADDR[12:0]	O	Row/column address
$\overline{\text{RAS}}$[3:0]	O	$\overline{\text{RAS}}$ per SIMM pair
$\overline{\text{CAS}}$[3:0]	O	$\overline{\text{CAS}}$ (four copies)
$\overline{\text{WE}}$	O	Write enable

Crossbar Interface Signals

Signal	Type	Description
BMX_CMD0[3:0]	O	Command to XB1 crossbar array of 18 devices
MRB_CTRL0	O	Fill the XB1 read buffer
MWB_CTRL0	O	Drain the XB1 write buffer

Crossbar Interface Signals

Signal	Type	Description
BMX_CMD1[3:0]	O	Duplicate of BMX_CMD0[3:0]
MRB_CTRL1	O	Duplicate of MRB_CTRL0
MWB_CTRL1	O	Duplicate of MWB_CTRL0

EBus Signals

Signal	Type	Condition	Description
EBUS_DATA[7:0]	I/O	5-V tolerant	Data in and data out pins - 3.3 volt output level
$\overline{\text{EBUS\_CS}}$	I	5-V tolerant	Chip select for USC on the EBus
EBUS_ADDR[2:0]	I	5-V tolerant	EBus address
$\overline{\text{EBUS\_RDY}}$	O		EBus ready to the STP2001 SLAVIO- 3.3 volt output level
$\overline{\text{EBUS\_WR}}$	I	5-V tolerant	Indicates write on EBus
$\overline{\text{EBUS\_RD}}$	I	5-V tolerant	Indicates read on EBus

Miscellaneous Signals

Signal	Type	Condition	Description
CLK+	I	PECL	System clock (differential)
CLK–	I	PECL	System clock (differential)
$\overline{\text{SYS\_RESET}}$	I	5-V tolerant	Power-on reset; pulldown
$\overline{\text{P\_BUTTON\_RESET}}$	I	5-V tolerant	POR button reset
$\overline{\text{X\_BUTTON\_RESET}}$	I	5-V tolerant	XIR button reset
PLL_BYPASS	I		Bypass internal PLL
JTAG_TDI	I	5-V tolerant	Test data input
JTAG_TDO	O		Test data output- 3.3 volt output level
JTAG_TCK	I	5-V tolerant	Scan clock
JTAG_TMS	I	5-V tolerant	Test mode select; pullup
$\overline{\text{JTAG\_TRST}}$	I	5-V tolerant	Reset TAP controller; pullup
DEBUG[3:0]	O		Debug pins
PM_OUT	O		Process monitor output

Power and Ground

Signal	Description
V_{DD}	+3.3 V
V_{SS}	Ground

Power and Ground

Signal	Description
PLL_VDD	Power for PLL
PLL_GND	Ground for PLL
V_{CC}	5-V reference for 5-V tolerant inputs

TECHNICAL OVERVIEW

The USC implements three UPA ports on two address buses. It has a programmable memory controller and an EBus interface. Addresses flow through the USC. Data flows through the crossbar switches.

UPA Port Interface (PIF)

The PIF is responsible for receiving UPA packets, decoding their destinations, and forwarding the packets to their proper destinations. The PIF also receives all P_Replys from UPA clients.

UPA address bus 0 has two clients: the processor and U2S (UPA-to-SBus Interface), or U2P (UPA-to-PCI Interface). The PIF controls the arbitration on UPA address bus 0, for its two clients and itself. The two other masters on this bus are the processor and one of the system I/O devices. The PIF arbitration algorithm is described in the USC User Manual.

Noncached transactions are typically forwarded to a system I/O chip. Cached transactions are typically forwarded to the memory controller. The PIF maintains data coherency in the system between the processor cache, main memory, and the U2S merge buffer.

The UPA address bus 1 supports a single UPA64S device. This address bus is output only on the USC (for example: unidirectional), and the USC is always the master. This interface is typically used for a graphic slave device. The PIF will only generate and receive truncated P_Reply and S_Reply packets going to and coming from the UPA64s device.

The PIF contains three sets of the following registers (one for each UPA port, processor, U2S, UPA 64S device):

- SC_Port_Config registers
- SC_Port_Status registers

UPA Data Path Scheduler (DPS)

The DPS is responsible for regulating the flow of data throughout the system. It generates the following:

- STP2230SOP (XB1/BMX) crossbar switch commands;
- S_Replys for all clients;
- UPA_DATA_STALL signals;
- UPA_ECC_VAL signals.

DPS contains no software-visible registers.

Memory Controller (MC)

The MC is responsible for controlling the SIMMs. It performs the following functions:

- Generates timing for read, write, and refresh;
- Converts the physical address in the UPA packet into row and column addresses;
- Maintains the refresh timer;
- Controls loading and unloading of data from the XB1 read and write buffers.

The PIF forwards memory requests to the MC. The MC communicates with the DPS to schedule delivery of data.

The MC contains the following registers:

- MC_Control 0; and
- MC_Control 1

These registers are described in further detail in the USC User Guide.

EBus Interface (EB)

The EB implements an interface to EBus, an asynchronous 8-bit interface controlled by the STP2001 Slave I/O Controller (SLAVIO). Since the USC contains no UPA data path, all reading and writing of internal registers has to take place via EBus. Since all internal registers are 32 bits wide, the EB has to perform packing and unpacking.

The EB block implements reset logic and contains a number of global registers.

- SC_Control register for controlling resets and logging reset status;
- SC_ID register, which contains the USC's JEDEC ID number, implementation and version numbers, and the number of UPA ports that the chip supports;
- Performance counters: SC_Perf_Ctrl, SC_Perf0, and SC_Perf1. These counters can be configured to count various events for performance analysis.

Clock and PLL

The USC will operate at a maximum frequency of 100 MHz (10 nanoseconds cycle time). It is a completely synchronous, edge-triggered, register-based design which uses only the rising edge of the clock to update the flip-flops.

The chip also contains a phase-locked loop (PLL) to remove the skew introduced by the internal clock distribution network. This improves I/O timing.

JTAG Interface

The USC provides a JTAG interface for full chip scan which is used only for ATPG and in-system interconnect testing. The USC's boundary is shadowed to allow for board-level test.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply voltage	0	4.1	V
V_{CC}	DC reference voltage	0	6.0	V
V_{IN}	Input voltage (any pin)	V_{SS}-0.3	V_{DD} + 0.3	V
P_D	Continuous power dissipation		2.5	W
T_{STG}	Storage temperature range	-40	125	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	DC supply voltage	3.15	3.3	3.45	V
V_{CC}	5V reference voltage		5.0	5.25	V
V_{IN}	Input voltage	V_{SS}-0.3		V_{DD} + 0.3	V
T_C	Case temperature			70	°C
T_J	Operating junction temperature			105	°C

Capacitance [1]

Symbol	Parameter	Condition	Max	Units
C_{IN}	Input capacitance		10	pF
C_{OUT}	Output capacitance		10	pF
C_{IO}	I/O capacitance		15	pF

1. The parameter values are not tested, they are provided from simulation.

DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage, CLK + / –	PECL inputs	V_{DD}-1.81	V_{DD}-1.475	V
V_{IH}	Input high voltage, CLK + / –	PECL inputs	V_{DD}-1.165	V_{DD}-0.88	V
I_{IN}	Input current			10	µA
V_{OL}	Output low voltage	leakage current only		0.4	V
V_{OH}	Output high voltage	leakage current only	2.4		V
I_{OZ}	High Z leakage current			10	µA
I_{DD}	Supply current			758	mA
P_D	Power dissipation			2500	mW

AC CHARACTERISTICS

Nearly all inputs and outputs are registered and are referenced to the PECL differential input clock (CLK+ and CLK–). This clock input controls an on-board PLL. These signals are clocked by the rising edge of CLK+ at the crossover between CLK+ and CLK– (where both signals are at the same voltage). All inputs are applied with a rise and fall time of 1.0 nanosecond (ns).

The JTAG signals, are referenced to JTAG_TCK. They are asynchronous signals with respect to CLK+/CLK–.

The following signals are asynchronous to CLK + and CLK – and the JTAG clock. They include resets and the EBus Interface signals:

EBUS_ADDR[2:0]

$\overline{\text{EBUS\_CS}}$

$\overline{\text{EBUS\_RD}}$

$\overline{\text{EBUS\_WR}}$

EBUS_DATA[7:0]

$\overline{\text{P\_RESET}}$

$\overline{\text{X\_RESET}}$

$\overline{\text{SYS\_RESET}}$

$\overline{\text{JTAG\_TRST}}$

AC Characteristics, UPA_CLK+ / UPA_CLK –

Parameter	Signal Name	Condition	-83		-100		Units
			Min	Max	Min	Max	
t_{CYCLE}	CLK+ /CLK–		40.0	83.3	40	100.0	MHz
t_{WH}	CLK+ /CLK–		5.4		4.4		ns
t_{WL}	CLK+ /CLK–		5.4		4.4		ns
t_E	CLK+ /CLK–	Rising		600		600	ps
t_E	CLK– /CLK–	Falling		600		600	ps

AC Characteristics, Signals Referenced to Rising Edge of UPA_CLK

Parameter	Signal Name	Condition	-83		-100		Units
			Min	Max	Min	Max	
t_{SU}	UPA signals		2.5		3.0		ns
t_{H}	UPA signals		0.5		0.5		ns
t_{CO}	UPA signals	70 pF		6.1		4.1	ns
t_{VO}	UPA signals		0.5		0.5		ns
t_{CO}	BMX_CMD0[3:0]	70 pF		6.1		4.1	ns
t_{CO}	BMX_CMD1[3:0]	70 pF		6.1		4.1	ns
t_{CO}	MRB_CTRL[1:0]	70 pF		6.1		4.1	ns
t_{CO}	MWB_CTRL[1:0]	70 pF		6.1		4.1	ns
t_{CO}	MEMADDR[12:0]	70 pF		6.1		4.1	ns
t_{CO}	$\overline{\text{RAS}}$[3:0]	70 pF		6.1		4.1	ns
t_{CO}	$\overline{\text{CAS}}$[3:0]	70 pF		6.1		4.1	ns
t_{CO}	$\overline{\text{WE}}$	70 pF		6.1		4.1	ns
t_{CO}	$\overline{\text{EBUS\_RDY}}$	70 pF		11.9		11.9	ns

AC Characteristics, JTAG_TCK and Signals Referenced to JTAG_TCK

Parameter	Signal Name	Condition	-83		-100		Units
			Min	Max	Min	Max	
t_{CYCLE}	JTAG_TCK			10.0		10.0	MHz
t_{WH}	JTAG_TCK		30.0	70.0	30.0	70.0	ns
t_{WL}	JTAG_TCK		30.0	70.0	30.0	70.0	ns
t_{E}	JTAG_TCK	Rising		20.0		20.0	ns
t_{E}	JTAG_TCK	Falling		20.0		20.0	ns
t_{SU}	JTAG_TDI	Wrt rising edge of JTAG_TCK	2.5		2.5		ns
t_{H}	JTAG_TDI	Wrt rising edge of JTAG_TCK	6.5		6.5		ns
t_{SU}	JTAG_TMS	Wrt rising edge of JTAG_TCK	2.5		2.5		ns
t_{H}	JTAG_TMS	Wrt rising edge of JTAG_TCK	6.5		6.5		ns
t_{CO}	JTAG_TDO	70 pF; Wrt falling edge of JTAG_TCK		16.0		16.0	ns

Signal Timing Definition

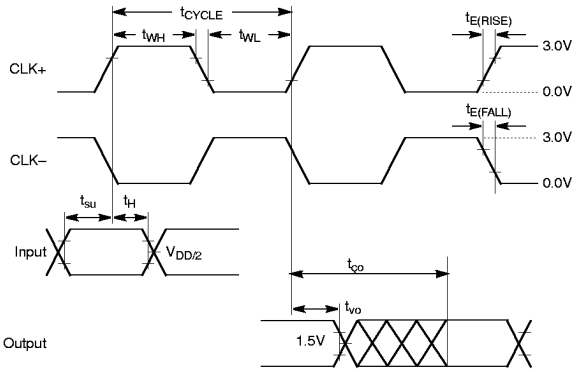


Figure 3. Signal Timing Definition

PLL Specifications

PLL and Clock Distribution Circuitry

The schematic below shows the PLL scheme inside the USC.

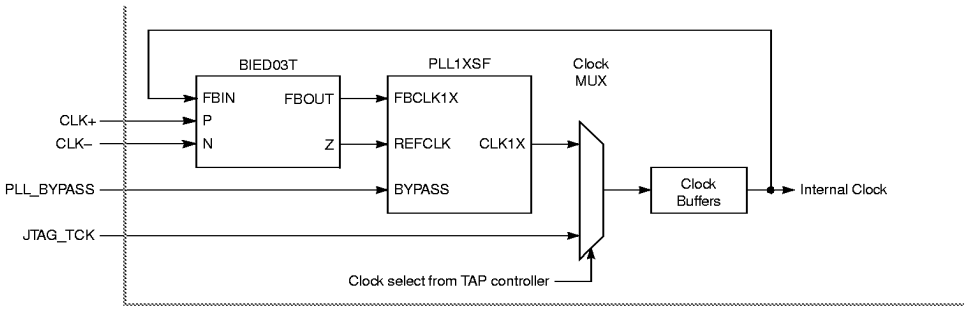


Figure 4. PLL and Clock Distribution Schematic

Power Supply Filter

The PLL power should be filtered with the following part or equivalent to reduce the system noise injected into the PLL by the system: TDK ACF321825 EMI/RFI filter.

TIMING DIAGRAMS

Bus Timings

All data transfers have a dead cycle between them, except for back-to-back single writes from the processor to a graphics slave device.

The following diagrams show some best-case response timing for the USC.

Figure 5 shows the best-case timing for forwarding a PRequest on address bus 0.

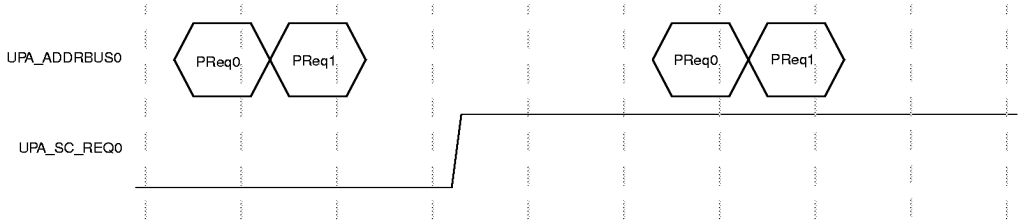


Figure 5. Best-Case PRequest-to-PRequest Timing (ABus0 to ABus0)

Figure 6 shows the best-case timing for sending an SRequest that is triggered by a PRequest.

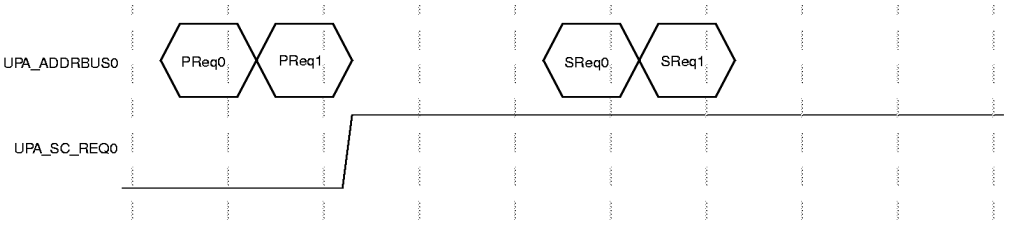


Figure 6. Best-Case PRequest-to-SRequest Timing (ABus0 to ABus0)

Since the USC is always the master of address bus 1 and no arbitration is ever required on that bus, the time it takes for the USC to forward a packet from address bus 0 to address bus 1 is faster than between two devices on address bus 0, as shown in *Figure 7*.

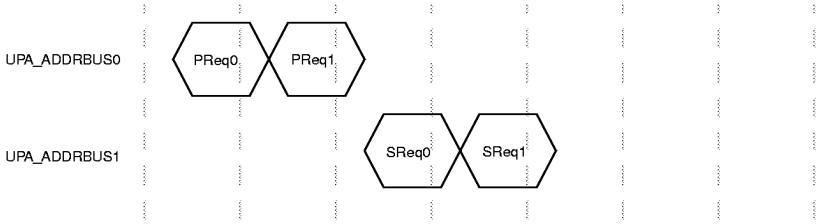


Figure 7. Best-Case PRequest-to-SRequest Timing (ABus0 to ABus1)

Figure 8 and *Figure 9* show the best-case timing for non-cacheable single and block read from U2S referenced to the time the P_Reply is issued from the slave. The timing for non-cacheable read from the fast frame buffer (FFB) (UPA64S) is the same, except that it is referenced to a single-cycle P_RASB instead of the two-cycle P_RAS/P_RAB.

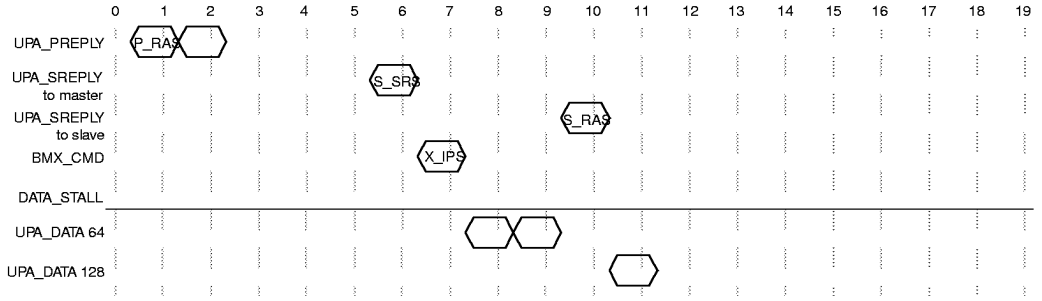


Figure 8. Best-Case Timing for Noncached Single Read, UPA64 -> UPA128

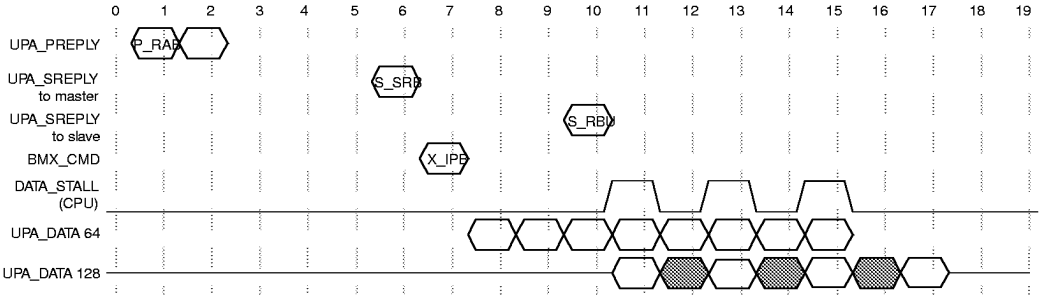


Figure 9. Best-Case Timing for Noncached Block Read, UPA64 -> UPA128

Figure 10 and *Figure 11* show the best-case timing for a non-cacheable single and block write to the U2S. A non-cacheable write to the FFB has similar timing, except that the time it takes to forward the PRequest is slightly less.

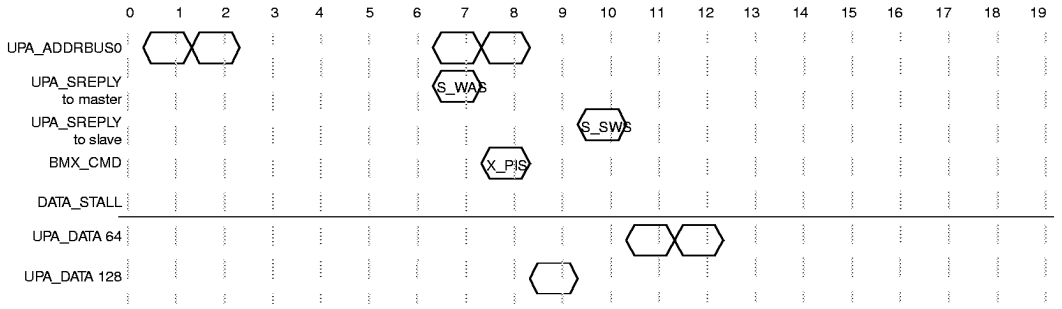


Figure 10. Best-Case Timing for Non-Cached Single Write, UPA128 -> UPA64

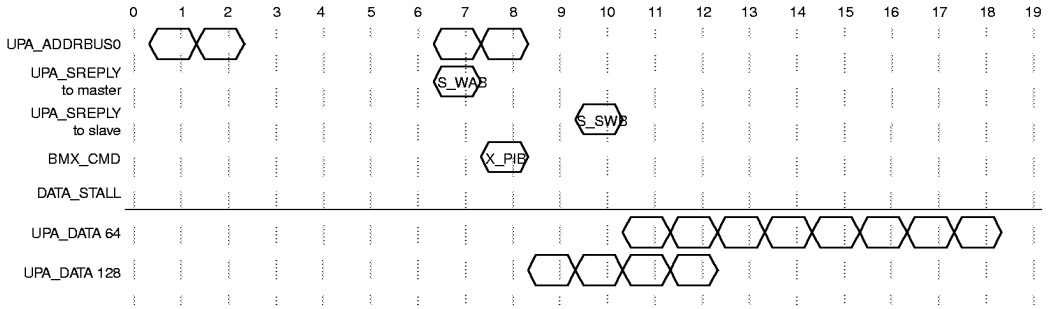


Figure 11. Best-Case Timing for Non-Cached Block Write, UPA128 -> UPA64

Figure 12 and *Figure 13* show a U2S single and block read from the FFB, referenced to the P_Reply from the FFB.

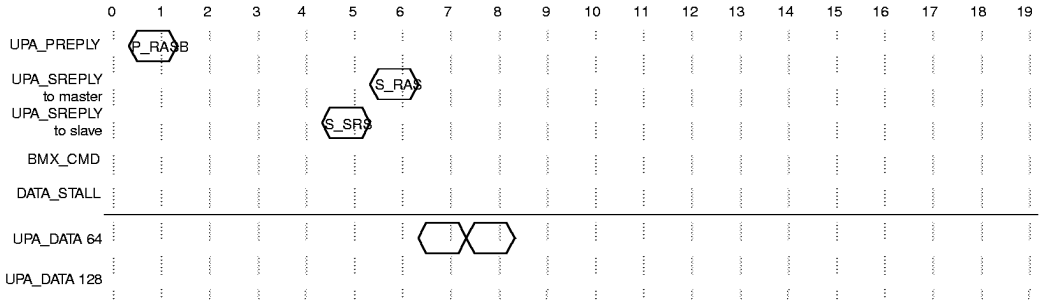


Figure 12. Best-Case Timing for Non-Cached Single Read, UPA64 -> UPA64

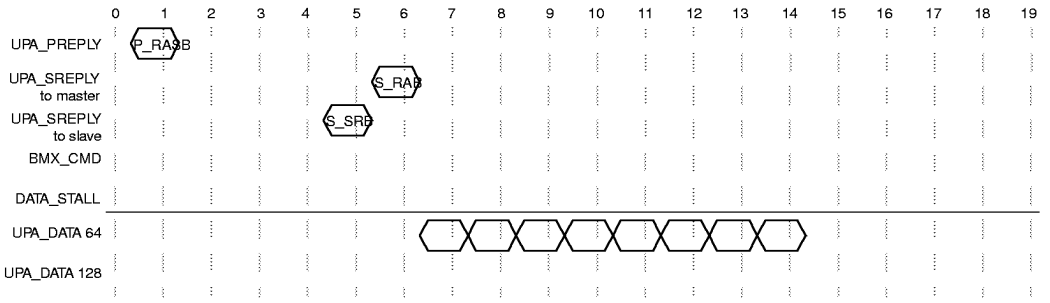


Figure 13. Best-Case Timing for Noncached Block Read, UPA64 -> UPA64

Figure 14 and *Figure 15* show the best-case timing for a U2S non-cacheable single and block write to FFB.

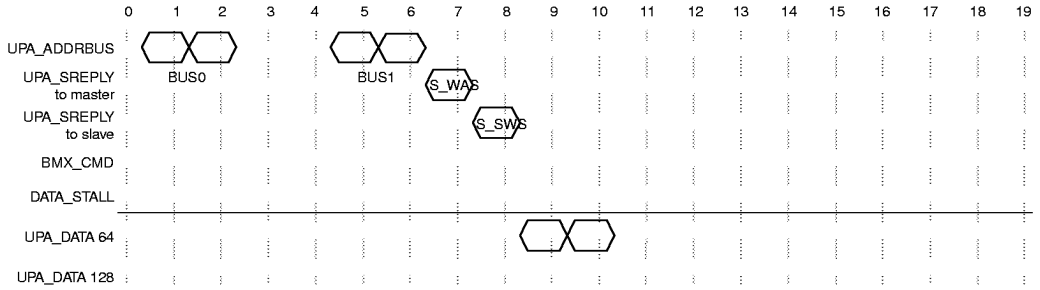


Figure 14. Best-Case Timing for Noncached Single Write, UPA64 -> UPA64

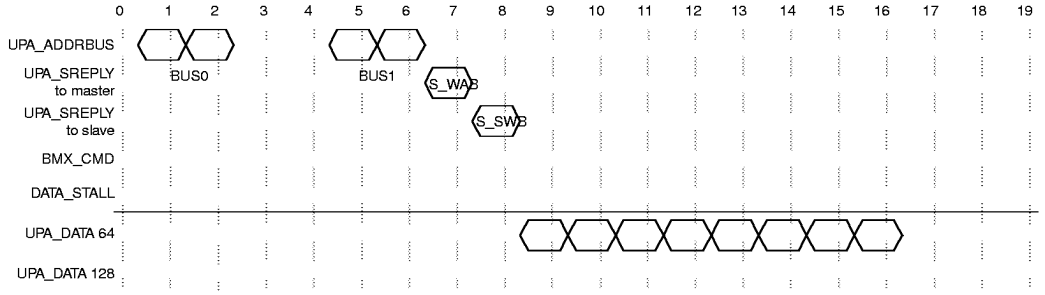


Figure 15. Best-Case Timing for Noncached Block Write, UPA64 -> UPA64

Figure 16 and *Figure 17* show the nominal timing for a U2S non-cacheable single and block read from the processor.

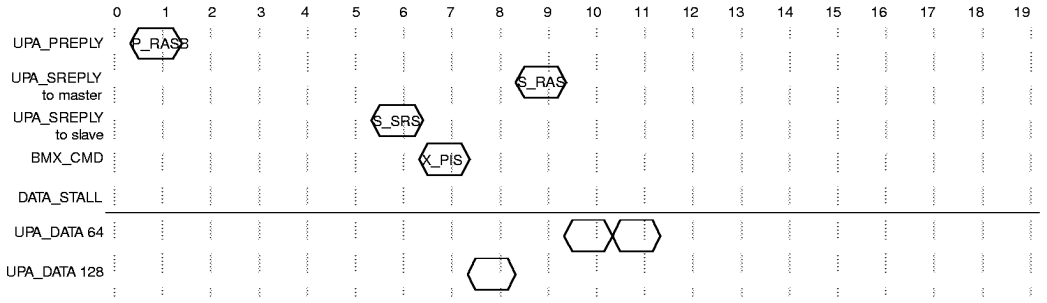


Figure 16. Best-Case Timing for Noncached Single Read, UPA128 -> UPA64

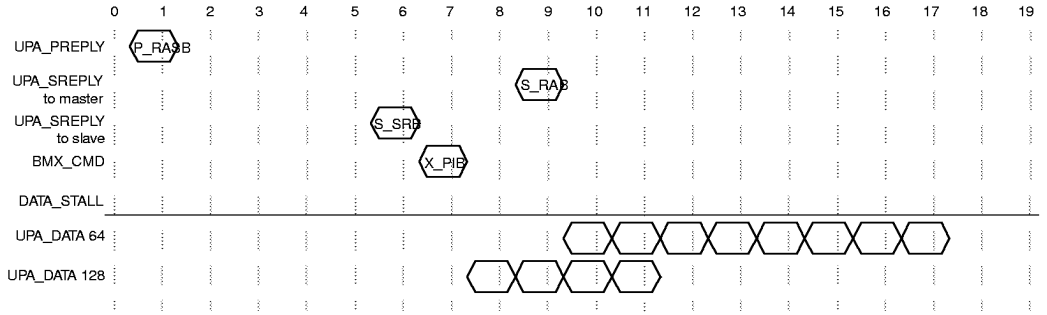


Figure 17. Best-Case Timing for Noncached Block Read, UPA128 -> UPA64

Note: *Timing diagrams for U2S non-cacheable single and block write to the processor are not shown because such transactions are dropped by the USC.*

Figure 18 shows the "fast path" timing for memory reads issued from the processor. Fast paths are characterized by row address valid one cycle earlier than that of normal paths. The fast path is only available for reads issued from the processor's master class 0. It is not available for writes or for any accesses from the U2S. Normal paths are used for all transactions that are not processor reads from memory, for example, DMA, memory writes, etc. See *Figure 22* and *Figure 23* for a graphic representation of fast paths and normal paths. Fast path is not implemented for processor writes because for processor transaction type P_WRI_REQ (described in the UPA specification) we need to examine the IVA bit (state bit embedded in the transaction packet, as described in the UPA specification) before launching the request to memory, and the IVA bit is in the second half of the PRequest packet. P_WRB_REQ (described in the UPA specification) almost always follows a victimizing read, and this can be overlapped with the read. Accesses from the U2S are less latency sensitive. Since the fast path is very timing critical and adds additional complexity to the logic, it is not implemented for the U2S.

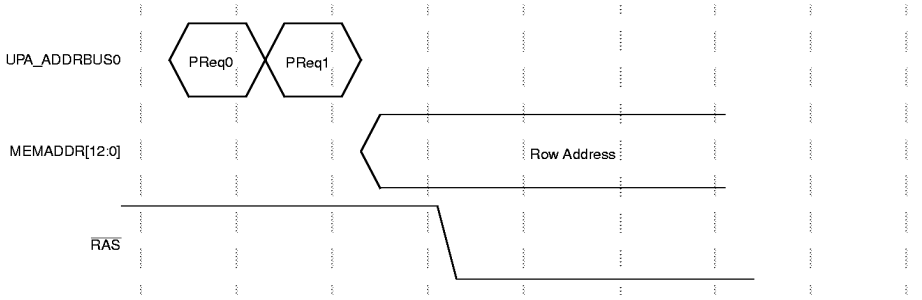


Figure 18. Best-Case PRequest-to-Memory Request Timing, Read (Fast Path)

Figure 19 shows a read or write issued through the "normal path."

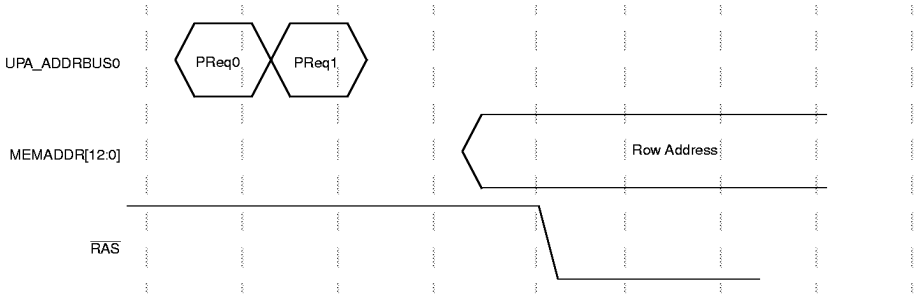


Figure 19. Best-Case PRequest-to-Memory Request Timing (Normal Path)

Basic Memory Timing

The memory controller (MC) timing is programmable so that memory timing can be optimized for different frequencies. Memory refresh and access timing have been divided into a number of segments. Memory Control and Status Register 1 (MCSR1) contains seven fields which allow custom tailoring of any particular segment: WPC1, RCD, PC0, CP, PC1, RP, and $\overline{RAS}$. For a detailed description of these fields, see the programming model described in the USC User Manual.

The timing diagram in *Figure 20* shows a generic template for a read or write transaction, how it is broken down into segments, and the corresponding fields in MCSR1 which control the width of each segment. Each individual segment is programmable by the firmware to optimize memory timing. See Figure 24 through Figure 28 for default memory timings.

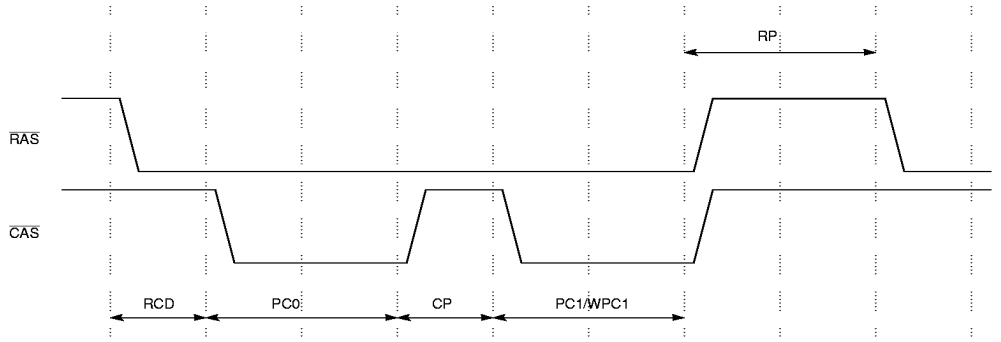


Figure 20. Basic Read/Write Timing

1. RCD is the $\overline{RAS}$-to-$\overline{CAS}$ delay.
2. PC0 is the page cycle 0 time.
3. CP is the $\overline{CAS}$-precharge time.
4. PC1 is the page cycle 1 time for a read operation.
5. WPC1 is the page cycle 1 time for a write operation.
6. RP is the $\overline{RAS}$-precharge time.

Note: *Reads use RCD, PC0, CP, PC1, and RP. Writes only use RCD, CP, WPC1, and RP; PC0 is fixed.*

Figure 21 shows a generic template for a refresh operation.

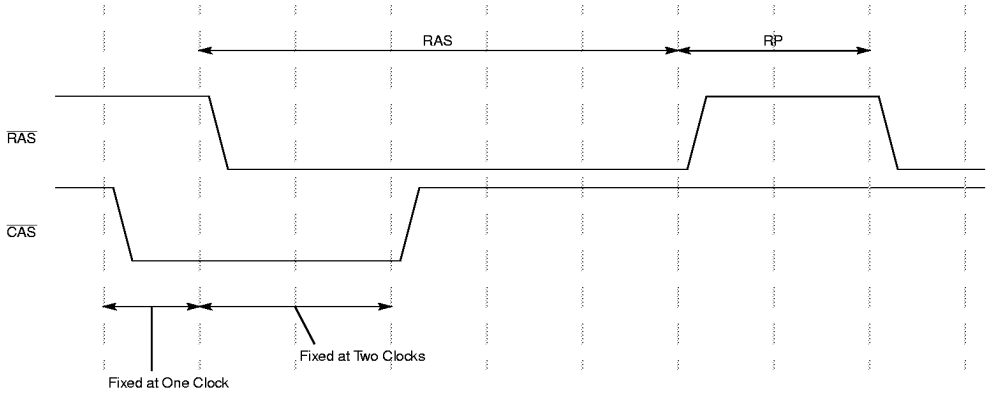


Figure 21. Basic Refresh Timing

1. $\overline{\text{RAS}}$ is the minimum $\overline{\text{RAS}}$ timing.
2. RP is the $\overline{\text{RAS}}$-precharge timing.

UPA-to-Memory Timing

Figure 22 and *Figure 23* show the minimum time for a UPA memory request packet issued on the UPA address bus pins to traverse the USC and appear on the USC's memory outputs, assuming that the USC is idle.

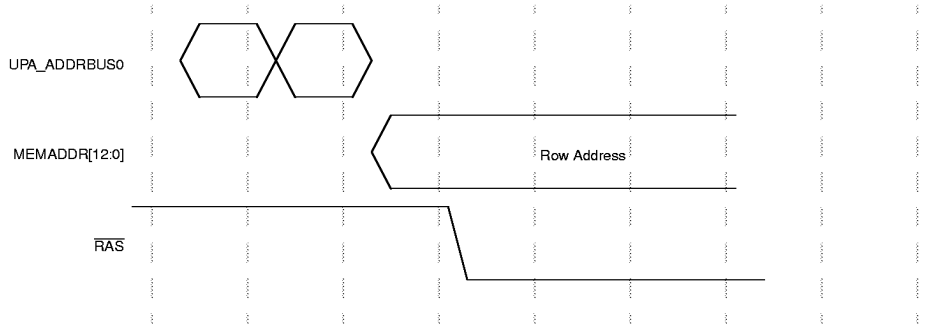


Figure 22. Best-Case UPA-to-Memory Timing (Fast Path)

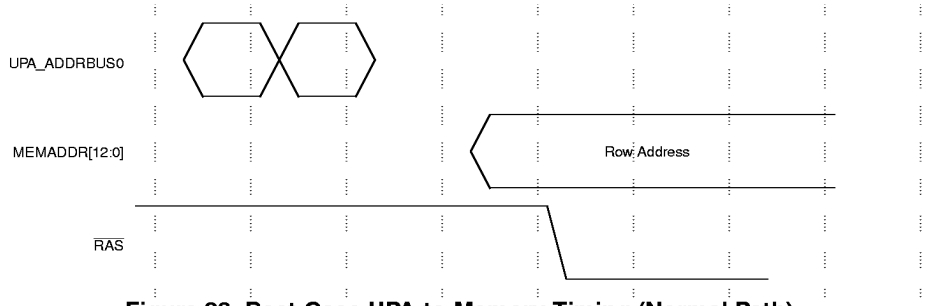


Figure 23. Best-Case UPA-to-Memory Timing (Normal Path)

Note: *Fast path timing is only applicable for memory reads issued from the processor. All other memory accesses use the normal path.*

Default Memory Timing

Figure 24 through *Figure 28* show the default timing after power on. These are the slowest, most conservative timings possible and are guaranteed to work at any frequency.

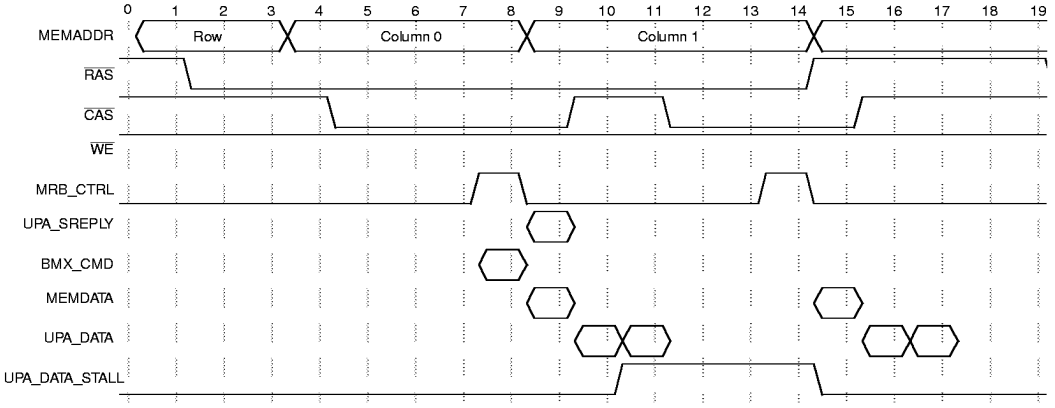


Figure 24. Default Memory CPU Read Timing

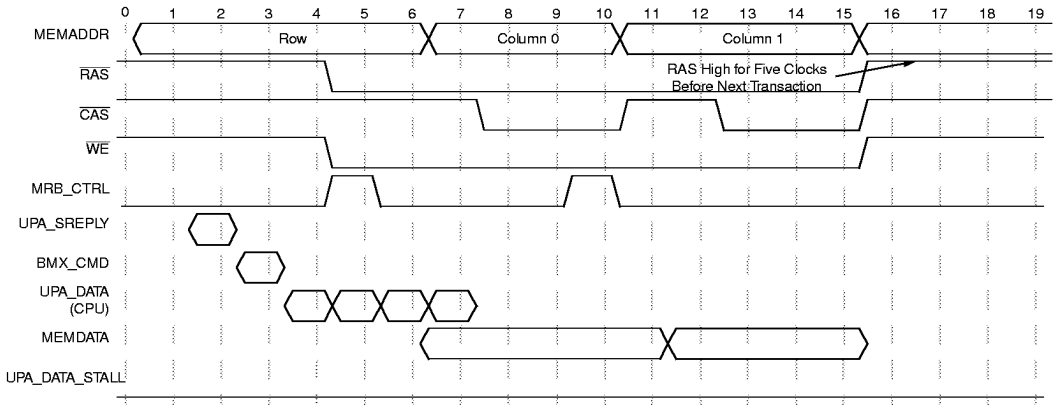


Figure 25. Default Memory CPU Write Timing

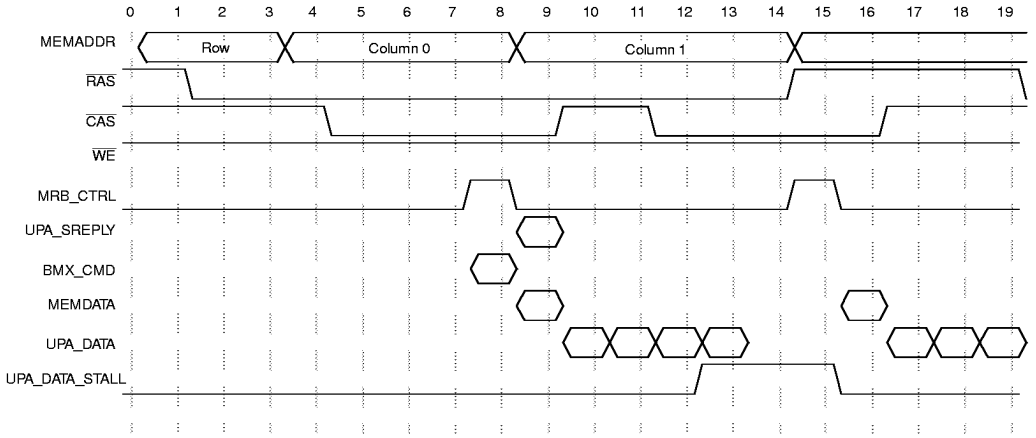


Figure 26. Default Memory U2S Read Timing

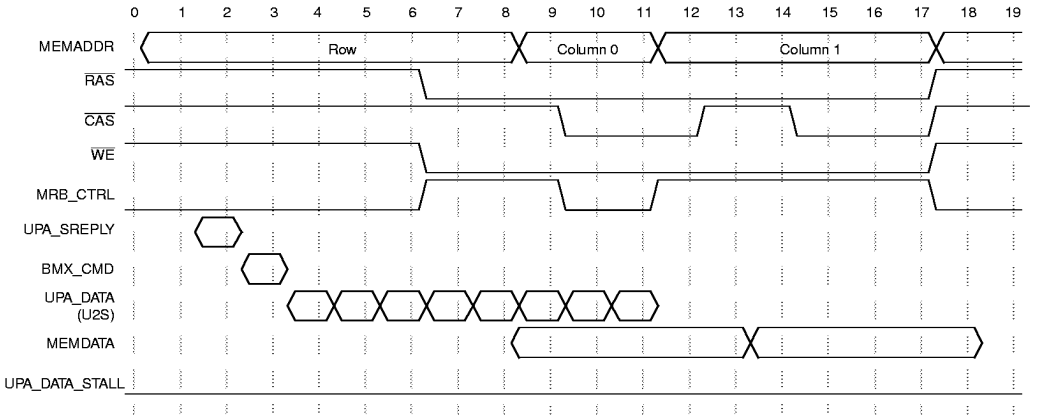


Figure 27. Default Memory U2S Write Timing

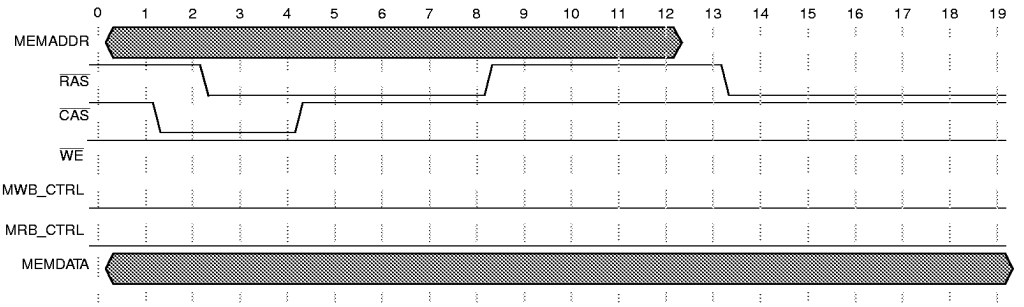


Figure 28. Default Refresh Timing

83.3 MHz (12 ns) Timings

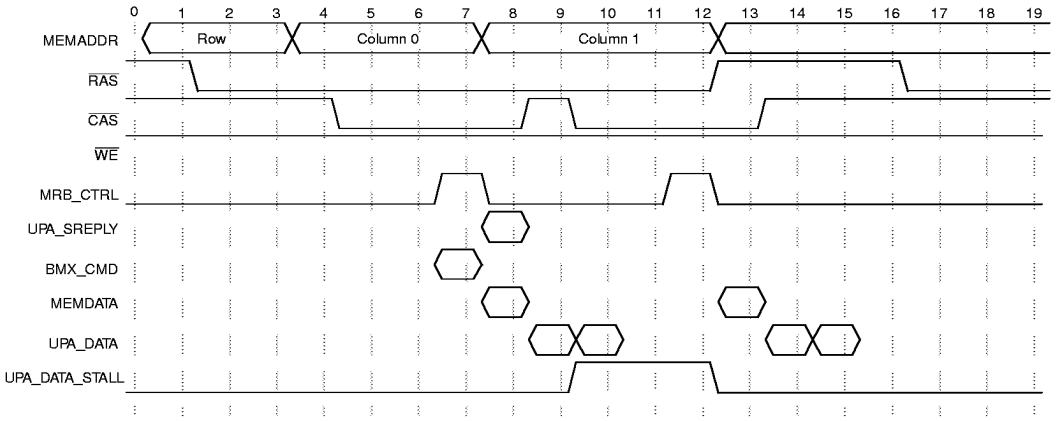


Figure 29. 83.3 MHz CPU Read Timing

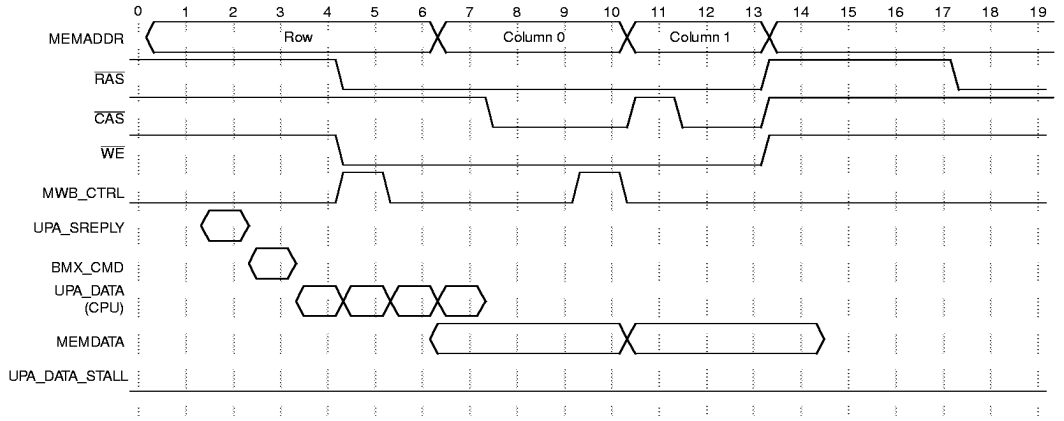


Figure 30. 83.3 MHz CPU Write Timing

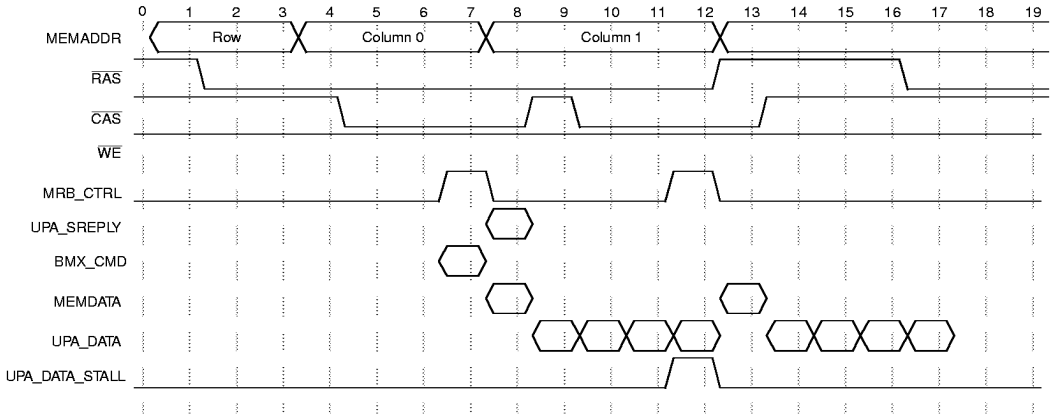


Figure 31. 83.3 MHz U2S Read Timing

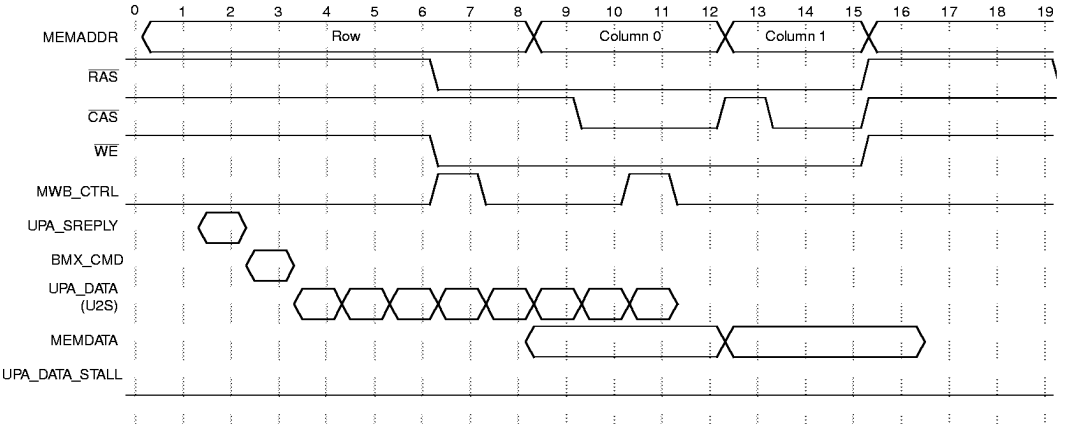


Figure 32. 83.3 MHz U2S Write Timing

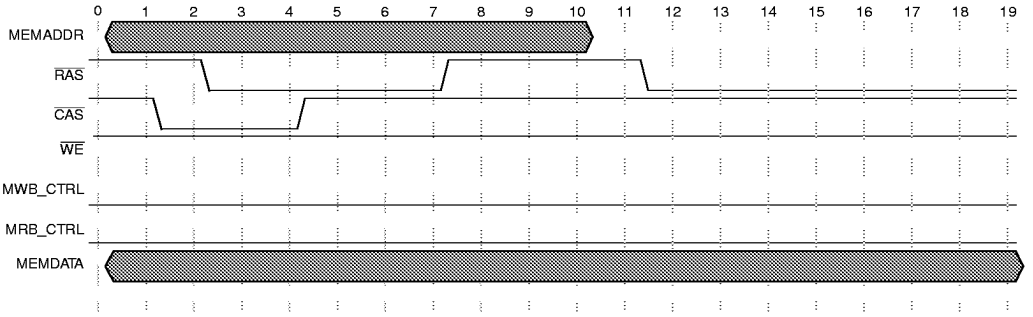


Figure 33. 83.3 MHz Refresh Timing

71.4 MHz (14 nanoseconds) Timings

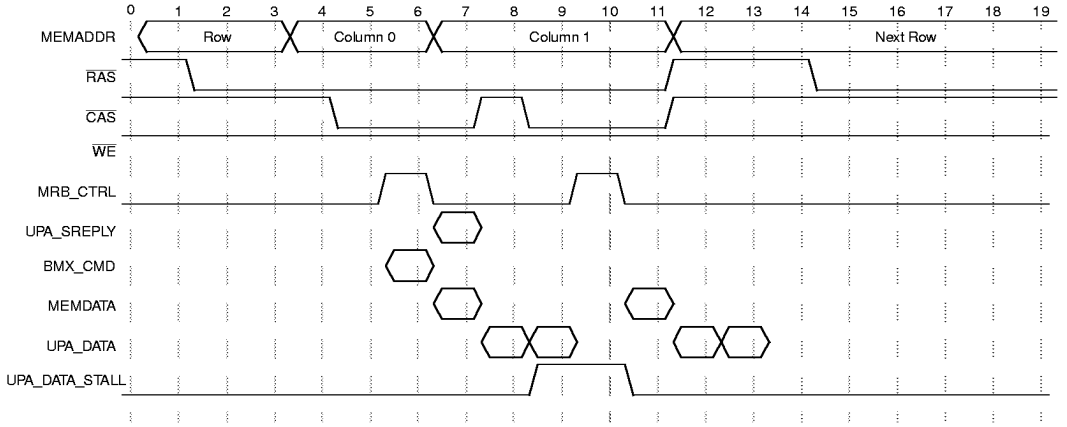


Figure 34. 71.4 MHz CPU Read Timing

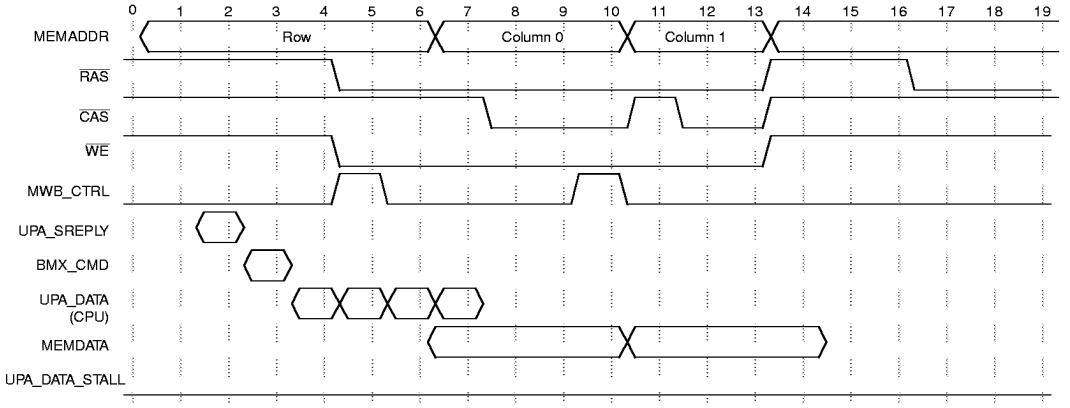


Figure 35. 71.4 MHz CPU Write Timing

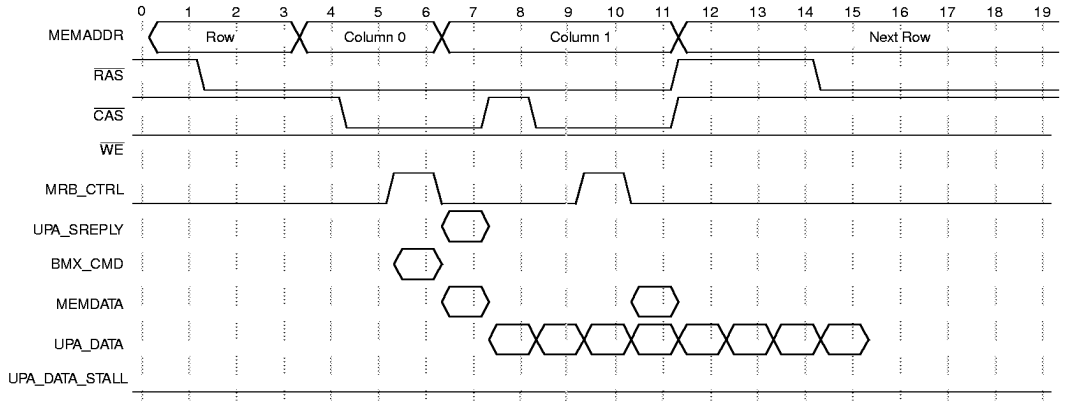


Figure 36. 71.4 MHz U2S Read Timing

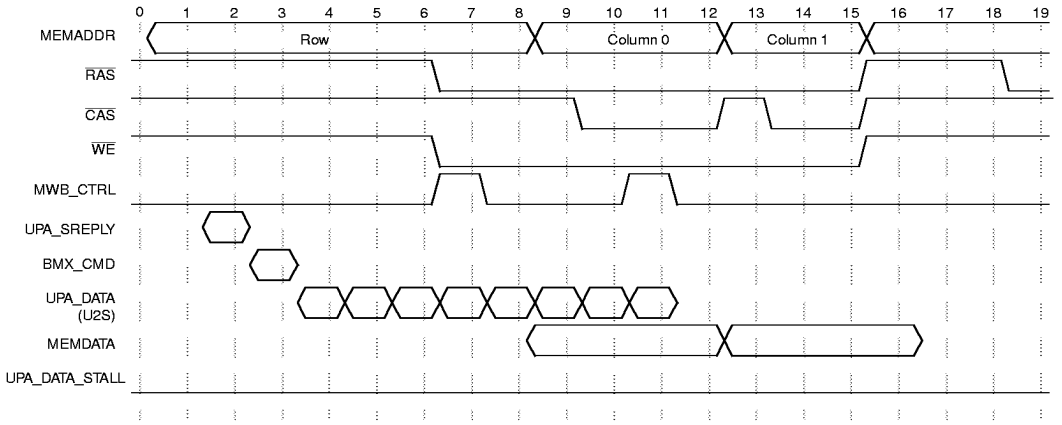


Figure 37. 71.4 MHz U2S Write Timing

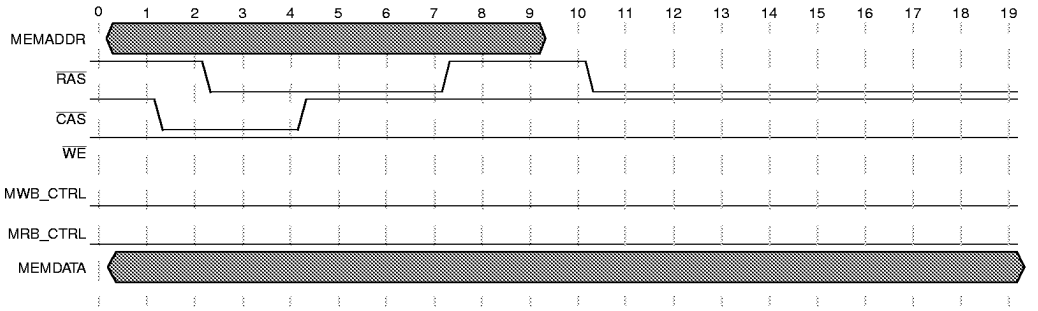


Figure 38. 71.4 MHz Refresh Timing

Minimum Timings

Figure 39 through *Figure 43* show the absolute minimum timing that the memory controller is capable of generating.

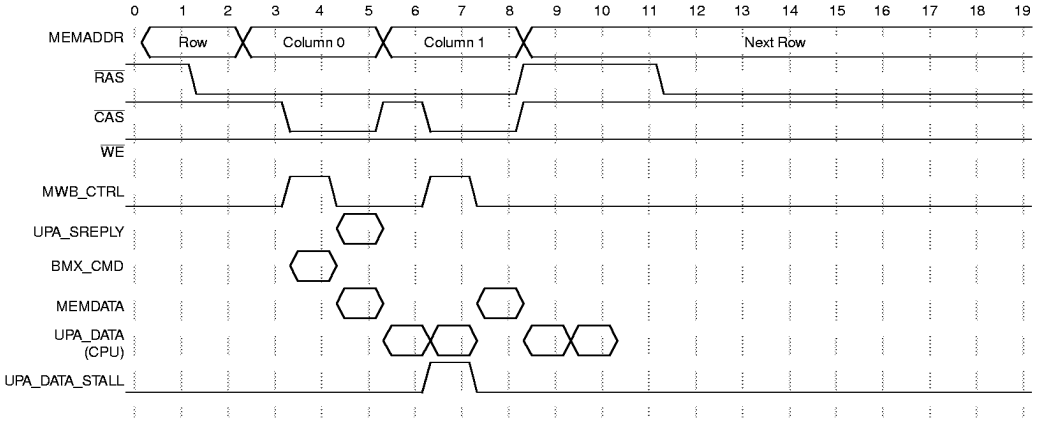


Figure 39. Minimum CPU Read Timing

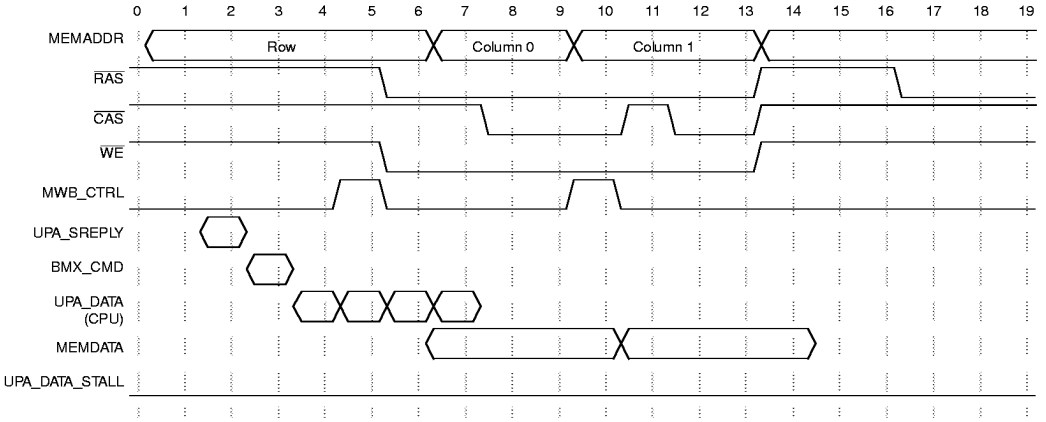


Figure 40. Minimum CPU Write Timing

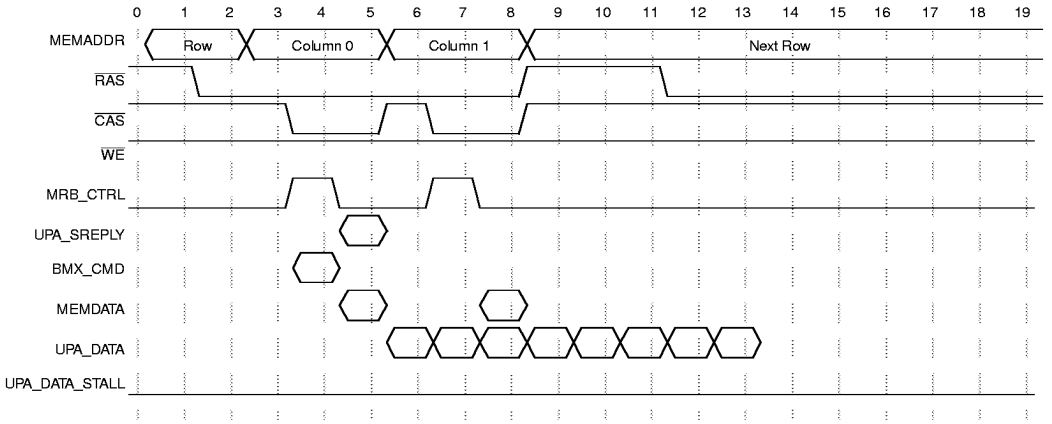


Figure 41. Minimum U2S Read Timing

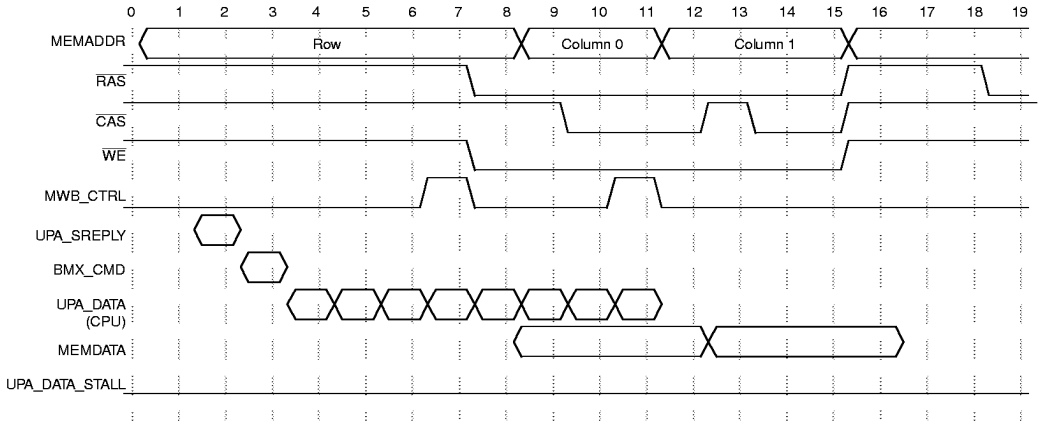


Figure 42. Minimum U2S Write Timing

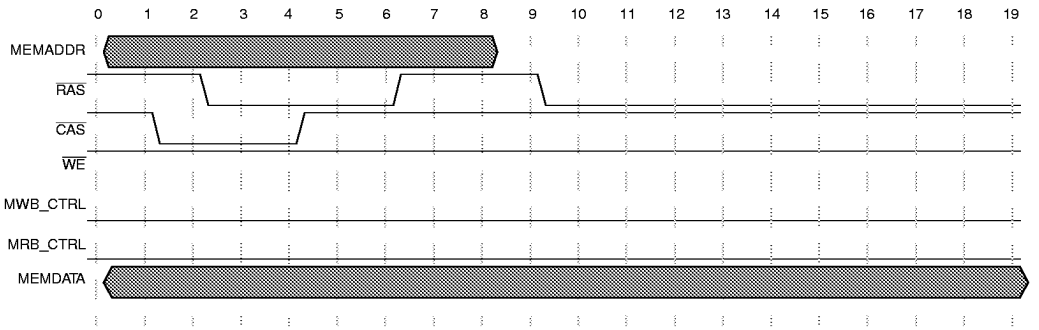


Figure 43. Minimum Refresh Timing

EBus Timing

Figure 44 and *Figure 45* show external timing for EBus accesses.

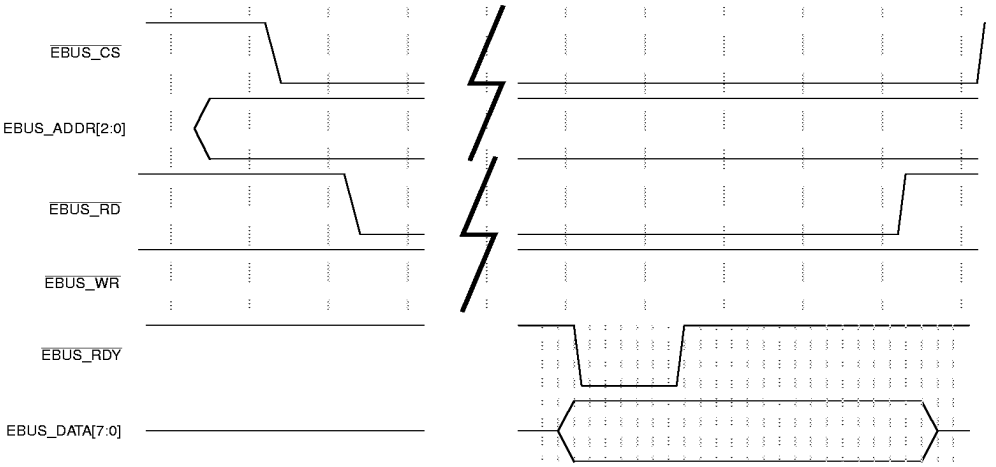


Figure 44. External EBus Read Timing

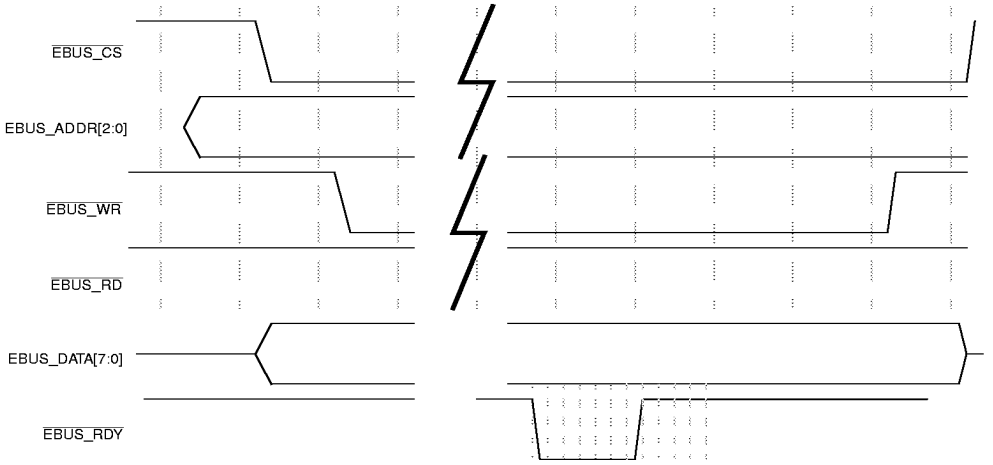


Figure 45. External EBus Write Timing

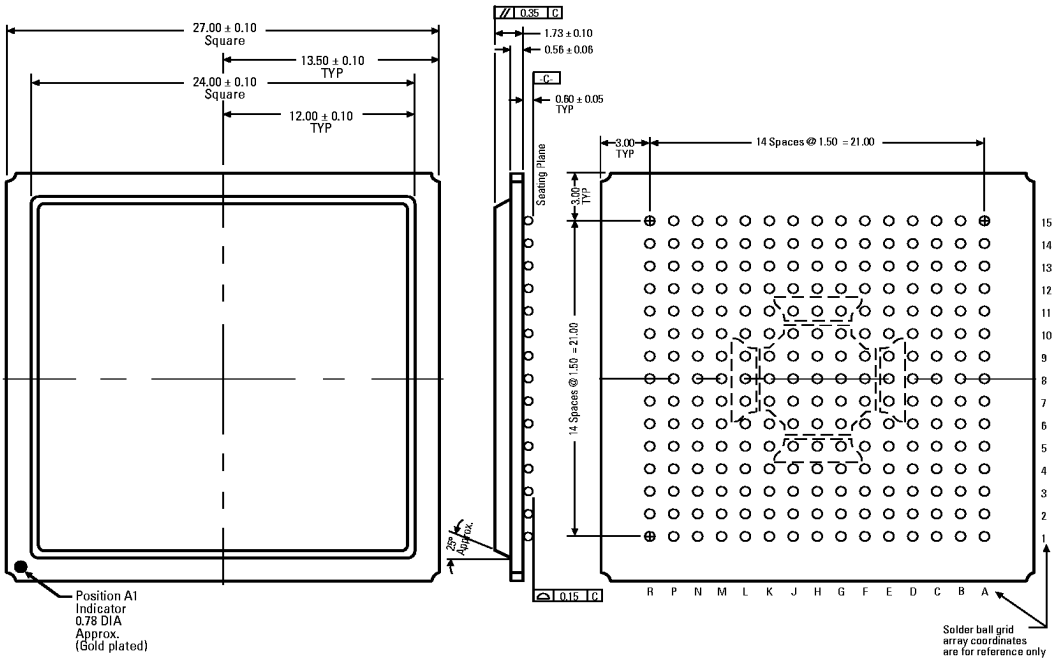
PACKAGE INFORMATION

225-Pin Plastic Ball Grid Array (ABGA) Pin Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	V_{SS}	D1	V_{DD}	G1	V_{SS}	K1	DEBUG_2 [1]	N1	MEMADDR_5
A2	UPA_PREPLY1_1	D2	BMX_CMD0_2	G2	$\overline{WE}$	K2	MEMADDR_12	N2	MEMADDR_7
A3	$\overline{JTAG\_TRST}$	D3	UPA_SREPLY0_0	G3	BMX_CMD1_0	K3	DEBUG_1 [1]	N3	MEMADDR_1
A4	V_{DD}	D4	UPA_PREPLY1_4	G4	$\overline{CAS2}$	K4	MEMADDR_10	N4	DEBUG_3 [1]
A5	JTAG_TDI	D5	UPA_PREPLY1_0	G5	V_{DD}	K5	MEMADDR_4	N5	UPA_ADDRBUS0_31
A6	$\overline{X\_RESET}$	D6	PLL_BYPASS	G6	V_{SS}	K6	UPA_ADR0_PAR0	N6	UPA_ADDRBUS0_24
A7	V_{SS}	D7	CLK+	G7	V_{SS}	K7	V_{SS}	N7	UPA_ADDRBUS0_21
A8	PLL_VDD	D8	UPA_ECC_VAL_0	G8	V_{SS}	K8	V_{SS}	N8	UPA_ADDRBUS0_18
A9	V_{DD}	D9	UPA_SREPLY1_1	G9	V_{SS}	K9	V_{SS}	N9	UPA_ADDRBUS0_17
A10	UPA_SREPLY1_2	D10	$\overline{EBUS\_RDY}$	G10	V_{SS}	K10	UPA_ADDRBUS0_00	N10	UPA_ADDRBUS0_10
A11	UPA_SREPLY1_0	D11	EBUS_DATA_4	G11	V_{DD}	K11	UPA_ADDRBUS1_27	N11	UPA_ADDRBUS0_06
A12	V_{SS}	D12	EBUS_ADDR_0	G12	UPA_ADDRBUS1_05	K12	UPA_ADDRBUS1_19	N12	UPA_ADDRBUS0_05
A13	$\overline{EBUS\_RD}$	D13	UPA_ADDR1_VAL1	G13	UPA_ADDRBUS1_09	K13	UPA_ADDRBUS1_21	N13	UPA_REQIN0_1
A14	EBUS_DATA_6	D14	5V_REF	G14	UPA_ADDRBUS1_07	K14	UPA_ADDRBUS1_16	N14	UPA_ADDRBUS1_26
A15	V_{DD}	D15	V_{SS}	G15	V_{DD}	K15	UPA_ADDRBUS1_14	N15	UPA_ADDRBUS1_23
B1	UPA_SREPLY0_1	E1	BMX_CMD0_1	H1	$\overline{CAS0}$	L1	MEMADDR_11	P1	MEMADDR_2
B2	UPA_SREPLY0_4	E2	$\overline{BMX\_CMD1\_1}$	H2	$\overline{RAS3}$	L2	MEMADDR_9	P2	UPA_PREPLY0_4
B3	UPA_SREPLY0_3	E3	BMX_CMD0_3	H3	$\overline{CAS1}$	L3	MEMADDR_6	P3	UPA_PREPLY0_3
B4	JTAG_TMS	E4	$\overline{MRB\_CTRL0}$	H4	DEBUG_0 [1]	L4	MEMADDR_0	P4	UPA_ADDRBUS0_34
B5	JTAG_TDO	E5	$\overline{UPA\_PREPLY1\_3}$	H5	V_{DD}	L5	UPA_PREPLY0_2	P5	UPA_ADDRBUS0_29
B6	UPA_DATA_STALL1	E6	$\overline{P\_RESET}$	H6	V_{SS}	L6	UPA_ADDRBUS0_33	P6	UPA_ADDRBUS0_28
B7	PLL_VSS	E7	V_{DD}	H7	V_{SS}	L7	V_{DD}	P7	UPA_ADDRBUS0_23
B8	UPA_DATA_STALL0	E8	V_{DD}	H8	V_{SS}	L8	V_{DD}	P8	UPA_ADDRBUS0_20
B9	UPA_SREPLY1_4	E9	V_{DD}	H9	V_{SS}	L9	V_{DD}	P9	UPA_ADDRBUS0_15
B10	$\overline{UPA\_RESET\_1}$	E10	$\overline{EBUS\_CS}$	H10	V_{SS}	L10	UPA_ADDRBUS0_04	P10	UPA_ADDRBUS0_13
B11	$\overline{EBUS\_WR}$	E11	$\overline{EBUS\_ADDR\_1}$	H11	V_{DD}	L11	UPA_ADDR0_VAL0_0	P11	UPA_ADDRBUS0_09
B12	$\overline{UPA\_RESET\_0}$	E12	UPA_SREPLY2_1	H12	UPA_ADDRBUS1_13	L12	UPA_ADDRBUS1_22	P12	UPA_ADDRBUS0_07
B13	EBUS_DATA_1	E13	$\overline{UPA\_PREPLY2\_1}$	H13	UPA_ADDRBUS1_12	L13	UPA_ADDRBUS1_24	P13	UPA_ADDRBUS0_01
B14	EBUS_DATA_3	E14	$\overline{UPA\_ADDRBUS1\_00}$	H14	UPA_ADDRBUS1_08	L14	UPA_ADDRBUS1_20	P14	UPA_REQIN0_0
B15	EBUS_DATA_0	E15	$\overline{UPA\_ADDRBUS1\_02}$	H15	UPA_ADDRBUS1_10	L15	UPA_ADDRBUS1_18	P15	UPA_SC_REQ0
C1	BMX_CMD1_3	F1	BMX_CMD0_0	J1	V_{DD}	M1	V_{SS}	R1	V_{DD}
C2	MWB_CTRL0	F2	$\overline{CAS3}$	J2	$\overline{RAS1}$	M2	MEMADDR_8	R2	UPA_PREPLY0_1
C3	MRB_CTRL1	F3	BMX_CMD1_2	J3	$\overline{RAS2}$	M3	MEMADDR_3	R3	UPA_ADDRBUS0_32
C4	UPA_PREPLY1_2	F4	MWB_CTRL1	J4	$\overline{RAS0}$	M4	NC	R4	V_{SS}
C5	JTAG_TCK	F5	UPA_SREPLY0_2	J5	V_{DD}	M5	UPA_PREPLY0_0	R5	UPA_ADDRBUS0_27
C6	$\overline{UPA\_XIR}$	F6	$\overline{PM\_OUT}$	J6	V_{SS}	M6	UPA_ADDRBUS0_30	R6	UPA_ADDRBUS0_25
C7	$\overline{SYS\_RESET}$	F7	V_{SS}	J7	V_{SS}	M7	UPA_ADDRBUS0_26	R7	V_{DD}
C8	$\overline{CLK-}$	F8	V_{SS}	J8	V_{SS}	M8	UPA_ADDRBUS0_22	R8	UPA_ADDRBUS0_19
C9	UPA_ECC_VAL_1	F9	V_{SS}	J9	V_{SS}	M9	UPA_ADDRBUS0_14	R9	V_{SS}
C10	UPA_SREPLY1_3	F10	EBUS_DATA_2	J10	V_{SS}	M10	UPA_ADDRBUS0_12	R10	UPA_ADDRBUS0_16
C11	EBUS_DATA_5	F11	UPA_SREPLY2_2	J11	V_{DD}	M11	UPA_ADDRBUS0_03	R11	UPA_ADDRBUS0_11
C12	EBUS_DATA_7	F12	UPA_ADDRBUS1_01	J12	UPA_ADDRBUS1_15	M12	UPA_ADDR0_VAL0_1	R12	V_{DD}
C13	EBUS_ADDR_2	F13	UPA_ADDRBUS1_06	J13	UPA_ADDRBUS1_17	M13	UPA_ADDRBUS1_28	R13	UPA_ADDRBUS0_08
C14	UPA_SREPLY2_0	F14	UPA_ADDRBUS1_03	J14	UPA_ADDRBUS1_11	M14	UPA_ADDRBUS1_25	R14	UPA_ADDRBUS0_02
C15	UPA_PREPLY2_0	F15	UPA_ADDRBUS1_04	J15	V_{SS}	M15	V_{DD}	R15	V_{SS}

1. DEBUG pins are used for internal debug only and are not used in a system implementation.

225-Pin Plastic ABGA Package Dimensions



Notes:

1. Drawing is not to scale.
2. Unless otherwise specified, all dimensions are in millimeters. Nonlimited dimensions other than size of raw material shall be held as follows when expressed:
   10^{-2} decimal places,
   $\pm$ 0.13 as angles,
   10^{-3} decimal places
3. It is imperative that measures be taken during assembly, handling, etc. to prevent the possibility of damage to devices by static electric discharge.
4. The flatness of the overmold surface in the center 10.16 mm DIA area, shall be within 0.076 mm.

ORDERING INFORMATION

Part Number	Speed	Description
STP2200ABGA-83	83 MHz	Uniprocessor System Controller
STP2200ABGA-100	100 MHz	Uniprocessor System Controller

Document Part Number: 802-7953-02