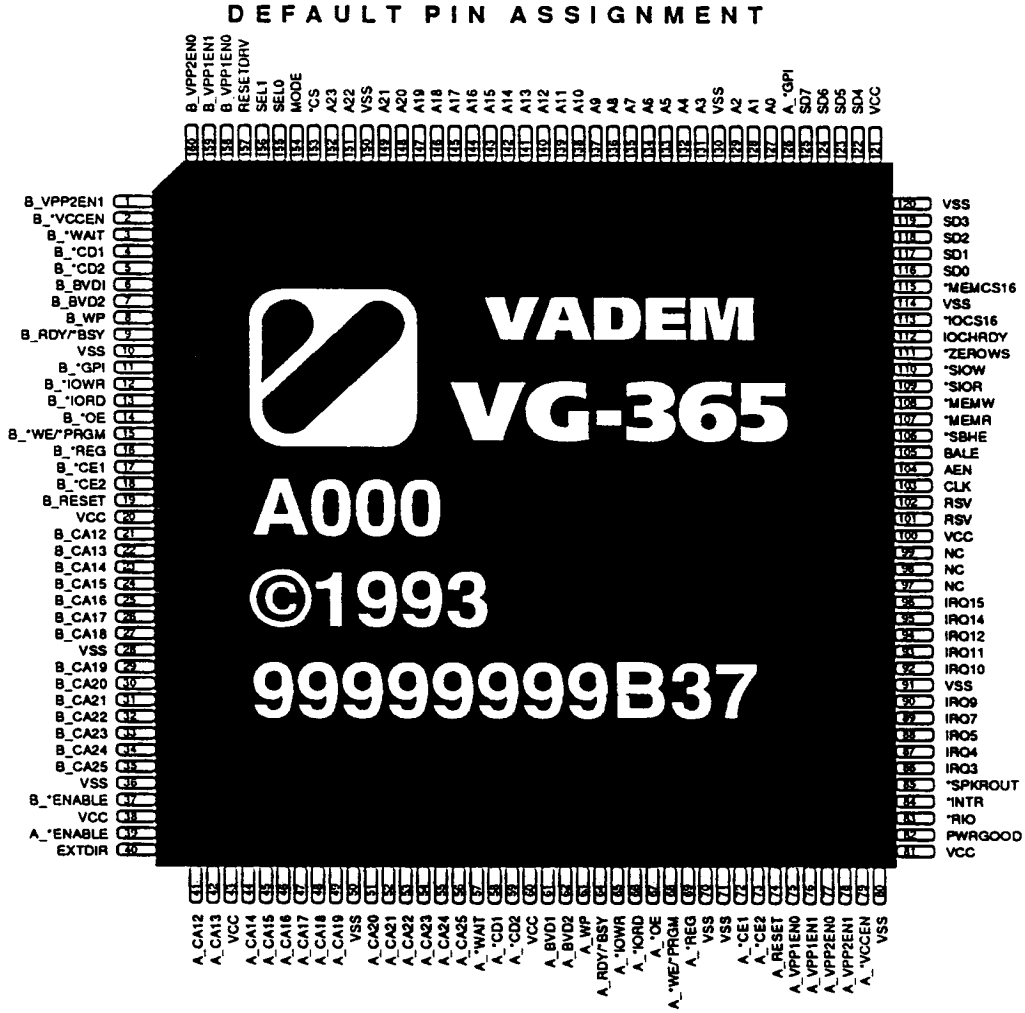
Pin Diagram

This section provides the pin assignment, signal description, block diagram, and pin descriptions for the VG-365 PC Card Socket Controller.

Pin Diagram
Figure 1-1



ALTERNATIVE PIN DEFINITIONS

PIN #	DEFAULT	ALTERNATIVE(S)
64,9	RDY/*BSY	*IREQ
62,7	BVD2	*SPKR
61,6	BVD1	*STSCHG, *RI
63,8	WP	*IOIS16
126,11	*GPI	*VPPVALID

Signal Description

Pin #	Signal Names	Type	Characteristics	# Pins
104	AEN	I	TTL Compatible	1
105	BALE	I	TTL Compatible	1
61, 6	BVD1 (*STSCHG/*RI)	I	Schmitt Trigger	2
62, 7	BVD2 (*SPKR)	I	Schmitt Trigger	2
56-51,49-44, 42-41,35-29, 27-21	CA[25:12]	O	8mA Tri-State	28
59,58,5,4	*CD[2:1]	I	Schmitt Trigger	4
73,72,18,17	*CE[2:1]	O	4mA Tri-State	4
103	CLK	I	TTL Compatible	1
153	*CS	I	TTL Compatible	1
39,37	*ENABLE	O	4mA Output	2
40	EXTDIR	O	4mA Output	1
10,28,36,50, 70,71,80,91, 114,120,130, 150	GND			12
126,11	*GPI	I	Schmitt Trigger with pull-up	2
84	*INTR	O	4mA Output	1
112	IOCHRDY	O	16 mA Tri-State	1
113	*IOCS16	O	16 mA 5V Open Drain	1
66,13	*IORD	O	4mA Tri-State	2
65,12	*IOWR	O	4mA Tri-State	2
96-92,90-86,	IRQs	O	8mA Tri-State	10
152,151, 149-145	LA[23:17]	I	TTL Compatible	7
115	*MEMCS16	O	16 mA 5V Open Drain	1
107	*MEMR	I	TTL Compatible	1
108	*MEMW	I	TTL Compatible	1
154	MODE	I	TTL Compatible	1
67,14	*OE	O	4mA Tri-State	2
82	PWRGOOD	I	Schmitt Trigger	1
64,9	RDY/*BSY (*IREQ)	I	Schmitt Trigger	2
69,16	*REG	O	4mA Tri-State	2
74,19	RESET	O	4mA Tri-State	2

Signal Description (cont.)

Pin #	Signal Names	Type	Characteristics	# Pins
157	RESETDRV	I	Schmitt Trigger with pull-down	1
83	*RIO	O	4mA Output	1
144-131, 129-127	SA[16:0]	I	TTL Compatible	17
106	*SBHE	I	TTL Compatible	1
156,155	SEL[1:0]	I	TTL Compatible	2
109	*SIOR	I	TTL Compatible	1
110	*SIOW	I	TTL Compatible	1
125-122, 119-116	SD[7:0]	I/O	I = TTL Compatible O = 8mA Tri-State	8
85	*SPKROUT	O	4mA Output	1
20,38,43,60 81,100,121	*VCC			7
79	*VCCEN	O	4mA Output	2
76,75,159, 158	VPP1EN[1:0]	O	4mA Output	4
78,77,1,160	VPP2EN[1:0]	O	4mA Output	4
57,3	*WAIT	I	TTL Compatible	2
68,15	*WE/*PRGM	O	4mA Tri-State	2
63,8	WP (*IOIS16)	I	TTL Compatible	2
111	*ZWS	O	16mA 5V Open Drain	1

Pin Descriptions

Symbol	Type	Pin No.	Description
AEN	I	104	System Address Enable. High during DMA cycles, low otherwise.
BALE	I	105	Bus Address Latch Enable. An active high input used to latch LA[23:17] at the beginning of a bus cycle.
BVD1 (*STSCHG/*RI)	I	61,6	If BVD1 is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost. For I/O PC Cards, this signal is held high when either or both the Signal on Change bit and Changed bit in the Card Status Register on the PC Card are set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. Or this pin is connected to Ring Indicate, which is qualified by Ring Indicate Enable to be passed on to the *RIO pin.
BVD2 (*SPKR)	I	62,7	BVD1 and BVD2 are generated by memory PC Cards with onboard batteries. These signals indicate the health of the battery. Both are asserted high when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery should be replaced, although data integrity on the memory PC Card is still assured. When the I/O interface is selected, BVD2 may be used to provide a single amplitude Digital Audio waveform intended to be passed through to the system's speaker without signal conditioning.
CA[25:12]	O	56-51, 49-44, 42,41, 35-29, 27-21	Card Address.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*CD[2:1]	I	59,58 5,4	Detects proper card insertion. The signals are connected to ground internally on the PC Card and will be forced low whenever a card is placed in a host socket. Status is available to software through the Interface Status Register.
*CE[2:1]	O	73,72 18,17	Active low card enable signals. *CE1 is used to enable even bytes, *CE2 for odd bytes. A multiplexing scheme based on A0, *CE1, *CE2 allows 8-bit hosts to access all data on Card Data[7:0] if desired.
CLK	I	103	System clock.
*CS	I	153	Chip Select. This active signal is driven from an external address decode logic if MODE=1. For an internal address decoding, MODE=0, and *CS should be driven to low. This input may be programmed to operate as a power down control signal, such that if *CS becomes inactive high, VG-365 will enter into power down mode for maximum power saving.
*ENABLE	O	39,37	Used to select PC Card Socket to activate. This signal controls the external address buffer logic. It will always be active low, unless the Output Enable bit is set to 0 in Power and RESETDRV control register.
EXTDIR	O	40	This signal is high during a read and low during a write. The default power up condition is low.
*GPI	I	126,11	General purpose inputs. May be used for one of several purposes. - An active low input indicates that Vpp power line has reached the user specified range. - An input indication a card eject or card insertion pending. - An input source for generating a card status change interrupt.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*INTR	O	84	Interrupt Request output: Active low output requesting a nonmaskable interrupt to the CPU.
IOCHRDY	O	112	I/O Channel Ready. This active high signal indicates that the current I/O bus cycle has completed. When a PC Card needs to extend a Read or Write cycle, the VG-365 pulls IOCHRDY low. IOCHRDY can be deasserted by either *WAIT, or by programming to add wait states for 16-bit memory and I/O cycles. If *WAIT is used in 16-bit mode, the wait state generator has to be set to 1 wait state.
*IOCS16	O	113	This active low I/O 16-bit chip select signal indicates to the host system the current I/O cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.
*IORD	O	66,13	I/O Read signal is driven active to read data from the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
*IOWR	O	65,12	I/O Write signal is driven active to write data to the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
IRQs	O	96-92, 90-86	IRQ[15, 14, 12:9, 7, 5:3].
LA[23:17]	I	152,151, 149-145	Local Address bus used to address memory devices on the ISA-bus. Together with the system address signals, they address up to 16MB on the ISA bus.
*MEMCS16	O	115	This active low 16-bit memory chip select signal indicates to the host system that the current memory cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*MEMR	I	107	Active low signal indicates a memory read cycle.
*MEMW	I	108	Active low signal indicates a memory write cycle.
MODE	I	154	Decode Mode. Used to determine if the port address chip select will be decoded internally (MODE-0), or with external logic (MODE=1).
*OE	O	67,14	Active low signal used to gate memory reads from memory cards.
PWRGOOD	I	82	Power Good is an active high signal which indicates that power to the system is stable. Connect to ground if not used. Combined with RESETDRV, it will indicate to VG-365 whether a cold reset, or a resume reset has occurred, to decide whether to reset the slot configuration registers. System implementations without a "POWERGOOD" as resume indication should tie this signal low.
RDY/*BSY (*IREQ)	I	64,9	Memory PC Cards drive Ready / *Busy low to indicate that the memory card circuits are busy processing a previous write command. It is set high when they are ready to accept a new data transfer command. For I/O PC Cards, this pin is used as an interrupt request and driven low to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested.
*REG	O	69,16	Select attribute memory. This signal is set inactive (high) for all accesses to common memory of a PC Card. When it is active, access is limited to Attribute Memory when *WE or *OE are active, and to I/O ports when *IORD or *IOWR are active. I/O PC Cards will not respond to *IORD or *IOWR when the *REG signal is inactive. During DMA operations the *REG signal is inactive.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
RESET	O	74,19	Provides a hard reset to a PC Card and clears the Card Configuration Option Register, thus placing card in an unconfigured (memory interface) state.
RESETDRV	I	157	Active high indicates a main system reset.
*RIO	0	83	Ring Indicate Output. Pass through of Ring Indicate output from I/O PC Card. VG-365 can also be configured to activate *RIO on card detect changes. *RIO will be functional in *CS controlled power down.
SA[16:0]	I	144-131, 129-127	System Address bus used to address memory and I/O devices on the ISA bus. These signals are latched and are valid throughout the bus cycle.
*SBHE	I	106	System Byte High Enable. When asserted, this active low signal indicates that a data transfer is occurring on the upper byte of the system data bus.
SD[7:0]	I/O	125-122, 119-116	System Data Bus.
SEL[1:0]	I	156,155	Strapping options that determine the VG-365 registers' base I/O address.
*SIOR	I	109	This active low I/O read signal instructs the VG-365 to drive data onto the data bus.
*SIOW	I	110	This active low I/O write signal instructs the VG-365 to latch the data on the data bus.
*SPKROUT	I/O	85	Digital audio signal which provides a single amplitude (digital) audio waveform to drive the system's speaker. Passes through *SPKR from an I/O PC Card. This signal must be held high when no audio signal is present.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*VCCEN	O	79,2	Power Control signal for card Vcc.
VPP1EN[1:0]	O	76,75, 159,158	Power Control signal for card Vpp1.
VPP2EN[1:0]	O	78,77, 1,160	Power Control signal for card Vpp2.
*WAIT	I	57,3	This signal is driven by the PC Card to delay completion of the memory or I/O cycle in progress.
*WE/*PRGM	O	68,15	The host uses *WE for gating memory write data, and for memory PC Cards that employ programmable memory.
WP (*IOIS16)	I	63,8	Reflects the status of the Write Protect switch on some memory PC Cards. If the memory PC Card has no write protect switch, the card will connect this line to ground (the card can always be written) or to Vcc (permanently write protected). When the I/O interface is selected, this pin is used for the "I/O is 16-bit Port" function: asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port which is addressed is capable of 16-bit access. If this signal is not asserted during a 16-bit I/O access, the system will generate 8-bit references to the even and odd byte of the 16-bit port being accessed. If 8-bit window size is selected, *IOIS16 is ignored.
*ZWS	O	111	Zero Wait State. An active low output indicates that the PC Card wishes to terminate the present bus cycle without inserting additional wait states. This cycle will not be driven during a 16-bit I/O access.