SONY

CXD4000R

Fingerprint Verification System LSI

Description

The CXD4000R is an IC that inputs the signal from a Sony fingerprint sensor and performs fingerprint verification.

This chip integrates a CPU, A/D converter, DRAM, USB controller and other circuits.

Features

- Combination with a Sony fingerprint sensor and a flash memory realizes a fingerprint verification system with a 3-chip configuration
- 16-bit microcomputer SPC970
- USB controller (conforms to Rev 1.1)

Fingerprint Verification Block

- Adoption of Sony's original verification algorithm also provides excellent results for blurred and deformed fingerprints
- False rejection ratio: 1% or less, false acceptance ratio: 0.1% or less (with 2 trials)
- Verification time per finger: approximately 40ms (Clock frequency: 48MHz, excluding fingerprint image loading time)

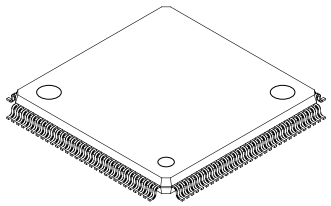
Microcomputer Block

- CPU: SPC970 series 16-bit CPU core
- Internal RAM: 4K bytes
- External flash memory: 16-bit, 2M bytes
- External expansion SRAM: 8-bit/16-bit, 2M bytes each
- General purpose register: 16 bits × 8 lines × 32 banks
- Processing rate: 41.6ns (f_{SYS}: 24MHz)
- Peripheral hardware
  - Serial interface × 1 channel (Clock synchronous serial interface or asynchronous serial interface)
  - 16-bit timer × 4 channels
  - External memory interface
  - 8-bit A/D converter (also used as sensor input)
  - 8-bit D/A converter × 1 channel
- General-purpose I/O: 12 (also used as interrupt inputs, etc.)

USB Controller

- Conforms to Rev 1.1
- USB transceiver circuit
- Supports full-speed (12Mbps)

120 pin LQFP (Plastic)



Applications

- Fingerprint verification units (stand-alone)
- Cellular phones
- Personal computers

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +4.6	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
• Input voltage	V_I	V_{SS} to V_{DD}	V
• Output voltage	V_O	V_{SS} to V_{DD}	V
• Operating temperature	Topr	0 to +70	°C

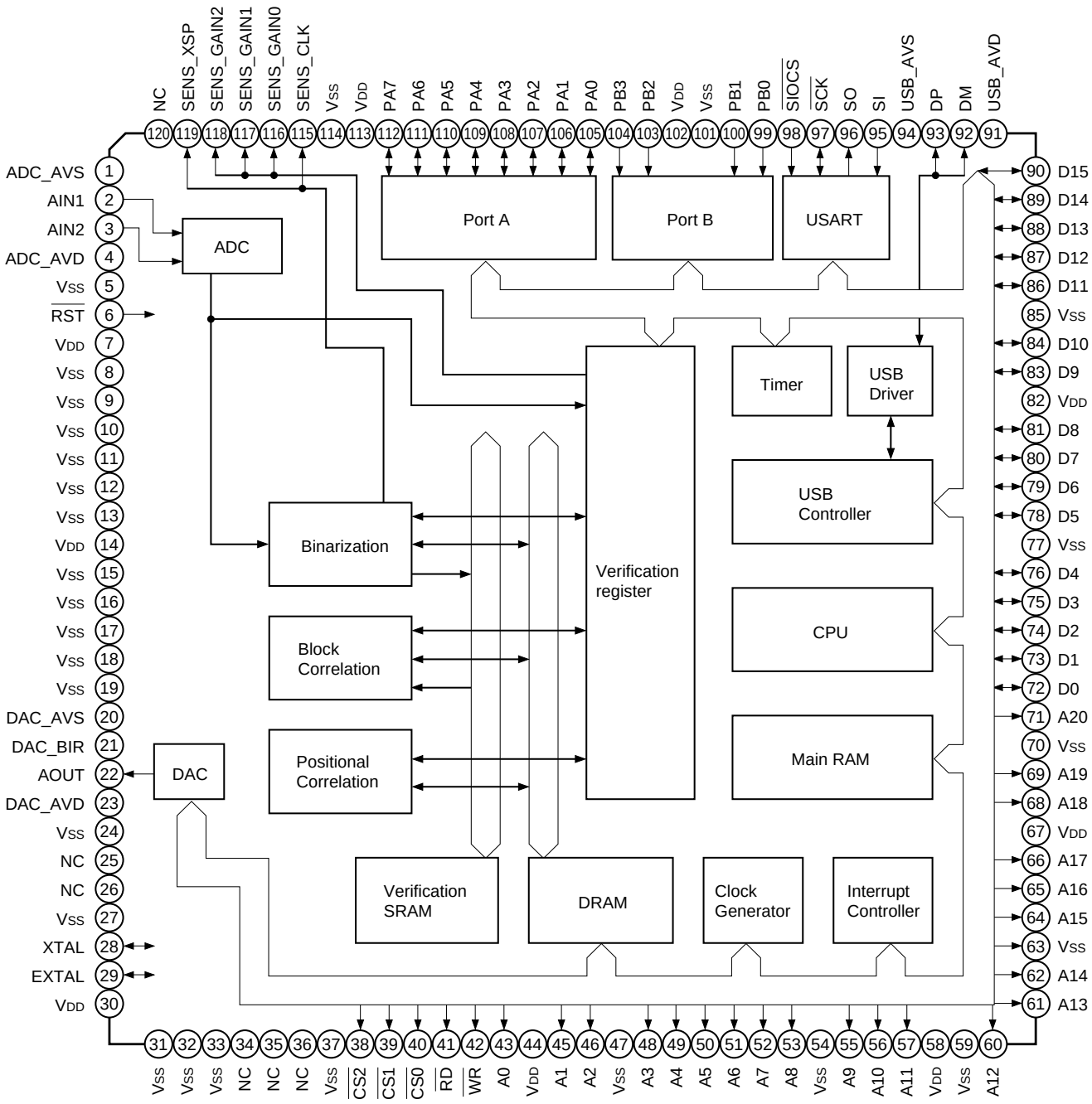
I/O Pin Capacitance

• Input pin capacitance	C_I	9 (max.)	pF
• Output pin capacitance	C_O	11 (max.)	pF
• I/O pin capacitance	$C_{I/O}$	11 (max.)	pF

Note) Measurement conditions: $V_{DD} = V_I = 0V$, f = 1MHz

E01664-PS

Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description	Remarks
1	ADC_AVS		A/D converter GND.	
2	AIN1	I	A/D converter analog input.	Sensor input
3	AIN2	I	A/D converter analog input.	
4	ADC_AVD		A/D converter power supply.	
5	V_{SS}		GND.	
6	$\overline{RST}$	I	Low level active system reset.	
7	V_{DD}		Power supply.	
8 to 13	V_{SS}		GND.	
14	V_{DD}		Power supply.	
15 to 19	V_{SS}		GND.	
20	DAC_AVS		D/A converter GND.	
21	DAC_BIR	I	Bias resistor connection for D/A converter output buffer (operational amplifier).	Pull-up with an external 33kΩ resistor
22	AOUT	O	D/A converter analog output.	
23	DAC_AVD		D/A converter power supply.	
24	V_{SS}		GND.	
25, 26	NC		No connected.	
27	V_{SS}		GND.	
28	XTAL	O	Oscillator connection for clock oscillation.	
29	EXTAL	I	Oscillator connection for clock oscillation.	
30	V_{DD}		Power supply.	
31 to 33	V_{SS}		GND.	
34 to 36	NC		No connected.	
37	V_{SS}		GND.	
38	$\overline{CS2}$	O	External expansion 16-bit SRAM chip select.	
39	$\overline{CS1}$	O	External expansion 8-bit SRAM chip select.	
40	$\overline{CS0}$	O	Flash memory chip select.	
41	$\overline{RD}$	O	External memory read strobe.	
42	$\overline{WR}$	O	External memory write strobe.	
43	A0	I/O	External memory address bus.	
44	V_{DD}		Power supply.	
45	A1	I/O	External memory address bus.	
46	A2	I/O	External memory address bus.	
47	V_{SS}		GND.	
48	A3	I/O	External memory address bus.	
49	A4	I/O	External memory address bus.	
50	A5	I/O	External memory address bus.	

Pin No.	Symbol	I/O	Description	Remarks
51	A6	I/O	External memory address bus.	
52	A7	I/O	External memory address bus.	
53	A8	I/O	External memory address bus.	
54	V_{SS}		GND.	
55	A9	I/O	External memory address bus.	
56	A10	I/O	External memory address bus.	
57	A11	I/O	External memory address bus.	
58	V_{DD}		Power supply.	
59	V_{SS}		GND.	
60	A12	I/O	External memory address bus.	
61	A13	I/O	External memory address bus.	
62	A14	I/O	External memory address bus.	
63	V_{SS}		GND.	
64	A15	I/O	External memory address bus.	
65	A16	I/O	External memory address bus.	
66	A17	I/O	External memory address bus.	
67	V_{DD}		Power supply.	
68	A18	I/O	External memory address bus.	
69	A19	I/O	External memory address bus.	
70	V_{SS}		GND.	
71	A20	I/O	External memory address bus.	
72	D0	I/O	External memory data bus.	Pulled-up internally
73	D1	I/O	External memory data bus.	Pulled-up internally
74	D2	I/O	External memory data bus.	Pulled-up internally
75	D3	I/O	External memory data bus.	Pulled-up internally
76	D4	I/O	External memory data bus.	Pulled-up internally
77	V_{SS}		GND.	
78	D5	I/O	External memory data bus.	Pulled-up internally
79	D6	I/O	External memory data bus.	Pulled-up internally
80	D7	I/O	External memory data bus.	Pulled-up internally
81	D8	I/O	External memory data bus.	Pulled-up internally
82	V_{DD}		Power supply.	
83	D9	I/O	External memory data bus.	Pulled-up internally
84	D10	I/O	External memory data bus.	Pulled-up internally
85	V_{SS}		GND.	
86	D11	I/O	External memory data bus.	Pulled-up internally
87	D12	I/O	External memory data bus.	Pulled-up internally

Pin No.	Symbol	I/O	Description	Remarks
88	D13	I/O	External memory data bus.	Pulled-up internally
89	D14	I/O	External memory data bus.	Pulled-up internally
90	D15	I/O	External memory data bus.	Pulled-up internally
91	USB_AVD		USB power supply.	
92	DM	I/O	USB D–	
93	DP	I/O	USB D+	
94	USB_AVS		USB GND.	
95	SI	I	Serial data input.	Pulled-up internally
96	SO	O	Serial data output.	Tri-state, pulled-up internally
97	$\overline{SCK}$	I/O	Serial clock I/O.	Pulled-up internally
98	$\overline{SIOCS}$	I	Serial chip select input.	Pulled-up internally
99	PB0	I	(Port B) Input port/external interrupt request input.	Pulled-up internally
100	PB1	I	(Port B) Input port/external interrupt request input.	Pulled-up internally
101	V_{SS}		GND.	
102	V_{DD}		Power supply.	
103	PB2	I	(Port B) Input port/external interrupt request input.	Pulled-up internally
104	PB3	I	(Port B) Input port/external interrupt request input.	Pulled-up internally
105	PA0	I/O	(Port A) I/O port.	Pulled-down internally
106	PA1	I/O	(Port A) I/O port.	Pulled-down internally
107	PA2	I/O	(Port A) I/O port.	Pulled-down internally
108	PA3	I/O	(Port A) I/O port.	Pulled-down internally
109	PA4	I/O	(Port A) I/O port.	Pulled-up internally
110	PA5	I/O	(Port A) I/O port.	Pulled-up internally
111	PA6	I/O	(Port A) I/O port.	Pulled-up internally
112	PA7	I/O	(Port A) I/O port/external 16-bit SRAM upper byte control.	Pulled-up internally
113	V_{DD}		Power supply.	
114	V_{SS}		GND.	
115	SENS_CLK	O	Sensor clock output.	
116	SENS_GAIN0	O	Sensor gain output.	
117	SENS_GAIN1	O	Sensor gain output.	
118	SENS_GAIN2	O	Sensor gain output.	
119	SENS_XSP	O	Sensor start pulse output.	
120	NC		No connected.	

Electrical Characteristics

DC Characteristics

(Within the recommended operating range)

Item		Symbol	Conditions	Min.	Max.	Unit	Applicable pins
Input voltage (1) (digital)	High level input voltage	V_{IH}		0.7V_{DD}		V	Inputs other than *3 and *4
	Low level input voltage	V_{IL}			0.2V_{DD}	V	
Input voltage (2) (USB interface)	Differential input sensitivity	Vdi		0.2	—	V	*3
	Differential common mode range	Vcm		0.8	2.5	V	
	Single-ended receiver high level input voltage	V_{IH}		2.0	V_{DD}	V	
	Single-ended receiver low level input voltage	V_{IL}		0	0.8	V	
Input voltage (3) (A/D input)	Analog input level	V_{IN}		0.1V_{DD}	0.9V_{DD}	V	*4
Output voltage (1) (digital)	High level output voltage	V_{OH1}	I_{OH} = –4mA	V_{DD} – 0.4	V_{DD}	V	*1
	Low level output voltage	V_{OL1}	I_{OL} = 4mA	0	0.4	V	
Output voltage (2) (digital)	High level output voltage	V_{OH2}	I_{OH} = –2mA	V_{DD} – 0.4	V_{DD}	V	*2
	Low level output voltage	V_{OL2}	I_{OL} = 2mA	0	0.4	V	
Output voltage (3) (USB interface)	Low level output voltage	V_{OL}	RL = 1.5kΩ to 3.6V	—	0.3	V	*3
	High level output voltage	V_{OH}	RL = 15kΩ to GND	2.8	3.6	V	
Output voltage (4) (D/A output)	Analog output level	V_{ON}		0	V_{DD}	V	*5

*1 A0 to A20, PA0 to PA7, $\overline{SCK}$, SO

*2 D0 to D15, SENS_CLK, SENS_GAIN0 to SENS_GAIN2, SENS_XSP, $\overline{CS0}$ to $\overline{CS2}$, $\overline{RD}$, $\overline{WR}$

*3 DP, DM

*4 AIN1, AIN2

*5 AOUT

AC Characteristics

(1) Oscillation Inverter I/O Characteristics

(Within the recommended operating range)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	LVth	EXTAL			$V_{DD}/2$		V
Input voltage	V_{IH}	EXTAL		$0.7V_{DD}$			V
	V_{IL}					$0.3V_{DD}$	V
Output voltage	V_{OH}	XTAL	Feed current where I_{OH} = –3.0mA	$V_{DD}/2$			V
	V_{OL}		Pull-in current where I_{OL} = 3.0mA			$V_{DD}/2$	V
Feedback resistor	RFB	EXTAL XTAL	$V_{IN} = V_{DD}$ or Vss	250k	1M	2.5M	Ω
Oscillation frequency	f_{EX}	EXTAL XTAL		20		48.12	MHz

Note) When using USB, the oscillation frequency should be 48MHz ± 0.25%.

(2) Frequency Division Clock Timing

(Within the recommended operating range)

Item	Symbol	Conditions	Min.	Max.	Unit
Microcomputer system clock period	t_{SYS}	Frequency division value 1/2 (clock frequency $\phi = f_{EX}/2$)	41.57	100	ns
		Frequency division value 1/4 (clock frequency $\phi = f_{EX}/4$)	83.13	200	ns
		Frequency division value 1/8 (clock frequency $\phi = f_{EX}/8$)	166.26	400	ns
		Frequency division value 1/16 (clock frequency $\phi = f_{EX}/16$)	332.51	800	ns
Verification engine clock period	t_{ENG}	Frequency division value 1/1 (clock frequency = f_{EX})	20.79	50	ns
		Frequency division value 1/2 (clock frequency = $f_{EX}/2$)	41.57	100	ns
		Frequency division value 1/4 (clock frequency = $f_{EX}/4$)	83.13	200	ns
		Frequency division value 1/8 (clock frequency = $f_{EX}/8$)	166.26	400	ns
		Frequency division value 1/16 (clock frequency = $f_{EX}/16$)	332.51	800	ns

(3) Reset Input

(Within the recommended operating range)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Reset input low level width	t_{RST}	$\overline{RST}$	Clock oscillation stabilized	$4/f_{EX}$ + 20	—	ns

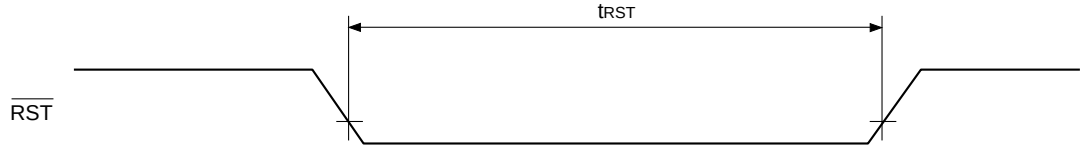


Fig. 1. Reset Input Timing

(4) Interrupt Input (Within the recommended operating range)

Item	Symbol	Pins	Conditions		Min.	Max.	Unit
External interrupt high and low level width	t_{IH} t_{IL}	PB0 to PB3	Noise filer not selected		20	—	ns
			Noise filter selected	CPU clock	tsys + 20	—	ns
				PS5	$32/f_{EX}$ + 20	—	ns
				PS7	$128/f_{EX}$ + 20	—	ns

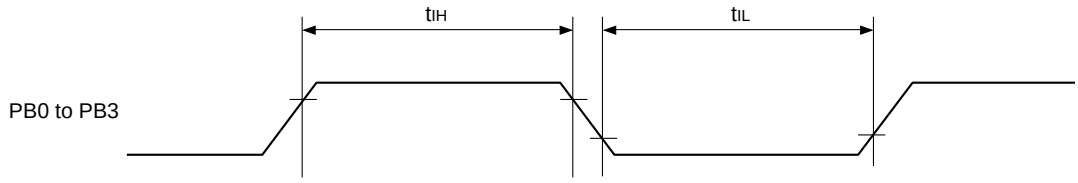


Fig. 2. Interrupt Input Timing

(5) A/D Converter Characteristics (Within the recommended operating range)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution				8		bits
Conversion rate	F_{CMAX}	V_{IN} = 0.1AVD to 0.9AVD, F_{IN} = 1kHz, ramp wave	0.5		12	MHz
Supply current	Iop	F_{IN} = 100kHz, sine wave	—	2.9	—	mA
Standby current	Istb	ADC standby	—	—	1	µA
Reference current	Iref		—	628	—	µA
Integral non-linearity error	El_{AD}	Endpoint method	—	0.7	—	LSB
Differential non-linearity error	Ed_{AD}		—	0.65	—	LSB

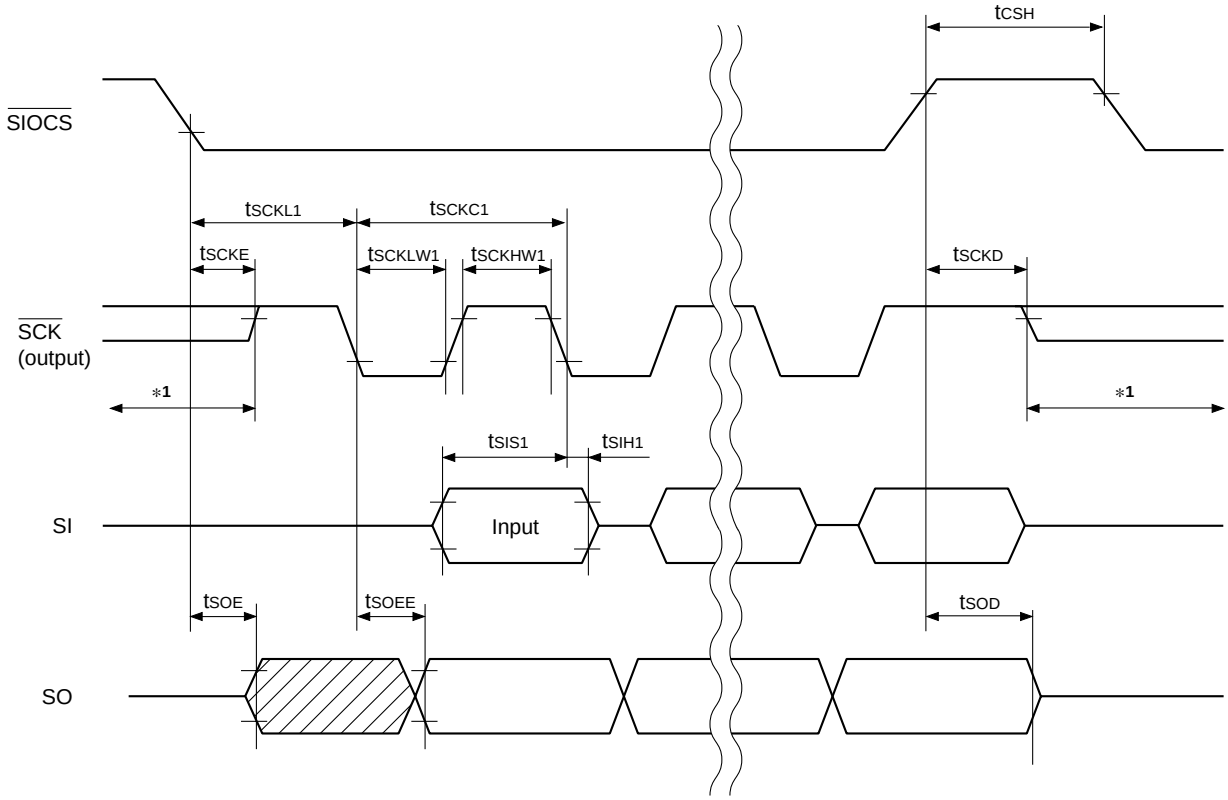
(6) D/A Converter Characteristics (Within the recommended operating range)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution			—	8	—	bits
Linearity error	El_{DA}	Endpoint method	—	0.34	—	LSB
Differential linearity error	Ed_{DA}		—	0.17	—	LSB
Output full-scale voltage	VFS		—	DAC_AVD – 1LSB	—	V

(7) Serial Transfer

SCK = Output mode (Within the recommended operating range)

Item	Symbol	Conditions	Min.	Max.	Unit
$\overline{\text{SIOCS}}$ high level width	t_{CSH}	CS automatic transfer mode	2tsys + 20		ns
$\overline{\text{SIOCS}} \downarrow \rightarrow \overline{\text{SCK}}$ enable	t_{SCKE}			2tsys + 50	ns
$\overline{\text{SIOCS}} \uparrow \rightarrow \overline{\text{SCK}}$ disable	t_{SCKD}			2tsys + 50	ns
$\overline{\text{SIOCS}} \downarrow \rightarrow$ SO enable	t_{SOE}			2tsys + 50	ns
$\overline{\text{SIOCS}} \uparrow \rightarrow$ SO disable	t_{SOD}			2tsys + 50	ns
$\overline{\text{SIOCS}} \downarrow \rightarrow \overline{\text{SCK}}$ low	t_{SCKL1}		4tsys		ns
$\overline{\text{SCK}}$ high pulse width	t_{SCKHW1}		$8/f_{EX}$ – 20		ns
$\overline{\text{SCK}}$ low pulse width	t_{SCKLW1}		$8/f_{EX}$ – 20		ns
$\overline{\text{SCK}}$ cycle time	t_{SCKC1}		$16/f_{EX}$		ns
SI input data setup time (activated by $\overline{\text{SCK}} \downarrow$)	t_{SIS1}		2tsys + 50		ns
SI input data hold time (activated by $\overline{\text{SCK}} \downarrow$)	t_{SIH1}		0		ns
$\overline{\text{SCK}} \downarrow \rightarrow$ SO delay time	t_{SOEE}			30	ns



*1 Output disabled state (Set to high level by an internal pull-up resistor.)

Fig. 7-1. Serial Transfer Timing ($\overline{\text{SCK}}$: Output mode)

SCK = Input mode (Within the recommended operating range)

Item	Symbol	Conditions	Min.	Max.	Unit
$\overline{\text{SIOCS}}$ high level width	t_{CSH}	CS automatic transfer mode	2tsys + 20		ns
$\overline{\text{SIOCS}} \downarrow \rightarrow \overline{\text{SCK}}$ low*2	t_{SCKL2}		4tsys + 20		ns
$\overline{\text{SIOCS}} \downarrow \rightarrow$ SO enable	t_{SOE}			2tsys + 50	ns
$\overline{\text{SIOCS}} \uparrow \rightarrow$ SO disable	t_{SOD}			2tsys + 50	ns
$\overline{\text{SCK}}$ high pulse width	t_{SCKH2}		tsys + 20		ns
$\overline{\text{SCK}}$ low pulse width	t_{SCKL2}		tsys + 20		ns
$\overline{\text{SCK}}$ cycle time	t_{SCKC2}		2tsys + 40		ns
SI input data setup time (activated by $\overline{\text{SCK}} \uparrow$)	t_{SIS2}		20		ns
SI input data hold time (activated by $\overline{\text{SCK}} \uparrow$)	t_{SIH2}		20		ns
$\overline{\text{SCK}} \downarrow \rightarrow$ SO delay time	t_{SOEE2}			3tsys + 50	ns

*2 Even if $\overline{\text{SCK}}$ goes to low level before $\overline{\text{SIOCS}}$ falls, this is ignored.

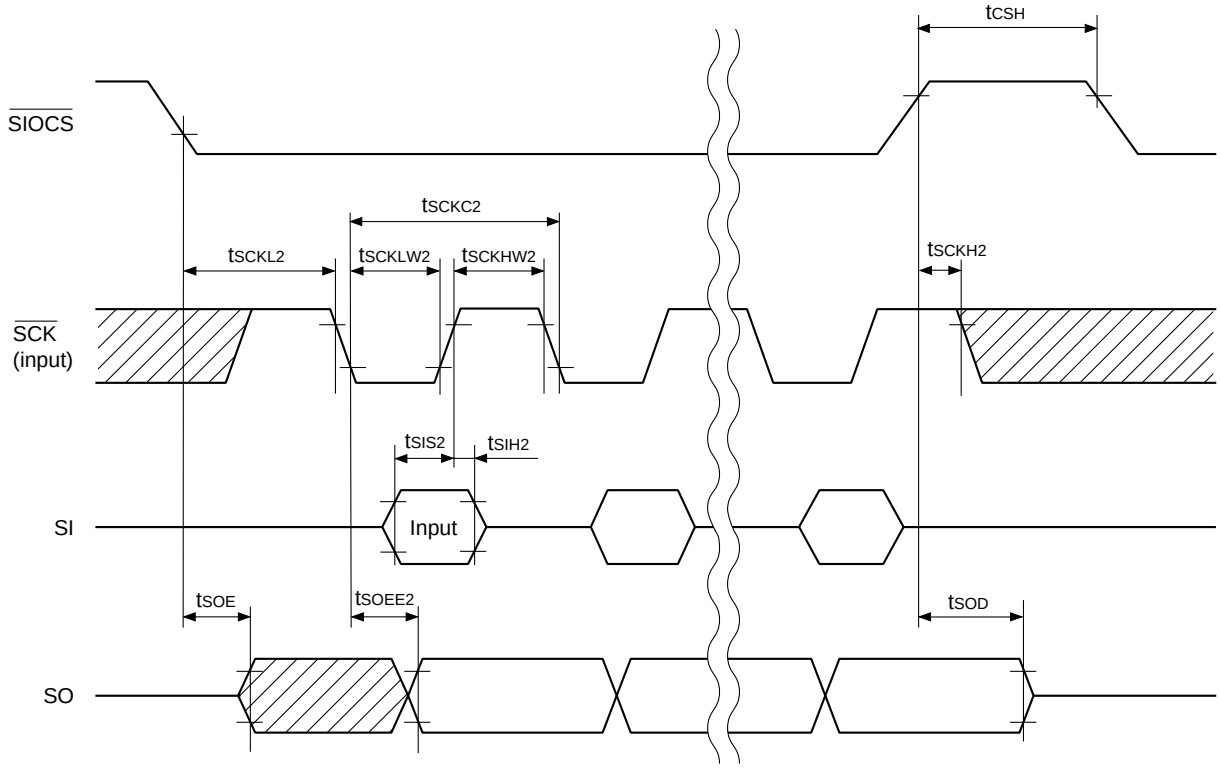


Fig. 7-2. Serial Transfer Timing ($\overline{\text{SCK}}$: Input mode)

(8) External Memory Interface

Read Timing (Within the recommended operating range)

Item	Symbol	Min.	Max.	Unit
Chip select pulse width*1	t_{RCS}	(2 + BWTn) × tsys – 20	(2 + BWTn) × tsys + 20	ns
Read strobe pulse width*1	t_{RD}	(1 + BWTn) × tsys – 20	(1 + BWTn) × tsys + 20	ns
Address $\overline{CSn}$ ↓ → $\overline{RD}$ ↓	t_{CSRD}	tsys – 20	tsys + 20	ns
Read data setup time	t_{DS}	50	—	ns
Read data hold time*2	t_{DH}	0	—	ns

*1 BWTn: Number of waits setting

*2 Prescribed from the timing at which any of A0 to A20, $\overline{CSn}$ or $\overline{RD}$ first becomes invalid.

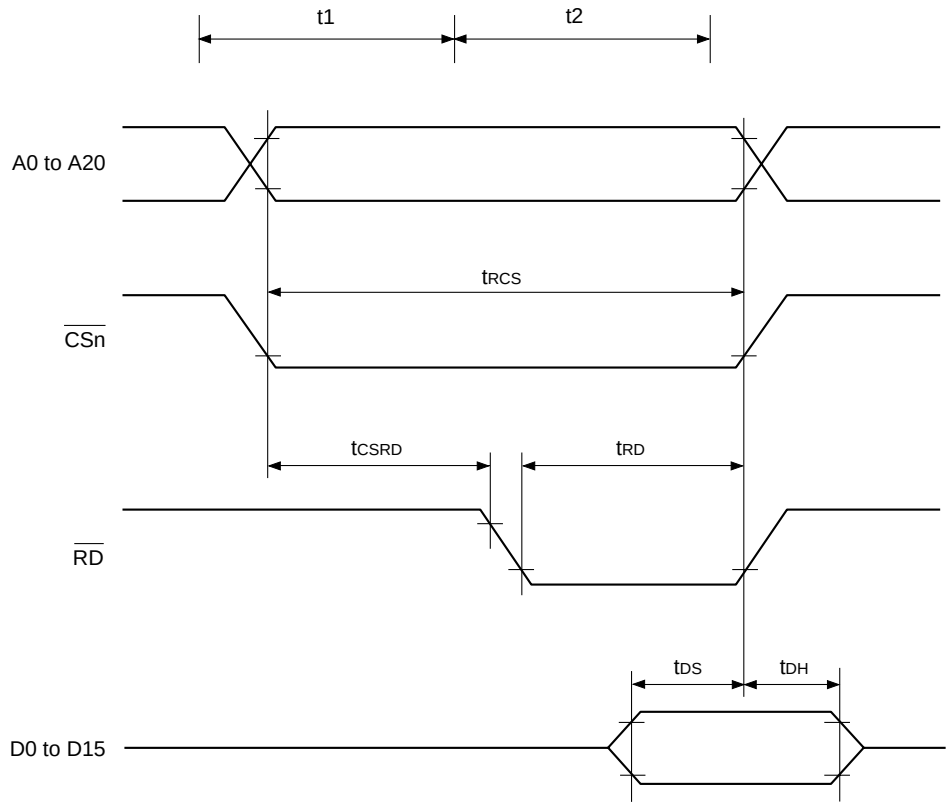


Fig. 8-1. External Memory Interface Timing (Read)

Write Timing (Within the recommended operating range)

Item	Symbol	Min.	Max.	Unit
Chip select pulse width	t_{WCS}	(3 + BWTn) × tsys – 20	(3 + BWTn) × tsys + 20	ns
Read strobe pulse width	t_{WR}	(1 + BWTn) × tsys – 20	(1 + BWTn) × tsys + 20	ns
Address $\overline{CSn}$ ↓ → $\overline{WR}$ ↓	t_{CSWR}	tsys/2 – 20	tsys/2 + 20	ns
$\overline{WR}$ ↑ → address $\overline{CSn}$ ↑	t_{WRCS}	tsys/2 – 20	tsys/2 + 20	ns
Write data enable → $\overline{WR}$ ↑	t_{DWR}	(1.5 + BWTn) × tsys – 20	(1.5 + BWTn) × tsys + 20	ns
$\overline{WR}$ ↑ → write data disable	t_{WRD}	10	tsys/2 + 20	ns

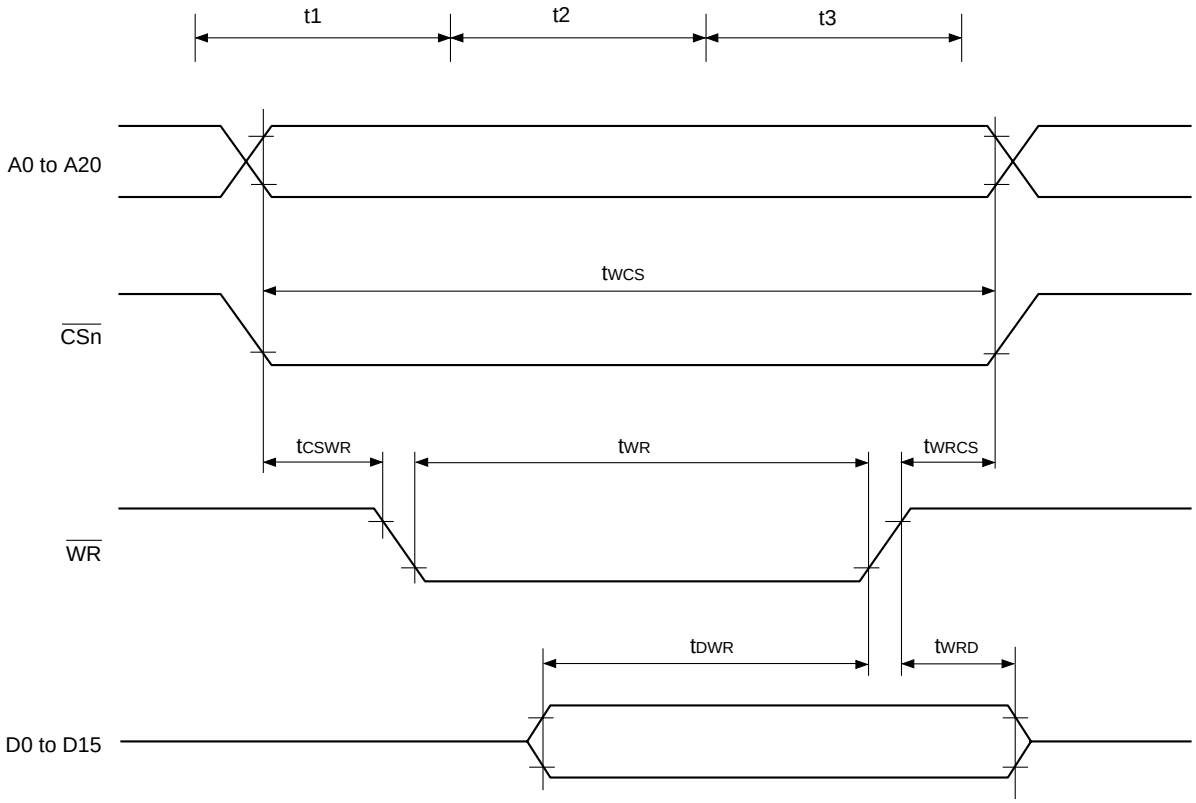
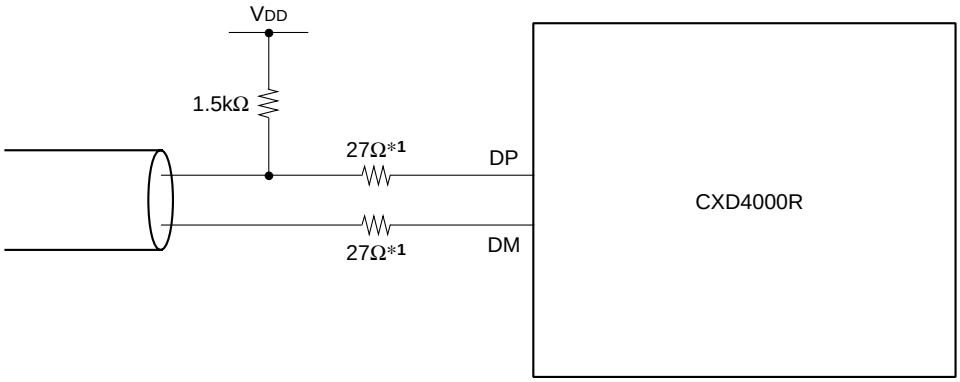


Fig. 8-2. External Memory Interface Timing (Write)

(9) USB Interface (Within the recommended operating range)

Item	Symbol	Conditions	Min.	Max.	Unit
Output impedance	Zdrv		28	43	Ω
Rise time	Tr	CL = 50pF	4	20	ns
Fall time	Tf	CL = 50pF	4	20	ns
Rise/fall ratio	Tr/Tf	CL = 50pF	0.9	1.1	—
Output signal crossover voltage	Vcrs	CL = 50pF	1.3	2.0	V

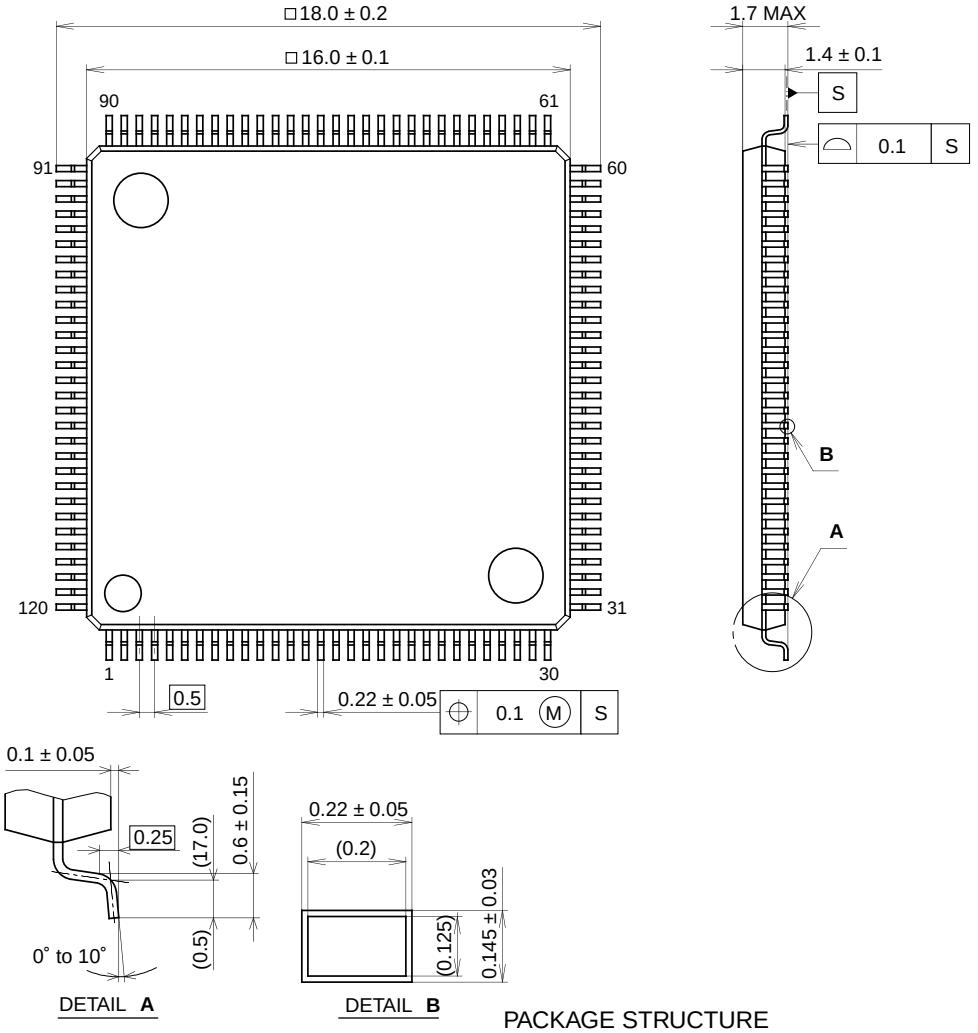


*1 Connect the DP and DM pins to the USB cable through 27Ω resistors.

Fig. 9. USB Interface Connection Circuit

Package Outline Unit: mm

120PIN LQFP (PLASTIC)



SONY CODE	LQFP-120P-L01
EIAJ CODE	LQFP120-P-1616
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.8g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm