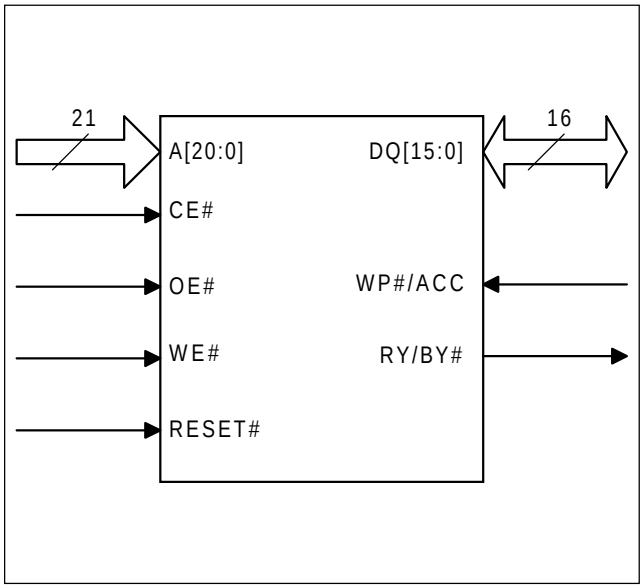
KEY FEATURES

- **Single Power Supply Operation**
  - Read, program and erase operations from 2.7 to 3.6 volts
  - Ideal for battery-powered applications
- **High Performance**
  - 70, 80, 90 and 120 ns access time versions for full voltage range operation
- **Ultra-low Power Consumption (Typical/ Maximum Values)**
  - Automatic sleep/standby current: 0.5/5.0 µA
  - Read current: 9/16 mA (@ 5 MHz)
  - Program/erase current: 20/30 mA
- **Top and Bottom Boot Block Versions**
  - Provide one 8 KW, two 4 KW, one 16 KW and sixty-three 32 KW sectors
- **Secured Sector**
  - An extra 128-word, factory-lockable sector available for an Electronic Serial Number and/or additional secured data
- **Sector Protection**
  - Allows locking of a sector or sectors to prevent program or erase operations within that sector
  - Temporary Sector Unprotect allows changes in locked sectors
- **Fast Program and Erase Times (typicals)**
  - Sector erase time: 0.5 sec per sector
  - Chip erase time: 32 sec
  - Word program time: 11 µs
  - Accelerated program time per word: 7 µs
- **Automatic Erase Algorithm Preprograms and Erases Any Combination of Sectors or the Entire Chip**
- **Automatic Program Algorithm Writes and Verifies Data at Specified Addresses**
- **Compliant With Common Flash Memory Interface (CFI) Specification**
  - Flash device parameters stored directly on the device
  - Allows software driver to identify and use a variety of current and future Flash products
- **Minimum 100,000 Write Cycles per Sector**
- **Compatible With JEDEC standards**
  - Pinout and software compatible with single-power supply Flash devices
  - Superior inadvertent write protection
- **Data# Polling and Toggle Bits**
  - Provide software confirmation of completion of program and erase operations
- **Ready/Busy (RY/BY#) Pin**
  - Provides hardware confirmation of completion of program and erase operations
- **Write Protect Function (WP#/ACC pin)**
  - Allows hardware protection of the first or last 32 KW of the array, regardless of sector protect status
- **Acceleration Function (WP#/ACC pin)**
  - Provides accelerated program times
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to allow reading data from, or programming data to, a sector that is not being erased
  - Erase Resume can then be invoked to complete suspended erasure
- **Hardware Reset Pin (RESET#) Resets the Device to Reading Array Data**
- **Space Efficient Packaging**
  - 48-pin TSOP and 63-ball FBGA packages

LOGIC DIAGRAM



GENERAL DESCRIPTION

The HY29LV320 is a 32 Mbit, 3 volt-only CMOS Flash memory organized as 2,097,152 (2M) words. The device is available in 48-pin TSOP and 63-ball FBGA packages. Word-wide data (x16) appears on DQ[15:0].

The HY29LV320 can be programmed and erased in-system with a single 3 volt V_{CC} supply. Internally generated and regulated voltages are provided for program and erase operations, so that the device does not require a higher voltage V_{PP} power supply to perform those functions. The device can also be programmed in standard EPROM programmers. Access times as fast as 70ns over the full operating voltage range of 2.7 - 3.6 volts are offered for timing compatibility with the zero wait state requirements of high speed microprocessors. To eliminate bus contention, the HY29LV320 has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device is compatible with the JEDEC single-power-supply Flash command set standard. Commands are written to the command register using standard microprocessor write timings, from where they are routed to an internal state-machine that controls the erase and programming circuits. Device programming is performed a word at a time by executing the four-cycle Program Command write sequence. This initiates an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Faster programming times are achieved by placing the HY29LV320 in the Unlock Bypass mode, which requires only two write cycles to program data instead of four.

The HY29LV320 features a sector architecture and is offered in two versions:

- **HY29LV320B** - a device with boot-sector architecture with the boot sectors at the bottom of the address range, containing one 8KW, two 4KW, one 16KW and sixty-three 32KW sectors.
- **HY29LV320T** - a device with boot-sector architecture with the boot sectors at the top of the address range, containing one 8KW, two 4KW, one 16KW and sixty-three 32KW sectors.

The HY29LV320's sector erase architecture allows any number of array sectors to be erased and reprogrammed without affecting the data contents of other sectors. Device erasure is initiated by executing the Erase Command sequence. This initiates an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. As during programming cycles, the device automatically times the erase pulse widths and verifies proper cell margin. Sectors are arranged into designated groups for purposes of protection and unprotection. Sector Group Protection optionally disables both program and erase operations in any combination of the sector groups of the memory array, while Temporary Sector Group Unprotect allows in-system erasure and code changes in previously protected sector groups. Erase Suspend enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. The device is fully erased when shipped from the factory.

Addresses and data needed for the programming and erase operations are internally latched during write cycles, and the host system can detect completion of a program or erase operation by observing the RY/BY# pin, or by reading the DQ[7] (Data# Polling) and DQ[6] (Toggle) status bits. Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions.

After a program or erase cycle has been completed, or after assertion of the RESET# pin (which terminates any operation in progress), the device is ready to read data or to accept another command. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The Secured Sector is an extra 128 word sector capable of being permanently locked at the factory or by customers. The Secured Indicator Bit (accessed via the Electronic ID mode) is permanently set to a '1' if the part is factory locked, and permanently set to a '0' if customer lockable. This way, customer lockable parts can never be used to replace a factory locked part. Factory locked parts provide several options. The Secured Sector may store a secure, random 8-word ESN (Electronic Serial Number), customer code programmed at the factory, or both. Customer Lock-

able parts may utilize the Secured Sector as bonus space, reading and writing like any other Flash sector, or may permanently lock their own code there.

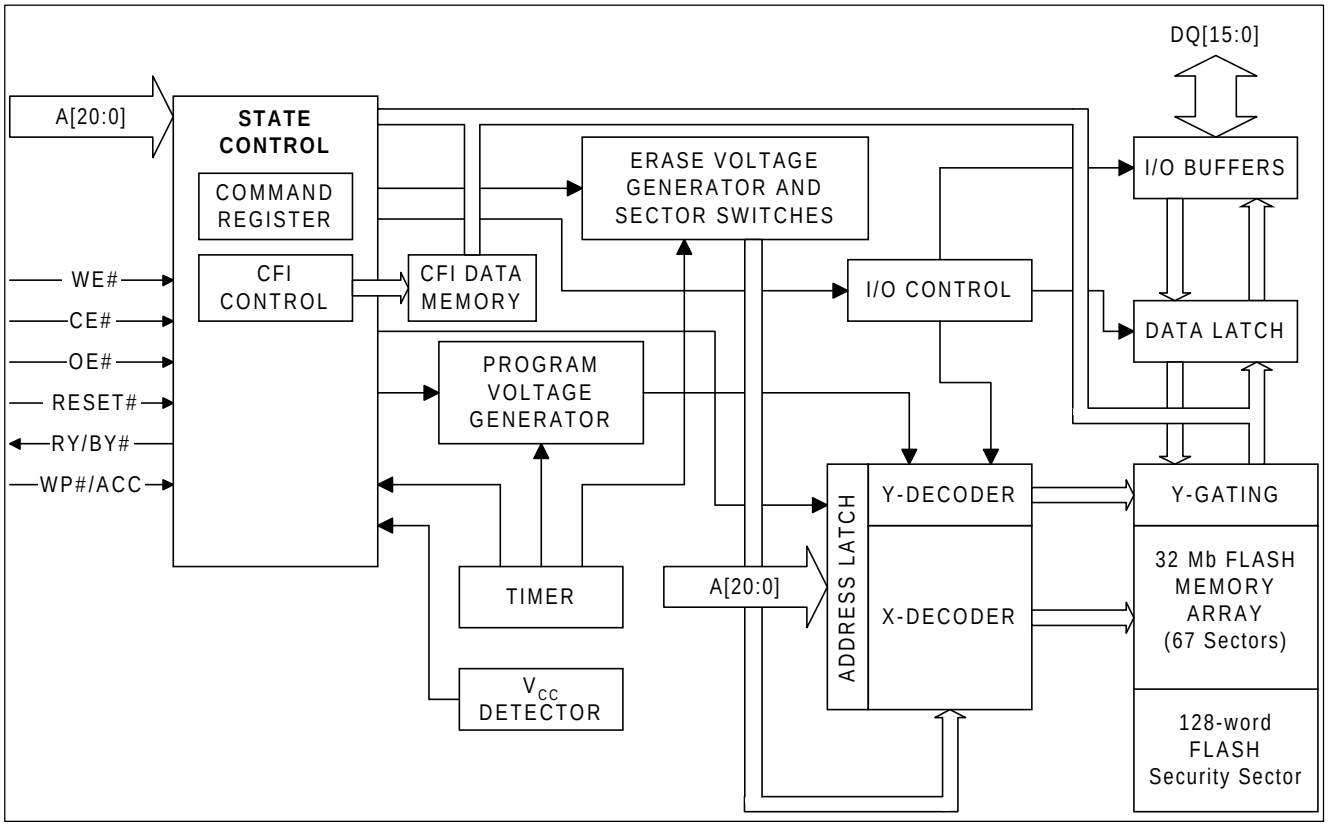
The WP#/ACC pin provides two functions. The Write Protect function provides a hardware method of protecting the boot sectors without using a high voltage. The Accelerate function speeds up programming operations, and is intended primarily to allow faster manufacturing throughput.

Two power-saving features are embodied in the HY29LV320. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The host can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

Common Flash Memory Interface (CFI)

To make Flash memories interchangeable and to encourage adoption of new Flash technologies, major Flash memory suppliers developed a flexible method of identifying Flash memory sizes and configurations in which all necessary Flash device parameters are stored directly on the device. Parameters stored include memory size, byte/word configuration, sector configuration, necessary voltages and timing information. This allows one set of software drivers to identify and use a variety of different, current and future Flash products. The standard which details the software interface necessary to access the device to identify it and to determine its characteristics is the Common Flash Memory Interface (CFI) Specification. The HY29LV320 is fully compliant with this specification.

BLOCK DIAGRAM

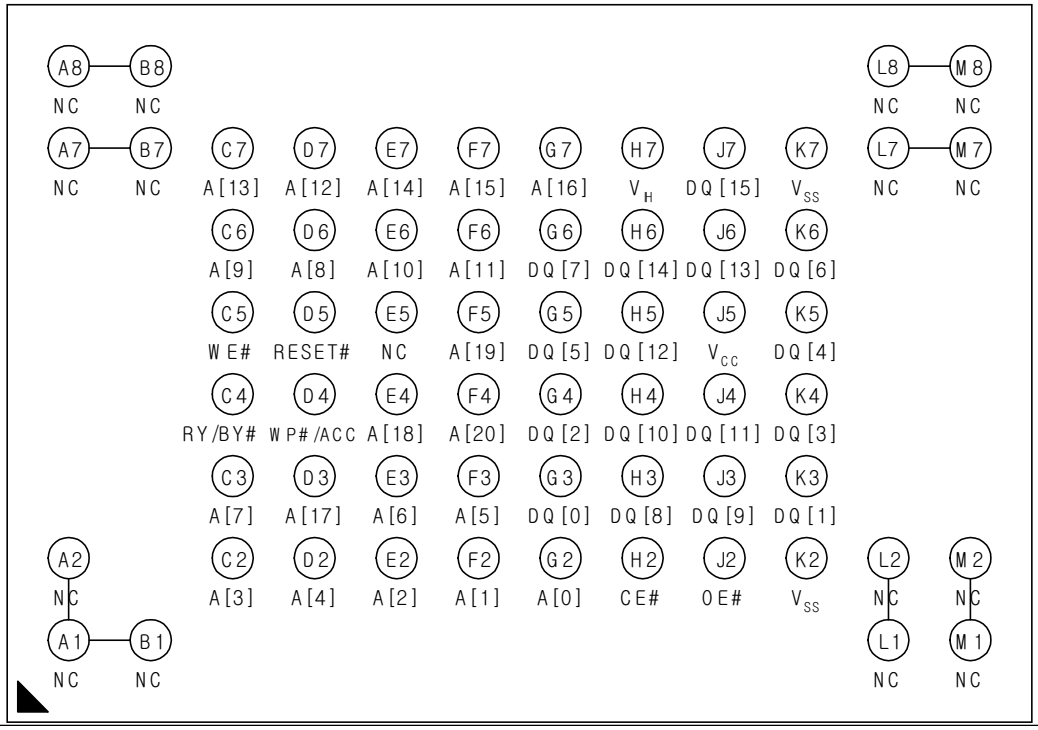


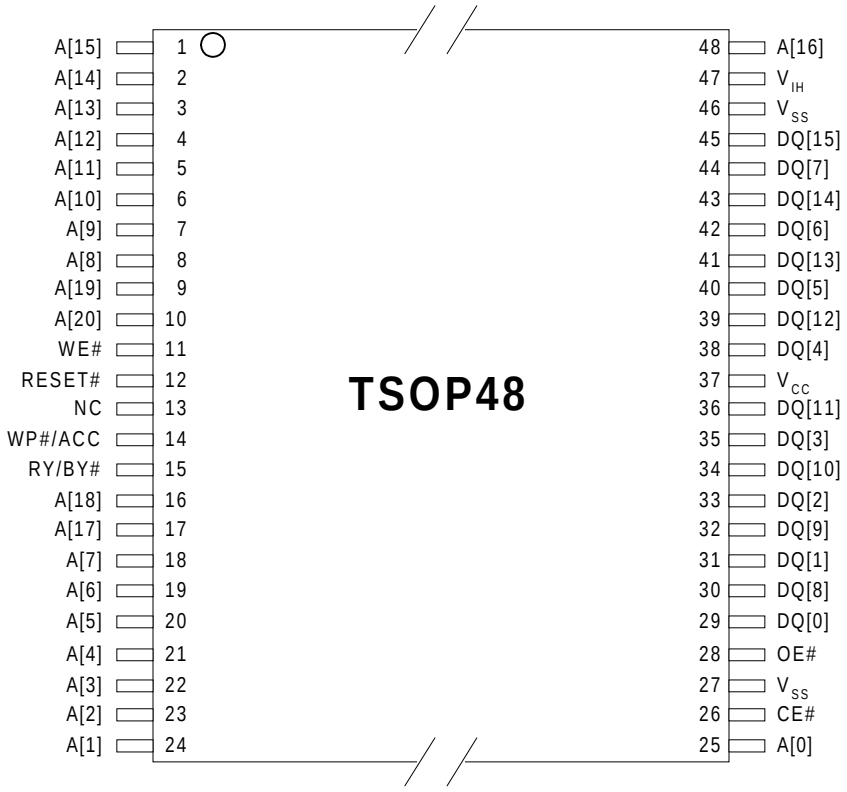
SIGNAL DESCRIPTIONS

Name	Type	Description
A[20:0]	Inputs	**Address, active High.** These 21 inputs select one of 2,097,152 (2M) words within the array for read or write operations.
DQ[15:0]	Inputs/Outputs Tri-state	**Data Bus, active High**. These pins provide a 16-bit data path for read and write operations.
CE#	Input	**Chip Enable, active Low.** This input must be asserted to read data from or write data to the HY29LV320. When High, the data bus is tri-stated and the device is placed in the Standby mode.
OE#	Input	**Output Enable, active Low**. This input must be asserted for read operations and negated for write operations. When High, data outputs from the device are disabled and the data bus pins are placed in the high impedance state.
WE#	Input	**Write Enable, active Low.** Controls writing of commands or command sequences for various device operations. A write operation takes place when WE# is asserted while CE# is also Low and OE# is High.
RESET#	Input	**Hardware Reset, active Low.** Provides a hardware method of resetting the HY29LV320 to the read array state. When the device is reset, it immediately terminates any operation in progress. The data bus is tri-stated and all read/write commands are ignored while the input is asserted. While RESET# is asserted the device will be in the Standby mode.
RY/BY#	Output Open Drain	**Ready/Busy Status.** Indicates whether a write or erase command is in progress or has been completed. Valid after the rising edge of the final WE# pulse of a command sequence. Remains Low while the device is actively programming data or erasing, and goes High when it is ready to read array data.
WP#/ACC	Input	**Write Protect, active Low/Accelerate (V_{HH}).** Placing this pin at V_{IL} disables program and erase operations in the top or bottom 32K words of the array. The affected sectors are sectors S0 - S3 for the HY29LV320B and sectors S63 - S66 for the HY29LV320T. If the pin is placed at V_{IH}, the protection state of those two sectors reverts to whether they were last set to be protected or unprotected using the Sector Group Protection and Unprotection capability of the HY29LV320. If V_{HH} is applied to this input, the device enters the Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. (The system would then use the two-cycle program command sequence as required by the Unlock Bypass mode.) Removing V_{HH} from the pin returns the device to normal operation. This pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. Leaving the pin floating or unconnected may result in inconsistent device operation.
V_{IH}	Input	**High Input.** Connect to V_{IH} or to V_{CC} to provide compatibility with similar x8/x16 devices.
V_{CC}	--	**3-volt (nominal) power supply.**
V_{SS}	--	**Power and signal ground.**

PIN CONFIGURATIONS

63-BallFBGA - Top View, Balls Facing Down





CONVENTIONS

Unless otherwise noted, a positive logic (active High) convention is assumed throughout this document, whereby the presence at a pin of a higher, more positive voltage (V_{IH}) causes assertion of the signal. A '#' symbol following the signal name, e.g., RESET#, indicates that the signal is asserted in the Low state (V_{IL}). See DC specifications for V_{IH} and V_{IL} values.

Whenever a signal is separated into numbered bits, e.g., DQ[7], DQ[6], ..., DQ[0], the family of bits may also be shown collectively, e.g., as DQ[7:0].

The designation 0xNNNN (N = 0, 1, 2, . . . , 9, A, . . . , E, F) indicates a number expressed in hexadecimal notation. The designation 0bXXXX indicates a number expressed in binary notation (X = 0, 1).

MEMORY ARRAY ORGANIZATION

The 32 Mbit Flash memory array is organized into 67 blocks called *sectors* (S0, S1, . . . , S66). A sector or several contiguous sectors are defined as a *sector group*. A sector is the smallest unit that can be erased and a sector group is the smallest unit that can be protected to prevent accidental or unauthorized erasure.

In the HY29LV320, four of the sectors, which comprise the *boot block*, are sized as follows: one of eight Kwords, two of four Kwords and one of sixteen Kwords. The remaining 63 sectors are sized at 32 Kwords. The boot block can be located at the bottom of the address range (HY29LV320B) or at the top of the address range (HY29LV320T).

Tables 1 and 2 define the sector addresses and corresponding array address ranges for the top and bottom boot block versions of the HY29LV320. See Tables 6 and 7 for sector group definitions.

Secured Sector Flash Memory Region

The Secured Sector (Sec^2) feature provides a 128 word Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). An associated 'Sec^2 Indicator' bit, which is permanently set at the factory and cannot be changed, indicates whether or not the Sec^2 is locked when shipped from the factory.

The device is offered with the Sec^2 either factory locked or customer lockable. The *factory-locked* version is always protected when shipped from the factory, and has the Sec^2 Indicator bit permanently set to a '1'. The *customer-lockable* version is shipped with the Sec^2 unprotected, allowing customers to utilize the sector in any manner they choose, and has the Sec^2 Indicator bit permanently set to a '0'. Thus, the Sec^2 Indicator bit prevents customer-lockable devices from being used to replace devices that are factory locked. The bit prevents cloning of a factory locked part and thus ensures the security of the ESN once the product is shipped to the field.

The system accesses the Sec^2 through a command sequence (see "Enter/Exit Secured Sector Command Sequence"). After the system has written the Enter Secured Sector command sequence, it may read the Sec^2 by using the addresses specified in Table 3. This mode of operation continues until the system issues the Exit Secured Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to addressing the Flash array.

> **Note:** While in the Sec^2 Read mode, only the reading of the 'Replaced Sector' (Table 3) is affected. Accesses within the specified sector, but outside the address range specified in the table, may produce indeterminate results. Reading of all other sectors in the device continues normally while in this mode.

Sec^2 Programmed and Protected At the Factory

In a factory-locked device, the Sec^2 is protected when the device is shipped from the factory and cannot be modified in any way. The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code
- Both a random, secure ESN and customer code

In devices that have an ESN, it will be located at the bottom of the sector: starting at word address 0x000000 and ending at 0x000007 for a Bottom Boot device, and starting at word address 0x1FE000 and ending at 0x1FE007 for a Top Boot device. See Table 3.

Table 1. HY29LV320T (Top Boot Block) Memory Array Organization

Sect-or	Size (KWord)	Sector Address [1]									Address Range [2, 3]
		A[20]	A[19]	A[18]	A[17]	A[16]	A[15]	A[14]	A[13]	A[12]	
S0	32	0	0	0	0	0	0	X	X	X	0x000000 - 0x007FFF
S1	32	0	0	0	0	0	1	X	X	X	0x008000 - 0x00FFFF
S2	32	0	0	0	0	1	0	X	X	X	0x010000 - 0x017FFF
S3	32	0	0	0	0	1	1	X	X	X	0x018000 - 0x01FFFF
S4	32	0	0	0	1	0	0	X	X	X	0x020000 - 0x027FFF
S5	32	0	0	0	1	0	1	X	X	X	0x028000 - 0x02FFFF
S6	32	0	0	0	1	1	0	X	X	X	0x030000 - 0x037FFF
S7	32	0	0	0	1	1	1	X	X	X	0x038000 - 0x03FFFF
S8	32	0	0	1	0	0	0	X	X	X	0x040000 - 0x047FFF
S9	32	0	0	1	0	0	1	X	X	X	0x048000 - 0x04FFFF
S10	32	0	0	1	0	1	0	X	X	X	0x050000 - 0x057FFF
S11	32	0	0	1	0	1	1	X	X	X	0x058000 - 0x05FFFF
S12	32	0	0	1	1	0	0	X	X	X	0x060000 - 0x067FFF
S13	32	0	0	1	1	0	1	X	X	X	0x068000 - 0x06FFFF
S14	32	0	0	1	1	1	0	X	X	X	0x070000 - 0x077FFF
S15	32	0	0	1	1	1	1	X	X	X	0x078000 - 0x07FFFF
S16	32	0	1	0	0	0	0	X	X	X	0x080000 - 0x087FFF
S17	32	0	1	0	0	0	1	X	X	X	0x088000 - 0x08FFFF
S18	32	0	1	0	0	1	0	X	X	X	0x090000 - 0x097FFF
S19	32	0	1	0	0	1	1	X	X	X	0x098000 - 0x09FFFF
S20	32	0	1	0	1	0	0	X	X	X	0x0A0000 - 0x0A7FFF
S21	32	0	1	0	1	0	1	X	X	X	0x0A8000 - 0x0AFFFF
S22	32	0	1	0	1	1	0	X	X	X	0x0B0000 - 0x0B7FFF
S23	32	0	1	0	1	1	1	X	X	X	0x0B8000 - 0x0BFFFF
S24	32	0	1	1	0	0	0	X	X	X	0x0C0000 - 0x0C7FFF
S25	32	0	1	1	0	0	1	X	X	X	0x0C8000 - 0x0CFFFF
S26	32	0	1	1	0	1	0	X	X	X	0x0D0000 - 0x0D7FFF
S27	32	0	1	1	0	1	1	X	X	X	0x0D8000 - 0x0DFFFF
S28	32	0	1	1	1	0	0	X	X	X	0x0E0000 - 0x0E7FFF
S29	32	0	1	1	1	0	1	X	X	X	0x0E8000 - 0x0EFFFF
S30	32	0	1	1	1	1	0	X	X	X	0x0F0000 - 0x0F7FFF
S31	32	0	1	1	1	1	1	X	X	X	0x0F8000 - 0x0FFFFF
S32 - S62	32	Same as S0 - S30 except A[20] = 1									Same as S0 - S30 except MSD = 1
S63	16	1	1	1	1	1	1	0	X	X	0x1F8000 - 0x1FBFFF
S64	4	1	1	1	1	1	1	1	0	0	0x1FC000 - 0x1FCFFF
S65	4	1	1	1	1	1	1	1	0	1	0x1FD000 - 0x1FDFFF
S66	8	1	1	1	1	1	1	1	1	X	0x1FE000 - 0x1FFFFF

Notes:
1. 'X' indicates don't care.
2. '0xN. . . N' indicates an address in hexadecimal notation.
3. The address range is A[20:0].

Table 2. HY29LV320B (Bottom Boot Block) Memory Array Organization

Sector	Size (KWord)	Sector Address [1]									Address Range [2, 3]
		A[20]	A[19]	A[18]	A[17]	A[16]	A[15]	A[14]	A[13]	A[12]	
S0	8	0	0	0	0	0	0	0	0	X	0x000000 - 0x001FFF
S1	4	0	0	0	0	0	0	0	1	0	0x002000 - 0x002FFF
S2	4	0	0	0	0	0	0	0	1	1	0x003000 - 0x003FFF
S3	16	0	0	0	0	0	0	1	X	X	0x004000 - 0x007FFF
S4	32	0	0	0	0	0	1	X	X	X	0x008000 - 0x00FFFF
S5	32	0	0	0	0	1	0	X	X	X	0x010000 - 0x017FFF
S6	32	0	0	0	0	1	1	X	X	X	0x018000 - 0x01FFFF
S7	32	0	0	0	1	0	0	X	X	X	0x020000 - 0x027FFF
S8	32	0	0	0	1	0	1	X	X	X	0x028000 - 0x02FFFF
S9	32	0	0	0	1	1	0	X	X	X	0x030000 - 0x037FFF
S10	32	0	0	0	1	1	1	X	X	X	0x038000 - 0x03FFFF
S11	32	0	0	1	0	0	0	X	X	X	0x040000 - 0x047FFF
S12	32	0	0	1	0	0	1	X	X	X	0x048000 - 0x04FFFF
S13	32	0	0	1	0	1	0	X	X	X	0x050000 - 0x057FFF
S14	32	0	0	1	0	1	1	X	X	X	0x058000 - 0x05FFFF
S15	32	0	0	1	1	0	0	X	X	X	0x060000 - 0x067FFF
S16	32	0	0	1	1	0	1	X	X	X	0x068000 - 0x06FFFF
S17	32	0	0	1	1	1	0	X	X	X	0x070000 - 0x077FFF
S18	32	0	0	1	1	1	1	X	X	X	0x078000 - 0x07FFFF
S19	32	0	1	0	0	0	0	X	X	X	0x080000 - 0x087FFF
S20	32	0	1	0	0	0	1	X	X	X	0x088000 - 0x08FFFF
S21	32	0	1	0	0	1	0	X	X	X	0x090000 - 0x097FFF
S22	32	0	1	0	0	1	1	X	X	X	0x098000 - 0x09FFFF
S23	32	0	1	0	1	0	0	X	X	X	0x0A0000 - 0x0A7FFF
S24	32	0	1	0	1	0	1	X	X	X	0x0A8000 - 0x0AFFFF
S25	32	0	1	0	1	1	0	X	X	X	0x0B0000 - 0x0B7FFF
S26	32	0	1	0	1	1	1	X	X	X	0x0B8000 - 0x0BFFFF
S27	32	0	1	1	0	0	0	X	X	X	0x0C0000 - 0x0C7FFF
S28	32	0	1	1	0	0	1	X	X	X	0x0C8000 - 0x0CFFFF
S29	32	0	1	1	0	1	0	X	X	X	0x0D0000 - 0x0D7FFF
S30	32	0	1	1	0	1	1	X	X	X	0x0D8000 - 0x0DFFFF
S31	32	0	1	1	1	0	0	X	X	X	0x0E0000 - 0x0E7FFF
S32	32	0	1	1	1	0	1	X	X	X	0x0E8000 - 0x0EFFFF
S33	32	0	1	1	1	1	0	X	X	X	0x0F0000 - 0x0F7FFF
S34	32	0	1	1	1	1	1	X	X	X	0x0F8000 - 0x0FFFFF
S35	32	1	0	0	0	0	0	X	X	X	0x100000 - 0x107FFF
S36 - S66	32	Same as S4 - S34 except A[20] = 1									Same as S4 - S34 except MSD = 1

Notes:
1. 'X' indicates don't care.
2. '0xN. . . N' indicates an address in hexadecimal notation.
3. The address range is A[20:0].

Table 3. HY29LV320 Secure Sector Addressing

Device	Sector Size (Words)	Replaced Sector [1]	Address Range [2]	Electronic Serial Number Address Range [2]
HY29LV320T	128	S66 (Table 1)	0x1FE000 - 0x1FE07F	0x1FE000 - 0x1FE007
HY29LV320B	128	S0 (Table 2)	0x000000 - 0x00007F	0x000000 - 0x000007

Notes:
1. Accesses within the specified sector, but outside the specified address range, may produce indeterminate results.
2. '0xN. . . N' indicates an address in hexadecimal notation. The address range is A[20:0].

Sec² NOT Programmed or Protected at the Factory

If the security feature is not required, the Sec² can be treated as an additional Flash memory space of 128 words. The Sec² can be read, programmed, and erased as often as required. The Sec² area can be protected using the following procedure:

- Write the three-cycle Enter Secure Sector Region command sequence.
- Follow the in-system sector protect algorithm as shown in Figure 3, except that RESET# may be at either V_{IH} or V_{ID}. This allows in-system protection of the Secure Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secure Sector.
- Once the Secure Sector is locked and verified, the system must write the Exit Secure Sector command sequence to return to reading and writing the remainder of the array.

Sec² protection must be used with caution since, once protected, there is no procedure available for unprotecting the Sec² area and none of the bits in the Sec² memory space can be modified in any way.

BUS OPERATIONS

Device bus operations are initiated through the internal command register, which consists of sets of latches that store the commands, along with the address and data information, if any, needed to execute the specific command. The command register itself does not occupy any addressable memory location. The contents of the command register serve as inputs to an internal state machine whose outputs control the operation of the device.

Table 4 lists the normal bus operations, the inputs and control levels they require, and the resulting outputs. Certain bus operations require a high voltage on one or more device pins. Those are described in Table 5.

Data is read from the HY29LV320 by using standard microprocessor read cycles while placing the word address on the device's address inputs. The host system must drive the CE# and OE# pins LOW and drive WE# high for a valid read operation to take place. See Figure 1.

The HY29LV320 is automatically set for reading array data after device power-up and after a hardware reset to ensure that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data, and the device remains enabled for read accesses until the command register contents are altered.

This device features an Erase Suspend mode. While in this mode, the host may read the array data from any sector of memory that is not marked for erasure. If the host reads from an address within an erase-suspended (or erasing) sector, or while the device is performing a program operation, the device outputs status data instead of array data. After completing an Automatic Program or Erase algorithm within a sector, that sector automatically returns to the read array data mode. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception noted above.

The host must issue a hardware reset or the software reset command to return a sector to the read array data mode if DQ[5] goes high during a program or erase cycle, or to return the device to the read array data mode while it is in the Electronic ID mode.

Table 4. HY29LV320 Normal Bus Operations [1]

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	A[20:0]	DQ[15:0]
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}
Write	L	H	L	H	Notes 2, 3	A_{IN}	D_{IN}
Output Disable	L	H	H	H	L/H	X	High-Z
CE# Normal Standby	H	X	X	H	L/H	X	High-Z
CE# Deep Standby	V_{CC} ± 0.3V	X	X	V_{CC} ± 0.3V	L/H	X	High-Z
Hardware Reset (Normal Standby)	X	X	X	L	L/H	X	High-Z
Hardware Reset (Deep Standby)	X	X	X	V_{SS} ± 0.3V	L/H	X	High-Z

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care (L or H), D_{OUT} = Data Out, D_{IN} = Data In. See DC Characteristics for voltage levels.
2. If WP#/ACC = V_{IL}, the boot sectors are protected. If WP#/ACC = V_{IH}, the protection state of the boot sectors depends on whether they were last protected or unprotected using the method described in "Sector Group Protection and Unprotection". If WP#/ACC = V_{HH}, all sectors will be unprotected.
3. See Table 5 for Accelerated Program function with WP#/ACC = V_{HH}.

Table 5. HY29LV320 Bus Operations Requiring High Voltage [1, 2]

Operation		CE#	OE#	WE#	RESET#	WP#/ACC	A[20:12] [3]	A[9]	A[6]	A[1]	A[0]	DQ[15:0] [7]
Accelerated Program		L	H	L	H	V_{HH} [5]	A_{IN}	A_{IN}	A_{IN}	A_{IN}	A_{IN}	CMD_{IN}
Sector Group Protect		L	H	L	V_{ID}	H	SGA	X	L	H	L	CMD_{IN}
Sector Unprotect		L	H	L	V_{ID}	H	X	X	H	H	L	D_{IN}
Temporary Sector Unprotect [6]		--	--	--	V_{ID}	Note 4	--	--	--	--	--	--
Manufacturer Code		L	L	H	H	L/H	X	V_{ID}	L	L	L	0x00AD
Device Code	HY29LV320B	L	L	H	H	L/H	X	V_{ID}	L	L	H	0x227D
	HY29LV320T											0x227E
Sector Protect State [4]	Unprotected	L	L	H	H	L/H	SA	V_{ID}	L	H	L	0xXX00
	Protected											0xXX01
Secure Sector Indicator Bit	Factory Locked	L	L	H	H	L/H	X	V_{ID}	L	H	H	0xXX80
	Not Factory Locked											0xXX00

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care (L or H), V_{ID} = 12V nominal. See DC Characteristics for voltage specifications.
2. Address bits not specified are Don't Care.
3. SA = Sector Address, SGA = Sector Group Address. See Tables 1, 2, 6, and 7. A_{IN} = address input.
4. If WP#/ACC = V_{IL}, the boot sectors remain protected.
5. Protected sectors are temporarily unprotected when V_{HH} is applied to the WP#/ACC pin.
6. Normal read, write and output disable operations are used in this mode. See Table 4.
7. D_{IN} = input data, CMD_{IN} = Command input.

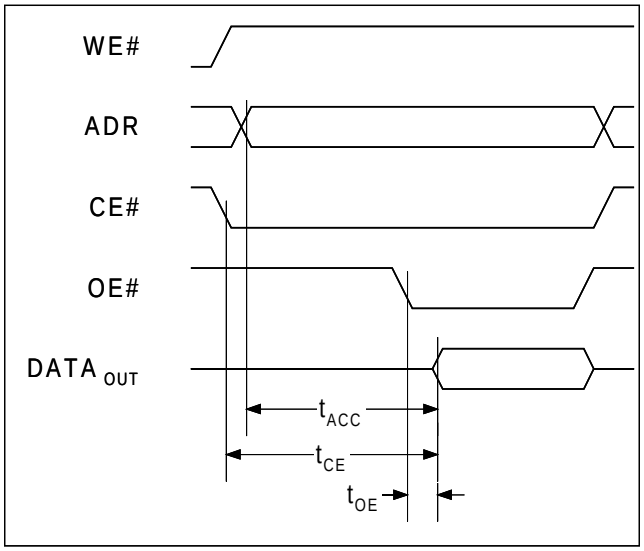


Figure 1. Read Operation

Write Operation

Certain operations, including programming data and erasing sectors of memory, require the host to write a command or command sequence to the HY29LV320. Writes to the device are performed by placing the word address on the device's address inputs while the data to be written is input on DQ[15:0]. The host system must drive the CE# and WE# pins Low and drive OE# High for a valid write operation to take place. All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. See Figure 2.

.The "Device Commands" section of this specification provides details on the specific device commands implemented in the HY29LV320.

Accelerated Program Operation

This device offers accelerated program operations through the "Accelerate" function provided by the WP#/ACC pin. This function is intended primarily for faster programming throughput at the factory.

If V_{HH} is applied to the WP#/ACC input, the device enters the Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would then use the two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the pin returns the device to normal operation.

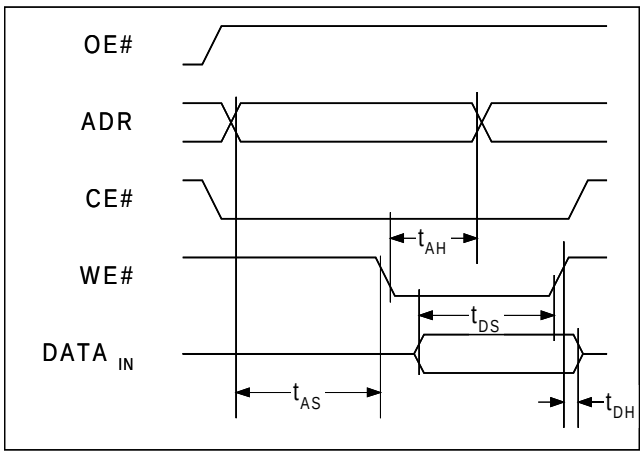


Figure 2. Write Operation

Note: WP# sector protection cannot be used while WP#/ACC = V_{HH}. Thus, all sectors are unprotected and can be erased and programmed while in Accelerated Programming mode.

Note: The Accelerate function does not affect the time required for Erase operations.

See the description of the WP#/ACC pin in the Pin Descriptions table for additional information on this function.

Write Protect Function

The Write Protect function provides a hardware method of protecting the boot sectors without using V_{ID}. This function is a second function provided by the WP#/ACC pin.

Placing this pin at V_{IL} disables program and erase operations in the bottom or top 32K words of the array (the boot sectors). The affected sectors are as follows (see Tables 1 and 2):

- HY29LV320B: S0 – S3
- HY29LV320T: S63 – S66

If the pin is placed at V_{IH}, the protection state of those sectors reverts to whether they were last set to be protected or unprotected using the method described in the Sector Group Protection and Unprotection sections.

Note: Sectors protected by WP#/ACC = V_{IL} remain protected during Temporary Sector Unprotect and cannot be erased or programmed. Also see note under Accelerate Program Operation above.

Standby Operation

When the system is not reading or writing to the device, it can place the device in the Standby

mode. In this mode, current consumption is greatly reduced, and the data bus outputs are placed in the high impedance state, independent of the OE# input. The Standby mode can invoked using two methods.

The device enters the *CE# Controlled Deep Standby* mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3V. Note that this is a more restricted voltage range than V_{IH} . If both CE# and RESET# are held at V_{IH} , but not within V_{CC} ± 0.3V, the device will be in the *Normal Standby* mode, but the standby current will be greater.

> **Note:** If the device is deselected during erasure or programming, it continues to draw active current until the operation is completed.

The device enters the *RESET# Controlled Deep Standby* mode when the RESET# pin is held at V_{SS} ± 0.3V. If RESET# is held at V_{IL} but not within V_{SS} ± 0.3V, the standby current will be greater. See RESET# section for additional information on the reset operation.

The device requires standard access time (t_{CE}) for read access when the device is in any of the standby modes before it is ready to read data.

Sleep Mode

The sleep mode automatically minimizes device power consumption. This mode is automatically entered when addresses remain stable for t_{ACC} + 30 ns (typical) and is independent of the state of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. The device does not enter sleep mode if an automatic program or automatic erase algorithm is in progress.

Output Disable Operation

When the OE# input is at V_{IH} , output data from the device is disabled and the data bus pins are placed in the high impedance state.

Reset Operation

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for the minimum specified period, the device immediately terminates any operation in progress, tri-states the data bus pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. If an operation was interrupted by the assertion of RESET#, it should be reinitiated once the device is ready to accept another command sequence to ensure data integrity.

Current is reduced for the duration of the RESET# pulse as described in the Standby Operation section.

If RESET# is asserted during a program or erase operation (RY/BY# pin is Low), the RY/BY# pin remains Low (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Automatic Algorithms). The system can thus monitor RY/BY# to determine when the reset operation completes, and can perform a read or write operation t_{RB} after RY/BY# goes High. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is High), the reset operation is completed within a time of t_{RP}. In this case, the host can perform a read or write operation t_{RH} after the RESET# pin returns High.

The RESET# pin may be tied to the system reset signal. Thus, a system reset would also reset the device, enabling the system to read the boot-up firmware from the Flash memory.

Sector Group Protect Operation

The hardware sector group protection feature disables both program and erase operations in any combination of sector groups. A sector group consists of a single sector or a group of adjacent sectors, as specified in Tables 6 and 7. This function can be implemented either in-system or by using programming equipment. It requires a high voltage (V_{ID}) on the RESET# pin and uses standard microprocessor bus cycle timing to implement sector protection. The flow chart in Figure 3 illustrates the algorithm.

The HY29LV320 is shipped with all sectors unprotected. It is possible to determine whether a sector is protected or unprotected. See the Electronic ID Mode section for details.

Sector Unprotect Operation

The hardware sector unprotection feature re-enables both program and erase operations in pre-

Table 6. Sector Groups - Top Boot Version

Group	Sectors (Table 1)	Group Address A[20:12]									Block Size (KWords)
SG0	S0	0	0	0	0	0	0	X	X	X	32
SG1	S1 - S3	0	0	0	0	0	1	X	X	X	96
		0	0	0	0	1	0	X	X	X	
		0	0	0	0	1	1	X	X	X	
SG2	S4 - S7	0	0	0	1	X	X	X	X	X	128
SG3	S8 -S11	0	0	1	0	X	X	X	X	X	128
SG4	S12 - S15	0	0	1	1	X	X	X	X	X	128
SG5	S16 - S19	0	1	0	0	X	X	X	X	X	128
SG6	S20 - S23	0	1	0	1	X	X	X	X	X	128
SG7	S24 - S27	0	1	1	0	X	X	X	X	X	128
SG8	S28 - S31	0	1	1	1	X	X	X	X	X	128
SG9	S32 - S35	1	0	0	0	X	X	X	X	X	128
SG10	S36 - S39	1	0	0	1	X	X	X	X	X	128
SG11	S40 - S43	1	0	1	0	X	X	X	X	X	128
SG12	S44 - S47	1	0	1	1	X	X	X	X	X	128
SG13	S48 - S51	1	1	0	0	X	X	X	X	X	128
SG14	S52 - S55	1	1	0	1	X	X	X	X	X	128
SG15	S56 - S59	1	1	1	0	X	X	X	X	X	128
SG16	S60 - S62	1	1	1	1	0	0	X	X	X	96
		1	1	1	1	0	1	X	X	X	
		1	1	1	1	1	0	X	X	X	
SG17	S63	1	1	1	1	1	1	0	X	X	16
SG18	S64	1	1	1	1	1	1	1	0	0	4
SG19	S65	1	1	1	1	1	1	1	0	1	4
SG20	S66	1	1	1	1	1	1	1	1	X	8

Table 7. Sector Groups - Bottom Boot Version

Group	Sectors (Table 2)	Group Address A[20:12]									Block Size (KWords)
SG0	S0	0	0	0	0	0	0	0	0	X	8
SG1	S1	0	0	0	0	0	0	0	1	0	4
SG2	S2	0	0	0	0	0	0	0	1	1	4
SG3	S3	0	0	0	0	0	0	1	X	X	16
SG4	S4 - S6	0	0	0	0	0	1	X	X	X	96
		0	0	0	0	1	0	X	X	X	
		0	0	0	0	1	1	X	X	X	
SG5	S7 - S10	0	0	0	1	X	X	X	X	X	128
SG6	S11 - S14	0	0	1	0	X	X	X	X	X	128
SG7	S15 - S18	0	0	1	1	X	X	X	X	X	128
SG8	S19 - S22	0	1	0	0	X	X	X	X	X	128
SG9	S23 - S26	0	1	0	1	X	X	X	X	X	128
SG10	S27 - S30	0	1	1	0	X	X	X	X	X	128
SG11	S31 - S34	0	1	1	1	X	X	X	X	X	128
SG12	S35 - S38	1	0	0	0	X	X	X	X	X	128
SG13	S39 - S42	1	0	0	1	X	X	X	X	X	128
SG14	S43 - S46	1	0	1	0	X	X	X	X	X	128
SG15	S47 - S50	1	0	1	1	X	X	X	X	X	128
SG16	S51 - S54	1	1	0	0	X	X	X	X	X	128
SG17	S55 - S58	1	1	0	1	X	X	X	X	X	128
SG18	S59 - S62	1	1	1	0	X	X	X	X	X	128
SG19	S63 - S65	1	1	1	1	0	0	X	X	X	96
		1	1	1	1	0	1	X	X	X	
		1	1	1	1	1	0	X	X	X	
SG20	S66	1	1	1	1	1	1	X	X	X	32

viously protected sector groups. This function can be implemented either in-system or by using programming equipment. Note that to unprotect any sector, all unprotected sector groups must first be protected prior to the first sector unprotect write cycle. *Also, the unprotect procedure will cause all sectors to become unprotected, thus, sector groups that require protection must be protected again after the unprotect procedure is run.*

This procedure requires V_{ID} on the RESET# pin and uses standard microprocessor bus cycle timing to implement sector unprotection. The flow chart in Figure 4 illustrates the algorithm.

Temporary Sector Unprotect Operation

This feature allows temporary unprotection of previously protected sector groups to allow changing the data in-system. Temporary Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. While in this mode, formerly protected sectors can be programmed or erased by invoking the appropriate commands (see Device Commands section). Once V_{ID} is removed from RESET#, all the previously protected sector groups are protected again. Figure 5 illustrates the algorithm.

NOTE: If WP#/ACC = V_{IL}, the boot sectors remain protected.

Electronic ID Operation (High Voltage Method)

The Electronic ID mode provides manufacturer and device identification, sector protection verification and Sec[2] region protection status through identifier codes output on DQ[15:0]. This mode is intended primarily for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm.

Two methods are provided for accessing the Electronic ID data. The first requires V_{ID} on address pin A[9], with additional requirements for obtain-

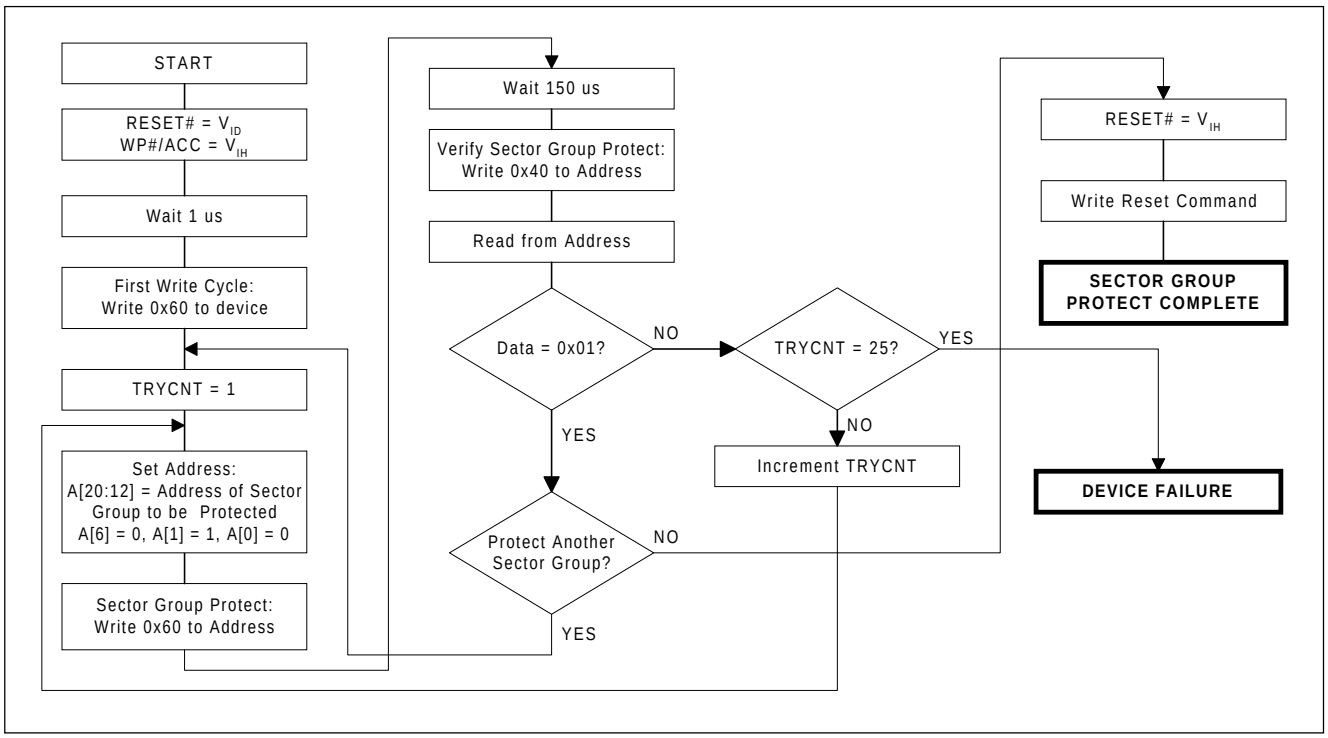


Figure 3. Sector Group Protect Algorithm

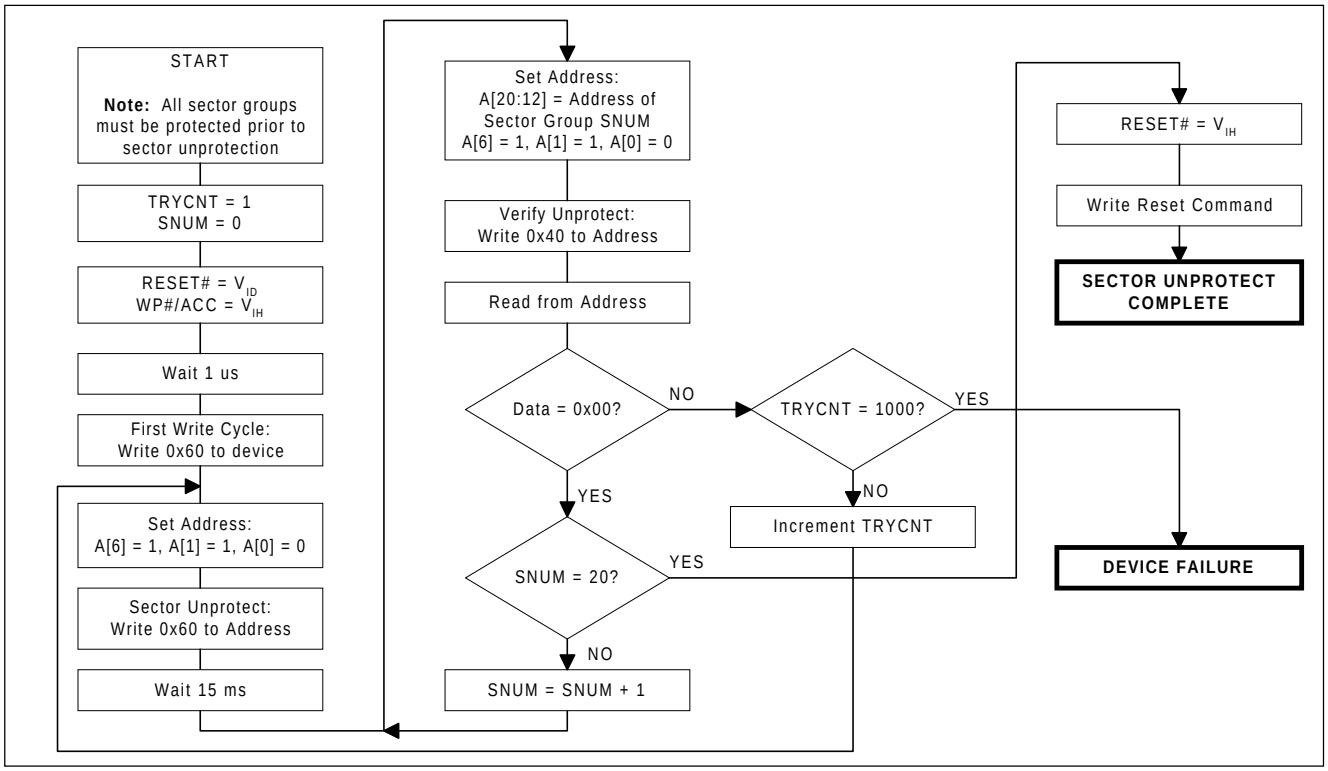


Figure 4. Sector Unprotect Algorithm

ing specific data items listed in Table 5. The Electronic ID data can also be obtained by the host through specific commands issued via the command register, as described later in the 'Device Commands' section of this data sheet.

While in the high-voltage Electronic ID mode, the system may read at specific addresses to obtain certain device identification and status information:

- A read cycle at address 0xXXX00 retrieves the manufacturer code.
- A read cycle at address 0xXXX01 returns the device code.
- A read cycle containing a sector address (SA) in A[20:12] and the address 0x04 in A[7:0] returns 0x01 if that sector is protected, or 0x00 if it is unprotected.
- A read cycle at address 0xXXX03 returns 0x80 if the Sec[2] region is protected and locked at the factory and 0x00 if it is not.

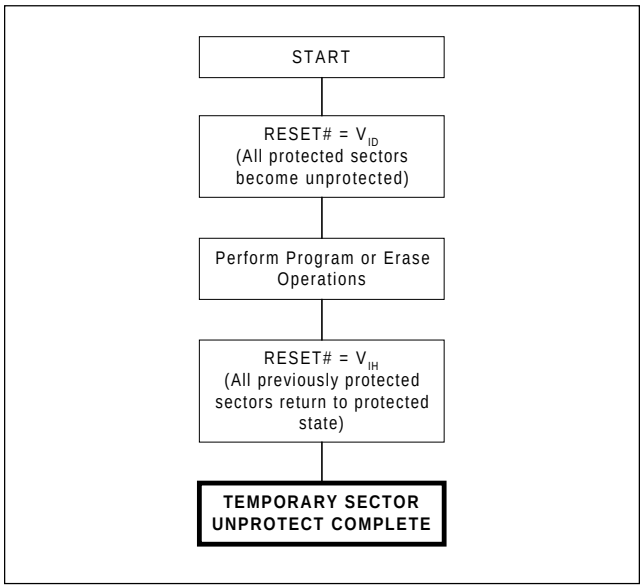


Figure 5. Temporary Sector Unprotect Algorithm

DEVICE COMMANDS

Device operations are initiated by writing designated address and data *command sequences* into the device. Commands are routed to the command register for execution. This register is automatically selected as the destination for all write operations and does not need to be explicitly addressed. Addresses are latched on the falling edge of WE# or CE#, whichever happens later. Data is latched on the rising edge of WE# or CE#, whichever happens first.

A command sequence is composed of one, two or three of the following sub-segments: an *unlock cycle*, a *command cycle* and a *data cycle*. Table 8 summarizes the composition of the valid command sequences implemented in the HY29LV320, and these sequences are fully described in Table 9 and in the sections that follow.

Writing incorrect address and data values or writing them in the improper sequence resets the device to the Read mode.

Reading Data

The device automatically enters the read array mode after device power-up, after the RESET# input is asserted and upon the completion of certain commands. Commands are not required to

Table 8. Composition of Command Sequences

Command Sequence	Number of Bus Cycles		
	Unlock	Command	Data
Read	0	0	Note 1
Reset	0	1	0
Enter Sec[2] Region	2	1	0
Exit Sec[2] Region	2	1	1
Program	2	1	1
Unlock Bypass	2	1	0
Unlock Bypass Reset	0	1	1
Unlock Bypass Program	0	1	1
Chip Erase	4	1	1
Sector Erase	4	1	1 (Note 2)
Erase Suspend	0	1	0
Erase Resume	0	1	0
Electronic ID	2	1	Note 3
CFI Query	0	1	Note 4

Notes:
1. Any number of Flash array read cycles are permitted.
2. Additional data cycles may follow. See text.
3. Any number of Electronic ID read cycles are permitted.
4. Any number of CFI data read cycles are permitted.

retrieve data in this mode. See Read Operation section for additional information.

After the device accepts an Erase Suspend command, the HY29LV320 enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

Reset Command

Writing the Reset command resets the sectors to the Read or Erase-Suspend mode. Address bits are don't cares for this command.

As described above, a Reset command is not normally required to begin reading array data. However, a Reset command must be issued in order to read array data in the following cases:

- If the device is in the Electronic ID mode, a Reset command must be written to return to the Read array mode. If the device was in the Erase Suspend mode when the device entered the Electronic ID mode, writing the Reset command returns the device to the Erase Suspend mode.

  Note: When in the Electronic ID bus operation mode, the device returns to the Read array mode when V_{ID} is removed from the A[9] pin. The Reset command is not required in this case.

- If the device is in the CFI Query mode, a Reset command must be written to return to the array Read mode.

- If DQ[5] (Exceeded Time Limit) goes High during a program or erase operation, a Reset command must be invoked to return the sectors to the Read mode (or to the Erase Suspend mode if the device was in Erase Suspend when the Program command was issued).

The Reset command may also be used to abort certain command sequences:

- In a Sector Erase or Chip Erase command sequence, the Reset command may be written at any time before erasing actually begins, including, for the Sector Erase command, between the cycles that specify the sectors to be erased (see Sector Erase command description). This aborts the command and resets the device to the Read mode. Once erasure begins, however, the device ignores the Reset command until the operation is complete.

- In a Program command sequence, the Reset command may be written between the sequence cycles before programming actually begins. This aborts the command and resets the device to the Read mode, or to the Erase Suspend mode if the Program command sequence is written while the device is in the Erase Suspend mode. Once programming begins, however, the device ignores the Reset command until the operation is complete.

- The Reset command may be written between the cycles in an Electronic ID command sequence to abort that command. As described above, once in the Electronic ID mode, the Reset command *must* be written to return to the array Read mode.

  Note: The Reset command does not return the device from Sec^2 Region access to normal array access. See descriptions of Enter/Exit Sec^2 Region commands for additional information.

Enter/Exit Sec^2 Region Command Sequences

The system can access the Sec^2 region of the device by issuing the Enter Sec^2 Region Command sequence. The device continues to access the Sec^2 region until the system issues the Exit Sec^2 Region Command sequence, which returns the device to normal operation.

Note that a hardware reset will reset the device to the Read Array mode.

Program Command Sequence

The system programs the device a word at a time by issuing the appropriate four-cycle Program Command sequence as shown in Table 9. The sequence begins by writing two unlock cycles, followed by the program setup command and, lastly, the program address and data. This initiates the Automatic Program algorithm that automatically provides internally generated program pulses and verifies the programmed cell margin. The host is not required to provide further controls or timings during this operation. When the Automatic Program algorithm is complete, the device returns to the reading array data mode. Several methods are provided to allow the host to determine the

Table 9. HY29LV320 Command Sequences

Command Sequence		Write Cycles	Bus Cycles [1, 2, 3, 4] First Add	First Data	Second Add	Second Data	Third Add	Third Data	Fourth Add	Fourth Data	Fifth Add	Fifth Data	Sixth Add	Sixth Data
Read		0	RA	RD										
Reset [7]		1	XXX	F0										
Enter Sec [2] Region		3	555	AA	2AA	55	555	88						
Exit Sec [2] Region		4	555	AA	2AA	55	555	90	XXX	00				
Normal Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Reset [6]		2	XXX	90	XXX	00								
Unlock Bypass Program [5]		2	XXX	A0	PA	PD								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase [9]		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend [7]		1	XXX	B0										
Erase Resume [8]		1	XXX	30										
Electronic ID [11]	Manufacturer Code	3	555	AA	2AA	55	555	90	XXX00	00AD				
	Device Code	3	555	AA	2AA	55	555	90	XXX01	Bottom Boot = 227D, Top Boot = 227E				
	Sector Protect Verify	3	555	AA	2AA	55	555	90	(SA)X02	XX00 = Unprotected Sector XX01 = Protected Sector				
	Sec[2] Region Indicator Bit	3	555	AA	2AA	55	555	90	XXX03	XX00 = NOT protected and locked at factory XX80 = Protected and locked at factory				
Common Flash Interface (CFI) Query [10]		1	XXX55	98										

Legend:

X = Don't Care
PA/PD = Memory address/data for the program operation
RA/RD = Memory address/data for the read operation
SA = A[20:12], sector address of the sector to be erased or verified (see Tables 1 and 2).

Notes:

1. All values are in hexadecimal.
2. All bus cycles are write operations except all cycles of the Read command and the fourth cycle of Electronic ID command.
3. Data bits DQ[15:8] are don't cares except for 'PD' in program cycles.
4. Address is A[10:0]. Other (upper) address bits are don't cares except when 'SA' or 'PA' is required.
5. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
6. The Unlock Bypass Reset command is valid only while the device is in the Unlock Bypass mode.
7. The Erase Suspend command is valid only during a sector erase operation. The system may read and program in non-erasing sectors, or enter the Electronic ID mode, while in the Erase Suspend mode.
8. The Erase Resume command is valid only during the Erase Suspend mode.
9. Multiple sectors may be specified for erasure. See command description.
10. See CFI section of specification for additional information.
11. See Electronic ID section of specification for additional information.

status of the programming operation, as described in the Write Operation Status section.

Commands written to the device during execution of the Automatic Program algorithm are ignored. Note that a hardware reset immediately terminates the programming operation (see Reset Operation Timings). To ensure data integrity, the user should reinitiate the aborted Program Command sequence after the reset operation is complete.

Programming is allowed in any sequence. Only erase operations can convert a stored “0” to a “1”. Thus, a bit cannot be *programmed* from a “0” back to a “1”. Attempting to do so will cause the HY29LV320 to halt the operation and set DQ[5] to “1”, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”.

Figure 6 illustrates the programming operation.

Unlock Bypass Command Sequence

Unlock bypass provides a faster method than the normal Program Command for the host system to program the array. As shown in Table 9, the Unlock Bypass Command sequence consists of two unlock write cycles followed by a third write cycle containing the unlock bypass command, 0x20. The device then enters Unlock Bypass mode. In this mode, a two-cycle Unlock Bypass Program Command sequence is used instead of the standard four-cycle sequence to invoke a programming operation. The first cycle in this sequence contains the unlock bypass program command, 0xA0, and the second cycle specifies the program address and data, thus eliminating the initial two unlock cycles required in the standard Program Command sequence. Additional data is programmed in the same manner. The unlock bypass mode does not affect normal read operations.

During the unlock bypass mode, only the Unlock Bypass Program and the Unlock Bypass Reset commands are valid. To exit the Unlock Bypass mode, the host must issue the two-cycle Unlock Bypass Reset command sequence shown in Table 9.

Figure 6 illustrates the procedures for the normal and unlock bypass program operations.

The device automatically enters the unlock bypass mode when it is placed in Accelerate mode via the ACC pin.

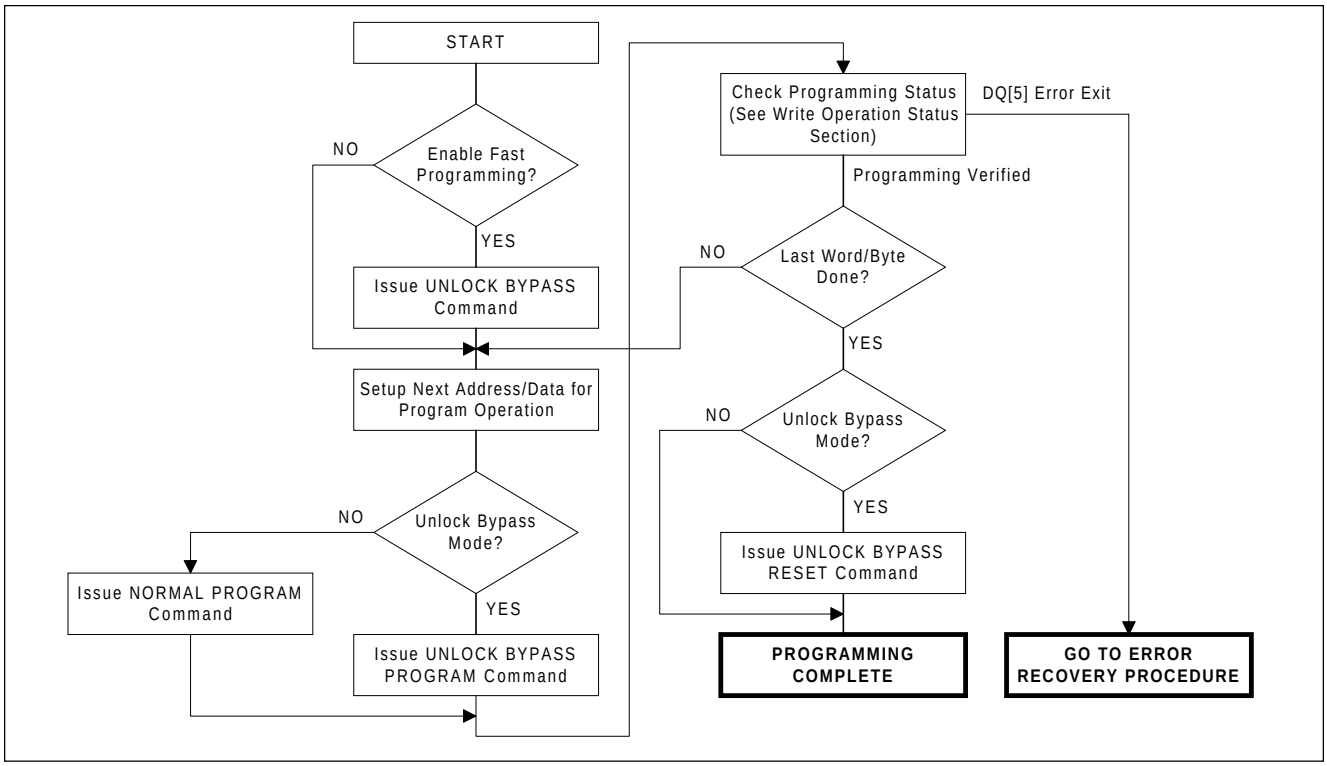


Figure 6. Normal and Unlock Bypass Programming Procedures

Chip Erase Command Sequence

The Chip Erase Command sequence consists of two unlock cycles, followed by a set-up command, two additional unlock cycles and then the Chip Erase Command. This sequence invokes the Automatic Chip Erase algorithm which automatically preprograms (if necessary) and verifies the entire memory for an all zero data pattern before electrical erase. The host system is not required to provide any controls or timings during these operations.

If all sectors in the device are protected, the device returns to reading array data after approximately 100 µs. If at least one sector is unprotected, the erase operation erases the unprotected sectors, and ignores the command for the sectors that are protected. Reads from the device during operation of the Automatic Chip Erase Algorithm return status data. See Write Operation Status section of this specification.

Commands written to the device during execution of the Automatic Chip Erase algorithm are ignored. Note that a hardware reset immediately terminates the chip erase operation (see Hardware Reset Timings). To ensure data integrity, the user should reinitiate the aborted Chip Erase Command sequence after the reset operation is complete.

When the Automatic Chip Erase algorithm is complete, the device returns to the reading array data mode. Several methods are provided to allow the host to determine the status of the erase operation, as described in the Write Operation Status section.

Figure 7 illustrates the chip erase procedure.

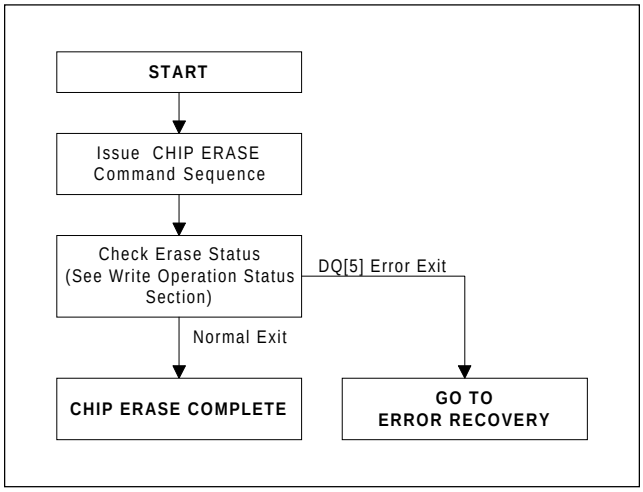


Figure 7. Chip Erase Procedure

Sector Erase Command Sequence

The Sector Erase Command sequence consists of two unlock cycles, followed by a set-up command, two additional unlock cycles and then the Sector Erase Command, which specifies which sector is to be erased. This sequence invokes the Automatic Sector Erase algorithm which automatically preprograms (if necessary) and verifies the specified sector for an all zero data pattern before electrical erase. The host system is not required to provide any controls or timings during these operations.

After the sector erase command cycle (sixth cycle) of the command sequence is issued, a sector erase time-out of 50 µs (min) begins, measured from the rising edge of the final WE# pulse in the command sequence. During this time, an additional sector address and Sector Erase Command may be written into an internal sector erase buffer. This buffer may be loaded in any sequence, and the number of sectors designated for erasure may be from one sector to all sectors. The only restriction is that the time between these additional cycles must be less than 50 µs, otherwise erasure may begin before the last address and command are accepted. To ensure that all commands are accepted, it is recommended that host processor interrupts be disabled during the time that the additional sector erase commands are being issued and then be re-enabled afterwards.

The system can monitor DQ[3] to determine if the 50 µs sector erase time-out has expired, as described in the Write Operation Status section. If the time between additional sector erase commands can be assured to be less than the time-out, the system need not monitor the timeout.

> **Note:** Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must then rewrite the command sequence, including any additional sector addresses and commands. Once the sector erase operation itself has begun, only the Erase Suspend command is valid. All other commands are ignored.

As for the chip erase command, note that a hardware reset immediately terminates the erase operation (see Hardware Reset Timings). To ensure data integrity, the aborted sector erase command sequence should be reissued once the reset operation is complete.

If all sectors designated for erasing are protected, the device returns to reading array data after approximately 100 µs. If at least one designated sector is unprotected, the erase operation erases the unprotected sectors, and ignores the command for the sectors that are protected. Read array operations cannot take place until the Automatic Erase algorithm terminates, or until the erase operation is suspended. Read operations while the algorithm is in progress provide status data. When the Automatic Erase algorithm is complete, the device returns the erased sector(s) to the Read (array data) mode.

Several methods are provided to allow the host to determine the status of the erase operation, as described in the Write Operation Status section.

Figure 8 illustrates the sector erase procedure.

Erase Suspend/Erase Resume Commands

The erase suspend command allows the system to interrupt a sector erase operation to program data into, or to read data from, any sector not designated for erasure. The command causes the erase operation to be suspended in all sectors designated for erasure. This command is valid only during the sector erase operation, including during the 50 µs time-out period at the end of the command sequence, and is ignored if it is issued during chip erase or programming operations.

The HY29LV320 requires a maximum of 20 µs to suspend the erase operation if the erase suspend command is issued during active sector erasure. However, if the command is written during the sector erase time-out, the time-out is terminated and the erase operation is suspended immediately. Once the erase operation has been suspended, the system can read array data from or program data into any sector that is not designated for erasure (protected sectors cannot be programmed). Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ[7:0]. The host can use DQ[7], or DQ[6] and DQ[2] together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspended read state and the host can initiate another programming operation (or read operation) within non-suspended sectors. The host can determine the status of a program operation during the erase-suspended state just as in the standard programming operation.

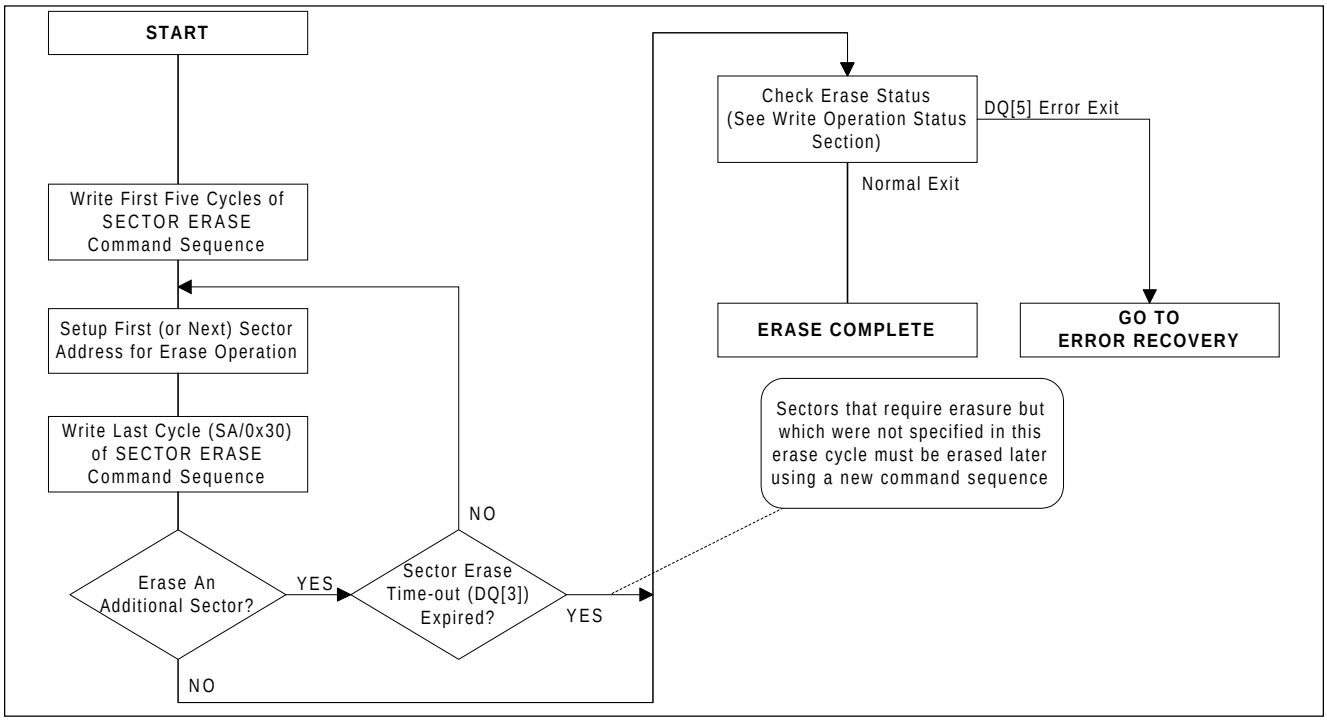


Figure 8. Sector Erase Procedure

The host may also write the Electronic ID Command sequence when the chip is in the Erase Suspend mode. The device allows reading Electronic ID codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the Electronic ID mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See Electronic ID Mode section for more information.

The system must write the Erase Resume command to exit the Erase Suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

> **Note**: If an erase operation is started while in the Sec[2] region and then suspended to do other operations, the host must return the device to the Sec[2] region before issuing the Erase Resume command. Failure to do this may result in the wrong sector being erased.

Electronic ID Command

The Electronic ID mode provides manufacturer and device identification and sector protection verification through identifier codes output on DQ[15:0]. This mode is intended primarily for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm.

Two methods are provided for accessing the Electronic ID data. The first requires V_{ID} on address pin A[9], as described previously in the Device Operations section.

The Electronic ID data can also be obtained by the host through specific commands issued via the command register, as shown in Table 9. This method does not require V_{ID}. The Electronic ID command sequence may be issued while the device is in the Read mode or in the Erase Suspend Read mode. The command may not be written while the device is actively programming or erasing.

The Electronic ID command sequence is initiated by writing two unlock cycles, followed by a third write cycle that contains the Electronic ID command. The device then enters the Electronic ID mode, and the system may read at any address any number of times without initiating another command sequence.

- A read cycle at address 0xXXX00 retrieves the manufacturer code.
- A read cycle at address 0xXXX01 in returns the device code.
- A read cycle containing a sector address (SA) in A[20:12] and the address 0x02 in A[7:0] returns 0x01 if that sector is protected, or 0x00 if it is unprotected.
- A read cycle at address 0xXXX03 returns 0x80 if the Sec[2] region is protected and locked at the factory and returns 0x00 if it is not.

The system must write the Reset command to exit the Electronic ID mode and return the bank to the normal Read mode, or to the Erase-Suspended read mode if the device was in that mode when the Electronic ID command was invoked. In the latter case, an Erase Resume command to that bank will continue the suspended erase operation.

Query Command and Common Flash Interface (CFI) Mode

The HY29LV320 is capable of operating in the Common Flash Interface (CFI) mode. This mode allows the host system to determine the manufacturer of the device, its operating parameters, its configuration and any special command codes that the device may accept. With this knowledge, the system can optimize its use of the chip by using appropriate timeout values, optimal voltages and commands necessary to use the chip to its full advantage.

Two commands are employed in association with CFI mode. The first places the device in CFI mode (Query command) and the second takes it out of CFI mode (Reset command). These are described in Table 10.

The single cycle Query command is valid only when the device is in the Read mode, including during Erase Suspend and Standby states and while in Electronic ID command mode, but is ignored otherwise. The command is not valid while the HY29LV320 is in the Electronic ID bus operation mode. Read cycles at appropriate addresses while in the Query mode provide CFI data as described later in this section. Write cycles are ignored, except for the Reset command.

The Reset command returns the device from the CFI mode to the array Read mode (even if it was

in the Electronic ID mode when the Query command was issued), or to the Erase Suspend mode if the device was in that mode prior to entering CFI mode. The Reset command is valid only when the device is in the CFI mode and as otherwise described for the normal Reset command.

Tables 10 - 13 specify the data provided by the HY29LV320 during CFI mode. Data at unspecified addresses reads out as 0x00. Note that a value of 0x00 for a data item normally indicates that the function is not supported. All values in these tables are in hexadecimal notation.

Table 10. CFI Mode: Identification Data Values

Description	Address	Data
Query-unique ASCII string "QRY"	10 11 12	0051 0052 0059
Primary vendor command set and control interface ID code	13 14	0002 0000
Address for primary algorithm extended query table	15 16	0040 0000
Alternate vendor command set and control interface ID code (none)	17 18	0000 0000
Address for secondary algorithm extended query table (none)	19 1A	0000 0000

Table 11. CFI Mode: System Interface Data Values

Description	Address	Data
V_{CC} supply, minimum (2.7V)	1B	0027
V_{CC} supply, maximum (3.6V)	1C	0036
V_{PP} supply, minimum (none)	1D	0000
V_{PP} supply, maximum (none)	1E	0000
Typical timeout for single word/byte write (2^N µs)	1F	0004
Typical timeout for maximum size buffer write (2^N µs)	20	0000
Typical timeout for individual block erase (2^N ms)	21	0009
Typical timeout for full chip erase (2^N ms)	22	000F
Maximum timeout for single word/byte write (2^N x Typ)	23	0005
Maximum timeout for maximum size buffer write (2^N x Typ)	24	0000
Maximum timeout for individual block erase (2^N x Typ)	25	0004
Maximum timeout for full chip erase (not supported)	26	0000

Table 12. CFI Mode: Device Geometry Data Values

Description	Address	Data
Device size (2^N bytes)	27	0016
Flash device interface code (01 = asynchronous x16)	28 29	0001 0000
Maximum number of bytes in multi-byte write (not supported)	2A 2B	0000 0000
Number of erase block regions	2C	0004
Erase block region 1 information [2E, 2D] = # of blocks in region - 1 [30, 2F] = size in multiples of 256-bytes	2D 2E 2F 30	0000 0000 0040 0000
Erase block region 2 information	31 32 33 34	0001 0000 0020 0000
Erase block region 3 information	35 36 37 38	0000 0000 0080 0000
Erase block region 4 information	39 3A 3B 3C	003E 0000 0000 0001

Table 13. CFI Mode: Vendor-Specific Extended Query Data Values

Description	Address	Data
Query-unique ASCII string "PRI"	40 41 42	0050 0052 0049
Major version number, ASCII	43	0031
Minor version number, ASCII	44	0030
Address sensitive unlock (0 = required, 1 = not required)	45	0000
Erase suspend(2 = to read and write)	46	0002
Sector protect (N = # of sectors/group)	47	0001
Temporary sector unprotect (1 = supported)	48	0001
Sector protect/unprotect scheme (4 = Am29LV800A method)	49	0004
Simultaneous R/W operation (xx = number of sectors in Bank 2: 0 = not supported)	4A	0000
Burst mode type (0 = not supported)	4B	0000
Page mode type (0 = not supported)	4C	0000
ACC Supply minimum (11.5V)	4D	00B5
ACC Supply maximum (12.5V)	4E	00C5
Top/bottom boot version (BB = Bottom Boot, TB = Top Boot)	4F	0002 (BB) 0003 (TB)

WRITE OPERATION STATUS

The HY29LV320 provides a number of facilities to determine the status of a program or erase operation. These are the RY/BY# (Ready/Busy#) pin and certain bits of a status word which can be read from the device during the programming and erase operations. Table 11 summarizes the status indications and further detail is provided in the subsections which follow.

RY/BY# - Ready/Busy#

RY/BY# is an open-drain output pin that indicates whether a programming or erase Automatic Algorithm is in progress or has completed. A pull-up resistor to V_{CC} is required for proper operation. RY/BY# is valid after the rising edge of the final WE# pulse in the corresponding command sequence.

If the output is Low (busy), the device is actively erasing or programming, including programming while in the Erase Suspend mode. If the output is High (ready), the device has completed the operation and is ready to read array data in the normal or Erase Suspend modes, or it is in the Standby mode.

DQ[7] - Data# Polling

The Data# (“Data Bar”) Polling bit, DQ[7], indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend mode. Data# Polling is valid after the rising edge of the final WE# pulse in the Program or Erase command sequence.

The system must do a read at the program address to obtain valid programming status information on this bit. While a programming operation is in progress, the device outputs the complement of the value programmed to DQ[7]. When the programming operation is complete, the device outputs the value programmed to DQ[7]. If a program operation is attempted within a protected sector, Data# Polling on DQ[7] is active for approximately 1 µs, then the device returns to reading array data.

The host must read at an address within any non-protected sector specified for erasure to obtain valid erase status information on DQ[7]. During an erase operation, Data# Polling produces a “0” on DQ[7]. When the erase operation is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ[7]. If all sectors selected for erasing are protected, Data# Polling on DQ[7] is active for approximately 100 µs, then the device returns to reading array data. If at least one selected sector is not protected, the erase operation erases the unprotected sectors,

Table 14. Write and Erase Operation Status Summary [1]

Mode	Operation	DQ[7]	DQ[6]	DQ[5]	DQ[3]	DQ[2]	RY/BY#
Normal	Programming in progress	DQ[7]#	Toggle	0/1 [2]	N/A	N/A	0
	Programming completed	Data	Data [4]	Data	Data	Data	1
	Erase in progress	0	Toggle	0/1 [2]	1 [3]	Toggle	0
	Erase completed [5]	Data	Data [4]	Data	Data	Data [4]	1
Erase Suspend	Read within erase suspended sector	1	No toggle	0	N/A	Toggle	1
	Read within non-erase suspended sector	Data	Data	Data	Data	Data	1
	Programming in progress [6]	DQ[7]#	Toggle	0/1 [2]	N/A	N/A	0
	Programming completed [6]	Data	Data [4]	Data	Data	Data	1

Notes:
1. A valid address is required when reading status information (except RY/BY#). For a programming operation, the address used for the read cycle should be the program address. For an erase operation, the address used for the read cycle should be any address within a non-protected sector marked for erasure (any address within a non-protected sector for the chip erase operation).
2. DQ[5] status switches to a '1' when a program or erase operation exceeds the maximum timing limit.
3. A '1' during sector erase indicates that the 50 µs time-out has expired and active erasure is in progress. DQ[3] is not applicable to the chip erase operation.
4. Equivalent to 'No Toggle' because data is obtained in this state.
5. Data (DQ[7:0]) = 0xFF immediately after erasure.
6. Programming can be done only in a non-suspended sector (a sector not specified for erasure).

and ignores the command for the specified sectors that are protected.

When the system detects that DQ[7] has changed from the complement to true data (or "0" to "1" for erase), it should do an additional read cycle to read valid data from DQ[7:0]. This is because DQ[7] may change asynchronously with respect to the other data bits while Output Enable (OE#) is asserted low.

Figure 9 illustrates the Data# Polling test algorithm.

DQ[6] - Toggle Bit I

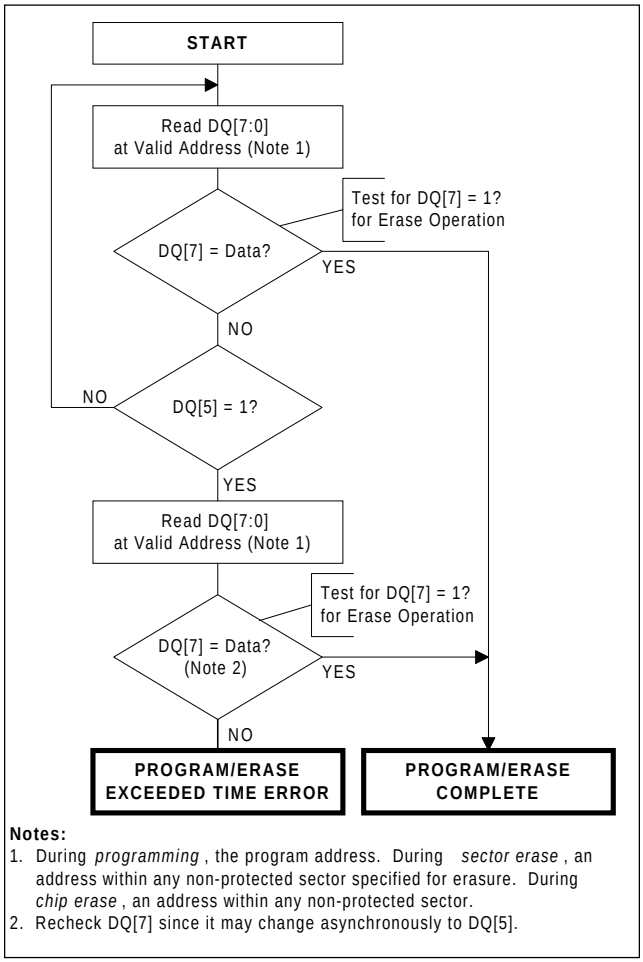
Toggle Bit I on DQ[6] indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the Program or Erase command sequence, including during the sector erase time-out. The system may use either OE# or CE# to control the read cycles.

Successive read cycles at any address during an Automatic Program algorithm operation (including programming while in Erase Suspend mode) cause DQ[6] to toggle. DQ[6] stops toggling when the operation is complete. If a program address falls within a protected sector, DQ[6] toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

While the Automatic Erase algorithm is operating, successive read cycles at any address cause DQ[6] to toggle. DQ[6] stops toggling when the erase operation is complete or when the device is placed in the Erase Suspend mode. The host may use DQ[2] to determine which sectors are erasing or erase-suspended (see below). After an Erase command sequence is written, if all sectors selected for erasing are protected, DQ[6] toggles for approximately 100 µs, then returns to reading array data. If at least one selected sector is not protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

DQ[2] - Toggle Bit II

Toggle Bit II, DQ[2], when used with DQ[6], indicates whether a particular sector is actively erasing or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. The device toggles DQ[2] with each OE# or CE# read cycle.



Notes:
1. During *programming* , the program address. During *sector erase* , an address within any non-protected sector specified for erasure. During *chip erase* , an address within any non-protected sector.
2. Recheck DQ[7] since it may change asynchronously to DQ[5].

Figure 9. Data# Polling Test Algorithm

DQ[2] toggles when the host reads at addresses within sectors that have been specified for erasure, but cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ[6], by comparison, indicates whether the device is actively erasing or is in Erase Suspend, but cannot distinguish which sectors are specified for erasure. Thus, both status bits are required for sector and mode information.

Figure 10 illustrates the operation of Toggle Bits I and II.

DQ[5] - Exceeded Timing Limits

DQ[5] is set to a '1' when the program or erase time has exceeded a specified internal pulse count limit. This is a failure condition that indicates that the program or erase cycle was not successfully completed. DQ[5] status is valid only while DQ[7] or DQ[6] indicate that the Automatic Algorithm is in progress.

The DQ[5] failure condition will also be signaled if the host tries to program a '1' to a location that is previously programmed to '0', since only an erase operation can change a '0' to a '1'.

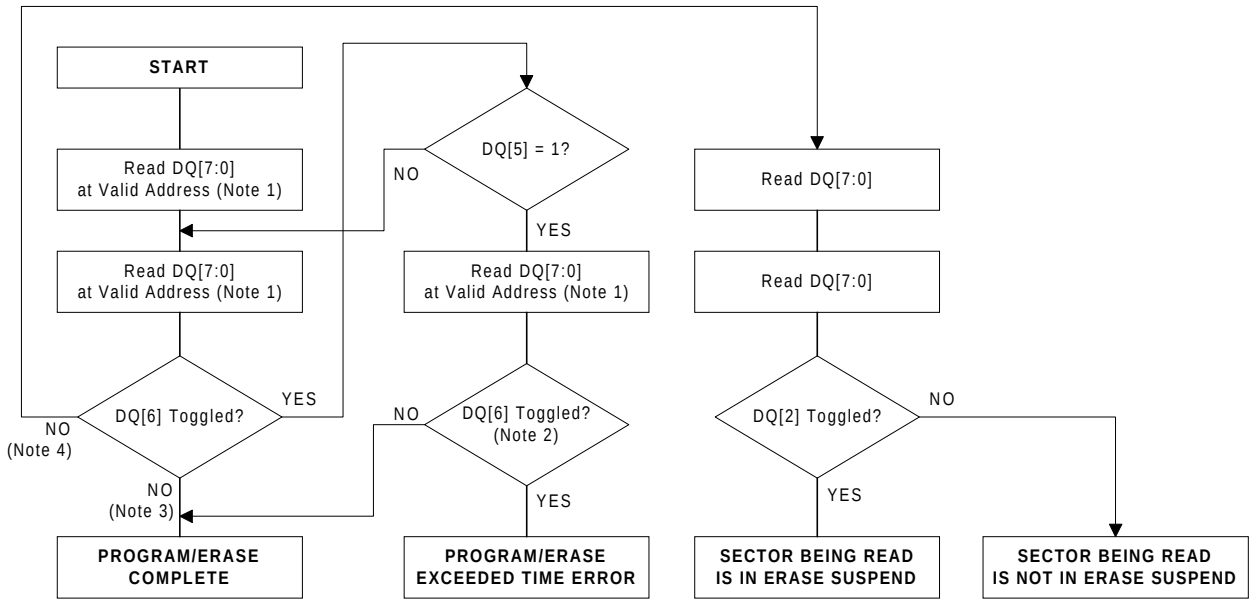
For both of these conditions, the host must issue a Reset command to return the device to the Read mode.

> **Note:** While DQ[5] indicates an error condition, no commands (except Reads) will be accepted by the device. If the device receives a command while DQ[5] is high, the first write cycle of that command will reset the error condition and the remaining write cycles of that command sequence will be ignored

DQ[3] - Sector Erase Timer

After writing a Sector Erase command sequence, the host may read DQ[3] to determine whether or not an erase operation has begun. When the sector erase time-out expires and the sector erase operation commences, DQ[3] switches from a '0' to a '1'. Refer to the "Sector Erase Command" section for additional information. Note that the sector erase timer does not apply to the Chip Erase command.

After the initial Sector Erase command sequence is issued, the system should read the status on DQ[7] (Data# Polling) or DQ[6] (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ[3]. If DQ[3] is a '1', the internally controlled erase cycle has begun and all further sector erase data cycles or commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ[3] is a '0', the device will accept a sector erase data cycle to mark an additional sector for erasure. To ensure that the data cycles have been accepted, the system software should check the status of DQ[3] prior to and following each subsequent sector erase data cycle. If DQ[3] is high on the second status check, the last data cycle might not have been accepted.



Notes:
1. During programming, the program address.
   During sector erase, an address within any sector scheduled for erasure.
2. Recheck DQ[6] since toggling may stop at the same time as DQ[5] changes from 0 to 1.
3. Use this path if testing for Program/Erase status.
4. Use this path to test whether sector is in Erase Suspend mode.

Figure 10. Toggle Bit I and II Test Algorithm

HARDWARE DATA PROTECTION

The HY29LV320 provides several methods of protection to prevent accidental erasure or programming which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise. These methods are described in the sections that follow.

Command Sequences

Commands that may alter array data require a sequence of cycles as described in Table 9. This provides data protection against inadvertent writes.

Low V_{CC} Write Inhibit

To protect data during V_{CC} power-up and power-down, the device does not accept write cycles when V_{CC} is less than V_{LKO} (typically 2.4 volts). The command register and all internal program/erase circuits are disabled, and the device resets to the Read mode. Writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by asserting any one of the following conditions: OE# = V_{IL} , CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the Read mode on power-up.

Sector Protection

Additional data protection is provided by the HY29LV320’s sector protect feature, described previously, which can be used to protect sensitive areas of the Flash array from accidental or unauthorized attempts to alter the data.

ABSOLUTE MAXIMUM RATINGS [4]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	ºC
T_{BIAS}	Ambient Temperature with Power Applied	-65 to +125	ºC
V_{IN2}	Voltage on Pin with Respect to V_{SS} : V_{CC} [1] A[9], OE#, WP#/ACC, RESET# [2] All Other Pins [1]	 -0.5 to +4.0 -0.5 to +12.5 -0.5 to (V_{CC} + 0.5)	 V V V
I_{OS}	Output Short Circuit Current [3]	200	mA

Notes:
1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0V for periods of up to 20 ns. See Figure 11. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 12.
2. Minimum DC input voltage on pins A[9], WP#/ACC, OE#, and RESET# is -0.5 V. During voltage transitions, A[9], WP#/ACC, OE#, and RESET# may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 11. Maximum DC input voltage on pins A[9], WP#/ACC, OE# and RESET# is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output at a time may be shorted to V_{SS}. Duration of the short circuit should be less than one second.
4. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: Commercial Temperature Devices Industrial Temperature Devices	 0 to +70 -40 to +85	 ºC ºC
V_{CC}	Operating Supply Voltage	Note 2	V

Notes:
1. Recommended Operating Conditions define those limits between which the functionality of the device is guaranteed.
2. See Valid Combinations table, page 43.

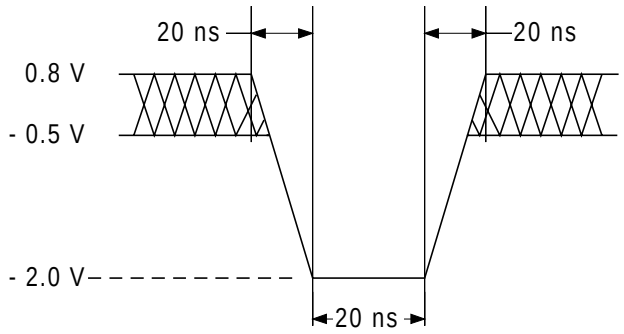


Figure 11. Maximum Undershoot Waveform

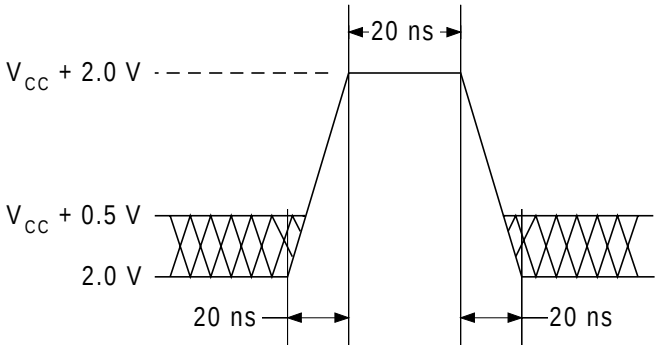


Figure 12. Maximum Overshoot Waveform

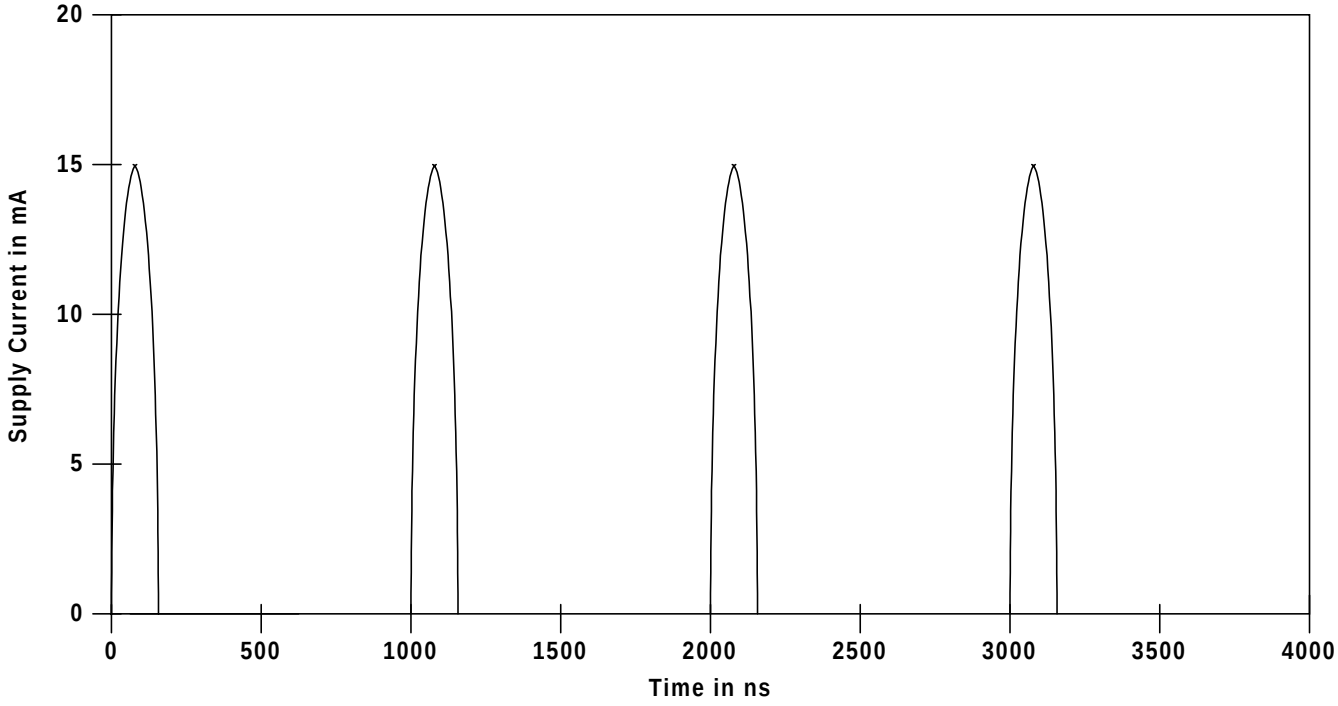
DC CHARACTERISTICS

Parameter	Description	Test Setup [2]		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}				±1.0	µA
I_{LIT}	A[9], Input Load Current	A[9] = 12.5V				35	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}				±1.0	µA
I_{CC1}	V_{CC} Active Read Current [1]	CE# = V_{IL}, OE# = V_{IH},	5 MHz		9	16	mA
			1 MHz		2	4	mA
I_{CC2}	V_{CC} Active Write Current [3, 4]	CE# = V_{IL}, OE# = V_{IH}			20	30	mA
I_{CC3}	V_{CC} CE# Controlled Deep Standby Current	CE# = V_{CC} ± 0.3 V, RESET# = V_{CC} ± 0.3 V, WP#/ACC = V_{CC} ± 0.3 V or V_{SS} ± 0.3 V			0.5	5	µA
I_{CC4}	V_{CC} RESET# Controlled Deep Standby Current	RESET# = V_{SS} ± 0.3 V, WP#/ACC = V_{CC} ± 0.3 V or V_{SS} ± 0.3 V			0.5	5	µA
I_{CC5}	Automatic Sleep Mode Current [5]	V_{IH} = V_{CC} ± 0.3 V, V_{IL} = V_{SS} ± 0.3 V			0.5	5	µA
I_{ACC}	Accelerated Program Current [4]	CE# = V_{IL} OE# = V_{IH}	V_{HH}		5	10	mA
			V_{CC}		15	30	mA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Electronic ID and Temporary Sector Unprotect	V_{CC} = 3.0V ± 10%		11.5		12.5	V
V_{HH}	Voltage for Program Acceleration	V_{CC} = 3.0V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	V_{CC} = V_{CC} Min, I_{OL} = 4.0 mA				0.45	V
V_{OH1}	Output High Voltage	V_{CC} = V_{CC} Min, I_{OH} = -2.0 mA		0.85 x V_{CC}			V
V_{OH2}		V_{CC} = V_{CC} Min, I_{OH} = -100 µA		V_{CC} - 0.4			V
V_{LKO}	Low V_{CC} Lockout Voltage [4]			2.3		2.5	V

Notes:
1. The I_{CC} current is listed is typically less than 2 mA/MHz with OE# at V_{IH}. Typical V_{CC} is 3.0 V.
2. All maximum current specifications are tested with V_{CC} = V_{CC} Max unless otherwise noted.
3. I_{CC} active while the Automatic Erase or Automatic Program algorithm is in progress.
4. Not 100% tested.
5. Automatic sleep mode is enabled when addresses remain stable for t_{ACC} + 50 ns (typical).

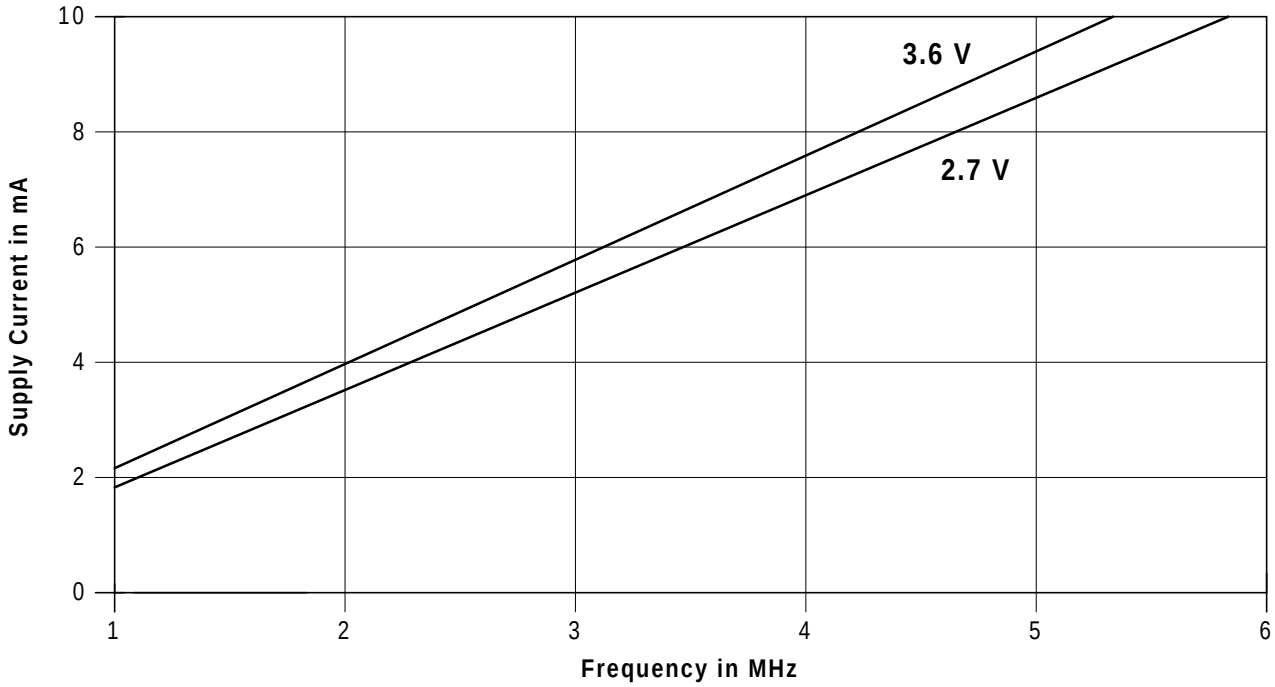
DC CHARACTERISTICS

Zero Power Flash



Note: Addresses are switching at 1 MHz.

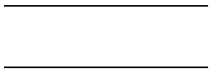
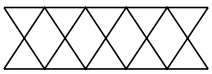
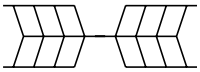
Figure 13. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: T_A = 25 °C.

Figure 14. Typical I_{CC1} Current vs. Frequency

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Centerline is High Impedance State (High Z)

TEST CONDITIONS

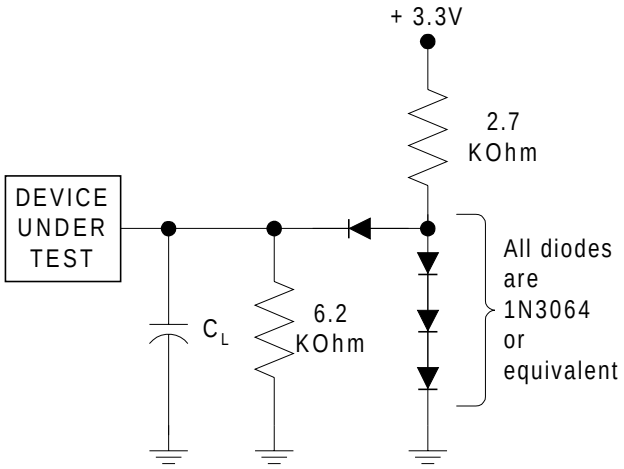


Figure 15. Test Setup

Table 15. Test Specifications

Test Condition	- 70	- 80 - 90 - 12	Unit
Output Load	1 TTL Gate		
Output Load Capacitance (C_L)	30	100	pF
Input Rise and Fall Times	5		ns
Input Signal Low Level	0.0		V
Input Signal High Level	3.0		V
Low Timing Measurement Signal Level	1.5		V
High Timing Measurement Signal Level	1.5		V

Note: Timing measurements are made at the reference levels specified above regardless of where the illustrations in the timing diagrams appear to indicate the measurements are made.

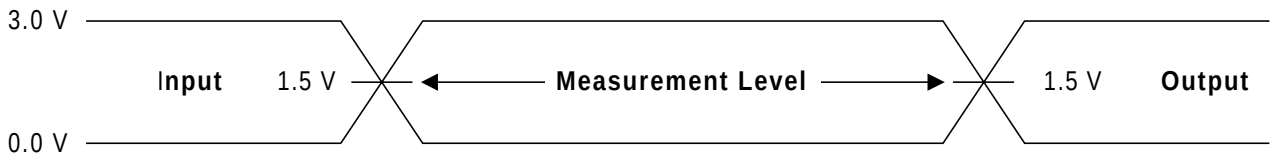


Figure 16. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Option				Unit
JEDEC	Std					- 70	- 80	- 90	- 12	
t_{AVAV}	t_{RC}	Read Cycle Time [1]			Min	70	80	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	80	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	80	90	120	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z [1]			Max	25	25	30	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		CE# = V_{IL}	Max	30	30	35	50	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z [1]			Max	25	30	30	30	ns
	t_{OEH}	Output Enable Hold Time [1]	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First [1]			Min	0				ns

Notes:
1. Not 100% tested.
2. See Figure 15 and Table 15 for test conditions.

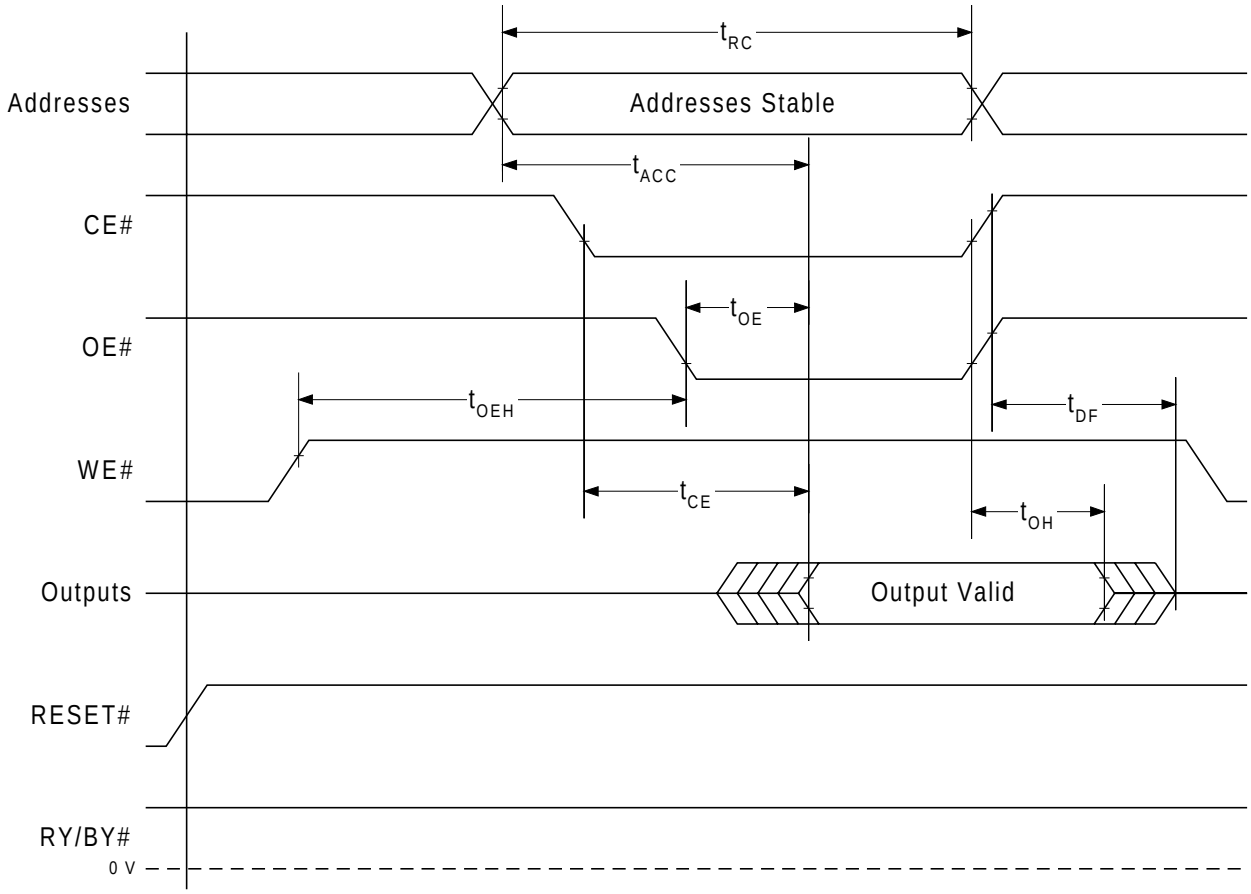


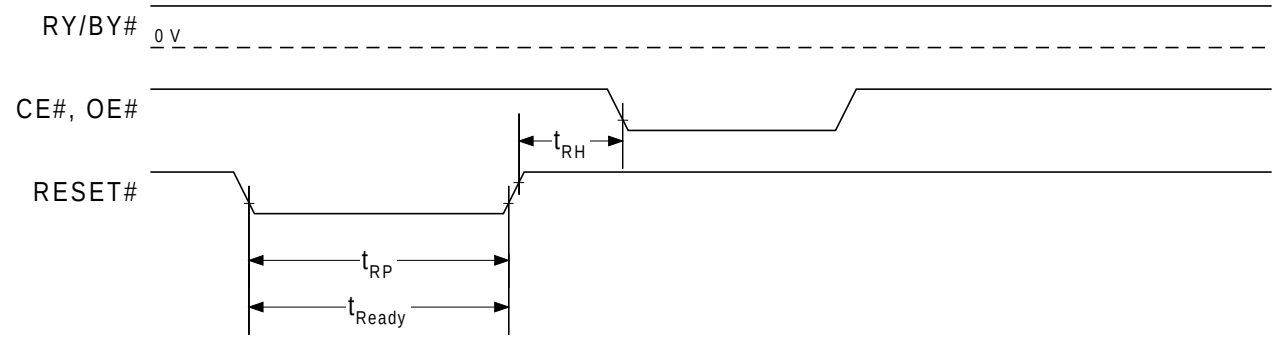
Figure 17. Read Operation Timings

AC CHARACTERISTICS

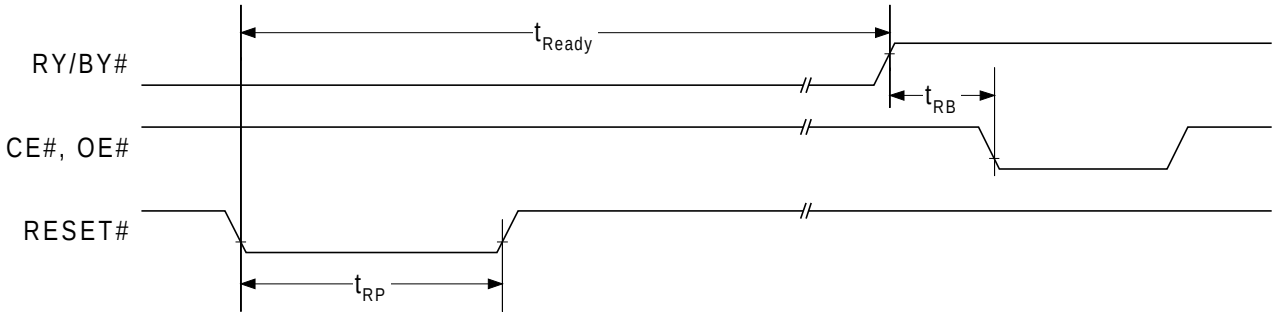
Hardware Reset (RESET#)

Parameter		Description	Test Setup		Speed Option				Unit
JEDEC	Std				- 70	- 80	- 90	- 12	
	t_{READY}	RESET# Pin Low (During Automatic Algorithms) to Read or Write [1]		Max	20				µs
	t_{READY}	RESET# Pin Low (NOT During Automatic Algorithms) to Read or Write [1]		Max	500				ns
	t_{RP}	RESET# Pulse Width		Min	500				ns
	t_{RH}	RESET# High Time Before Read [1]		Min	50				ns
	t_{RPD}	RESET# Low to Standby Mode		Max	20				µs
	t_{RB}	RY/BY# Recovery Time		Min	0				ns

Notes:
1. Not 100% tested.
2. See Figure 15 and Table 15 for test conditions.



Reset Timings NOT During Automatic Algorithms



Reset Timings During Automatic Algorithms

Figure 18. RESET# Timings

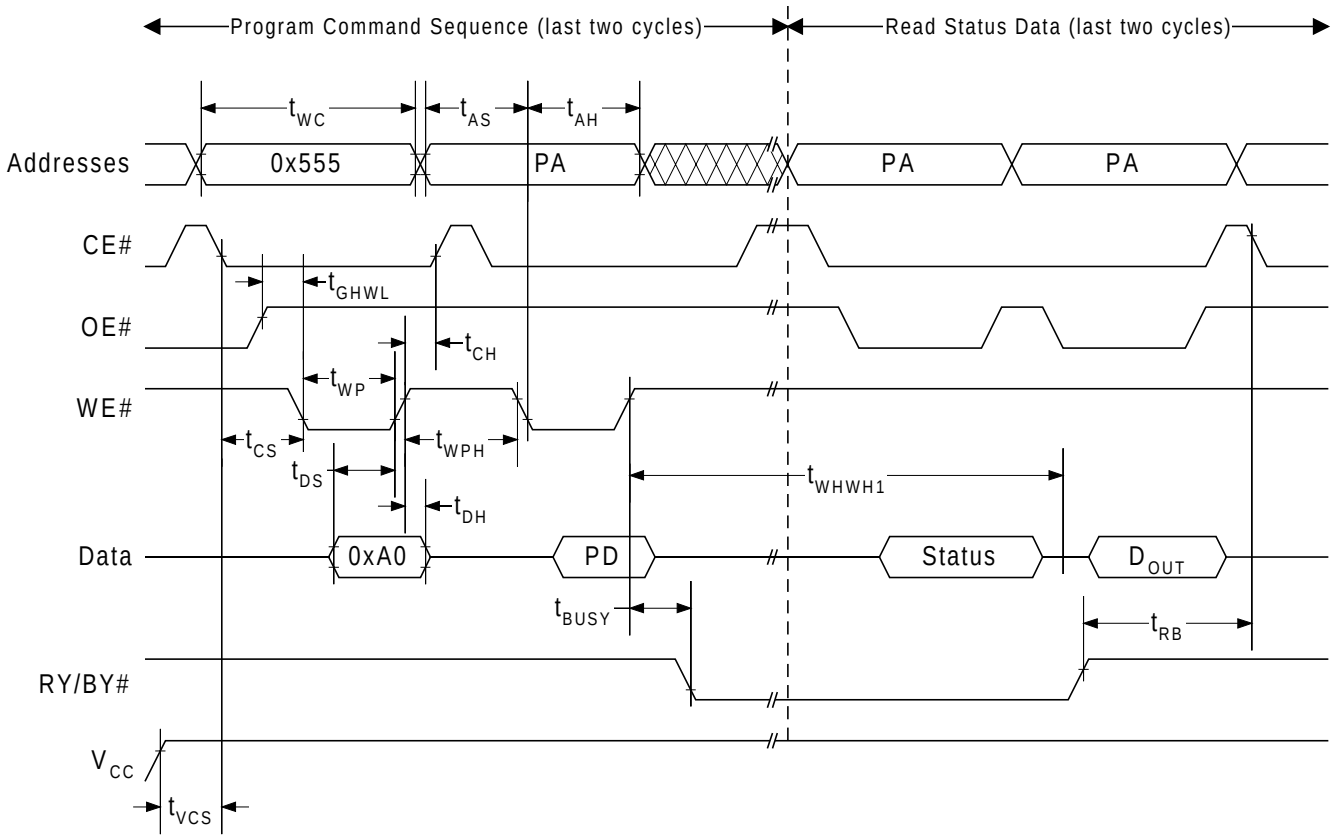
AC CHARACTERISTICS

Program and Erase Operations

Parameter		Description		Speed Option				Unit
JEDEC	Std			- 70	- 80	- 90	- 12	
t_{AVAV}	t_{WC}	Write Cycle Time [1]	Min	70	80	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
	t_{AST}	Address Setup Time to OE# or CE# Low for Toggle Bit Test	Min	15				ns
	t_{AHT}	Address Hold Time from OE# or CE# High for Toggle Bit Test	Min	0				ns
	t_{CEPH}	Chip Enable High Time for Toggle Bit Test	Min	20				ns
	t_{OEPH}	Output Enable High Time for Toggle Bit Test	Min	20				ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	45	45	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write	Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30				ns
t_{WHWH1}	t_{WHWH1}	Word Programming Operation [1, 2, 3]	Typ	11				µs
			Max	300				µs
		Chip Programming Operation [1, 2, 3, 5]	Typ	23				sec
			Max	70				sec
t_{WHWH1}	t_{WHWH1}	Accelerated Word Programming Operation [1, 2, 3]	Typ	7				µs
			Max	210				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation [1, 2, 4]	Typ	0.5				sec
			Max	7.5				sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation [1, 2, 4]	Typ	32				sec
		Erase and Program Cycle Endurance [1]	Min	100,000				cycles
			Typ	1,000,000				cycles
	t_{VCS}	V_{CC} Setup Time [1]	Min	50				µs
	t_{VHH}	V_{HH} Rise and Fall Time [1]	Min	250				ns
	t_{RB}	Recovery Time from RY/BY#	Min	0				ns
	t_{BUSY}	WE# High to RY/BY# Delay	Min	90				ns

Notes:

1. Not 100% tested.
2. Typical program and erase times assume the following conditions: 25 °C, V_{CC} = 3.0 volts, 100,000 cycles. In addition, programming typicals assume a checkerboard pattern. Maximum program and erase times are under worst case conditions of 90 °C, V_{CC} = 2.7 volts (3.0 volts for - 70 version), 100,000 cycles.
3. Excludes system-level overhead, which is the time required to execute the four-bus-cycle sequence for the program command. See Table 9 for further information on command sequences.
4. Excludes 0x00 programming prior to erasure. In the preprogramming step of the Automatic Erase algorithm, all bytes are programmed to 0x00 before erasure.
5. The typical chip programming time is considerably less than the maximum chip programming time listed since most words program faster than the maximum programming times specified. The device sets DQ[5] = 1 only If the maximum word program time specified is exceeded. See Write Operation Status section for additional information.



Notes:
1. PA = Program Address, PD = Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 19. Program Operation Timings

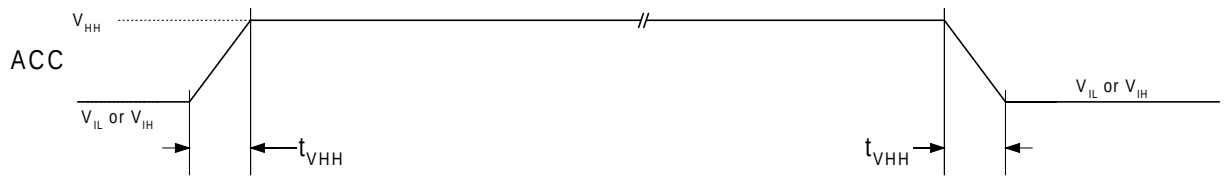
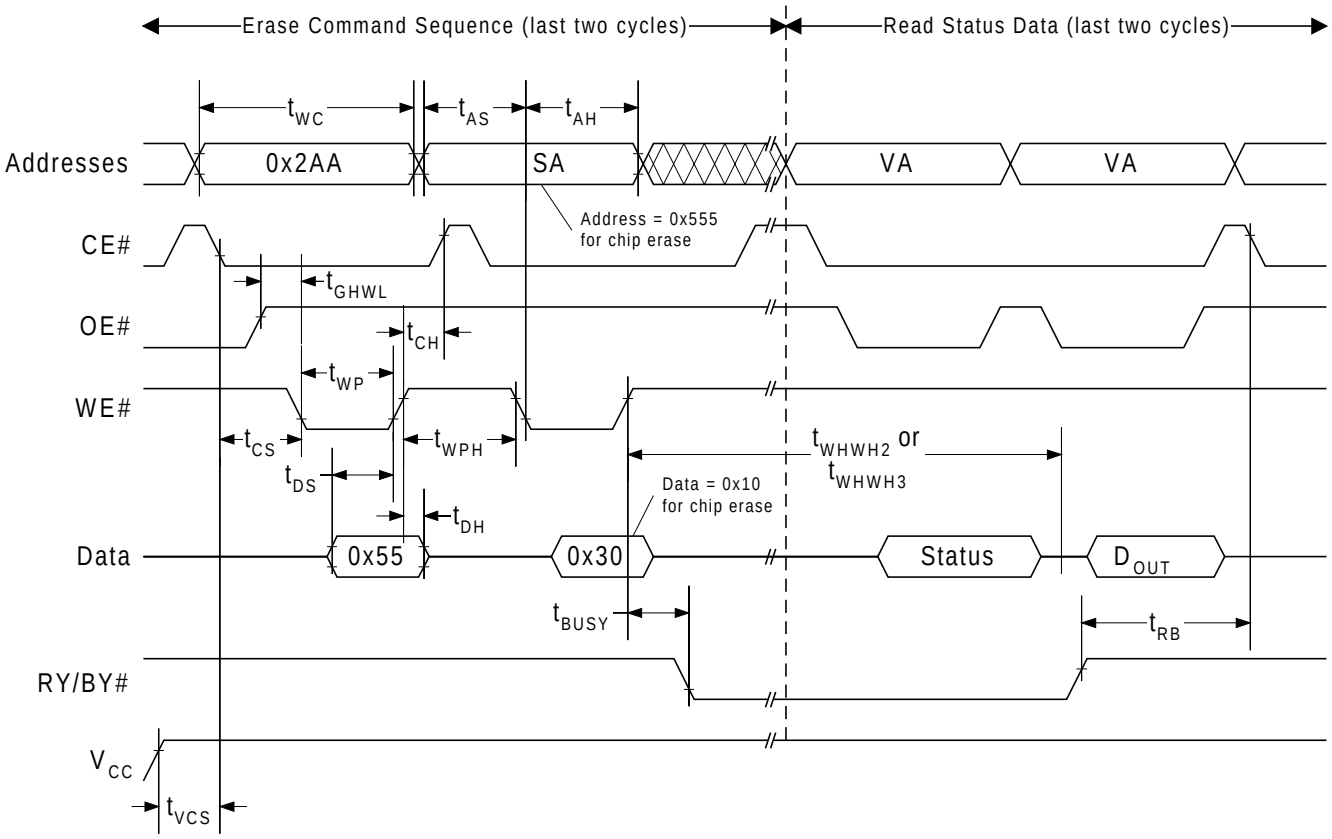


Figure 20. Accelerated Programming Voltage Timings

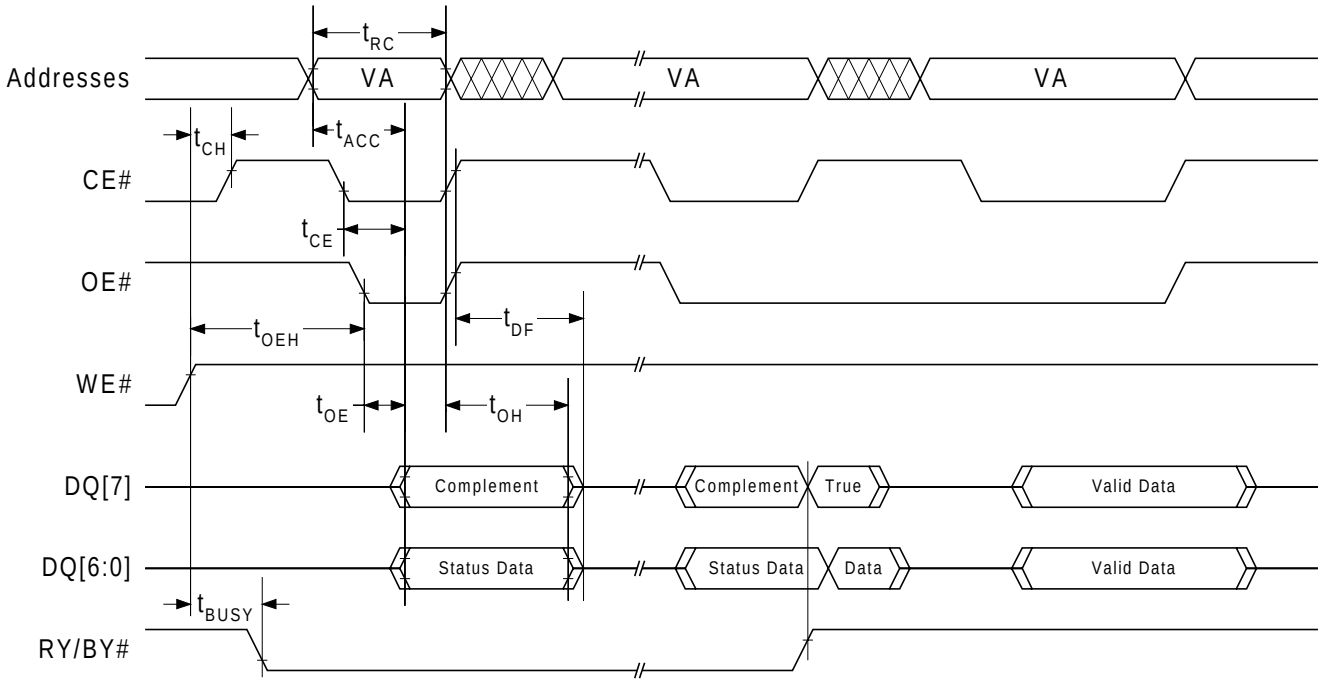
AC CHARACTERISTICS



Notes:
1. SA =Sector Address (for sector erase), VA = Valid Address for reading status data (see Write Operation Status section), D_{OUT} is the true data at the read address.(0xFF after an erase operation).
2. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

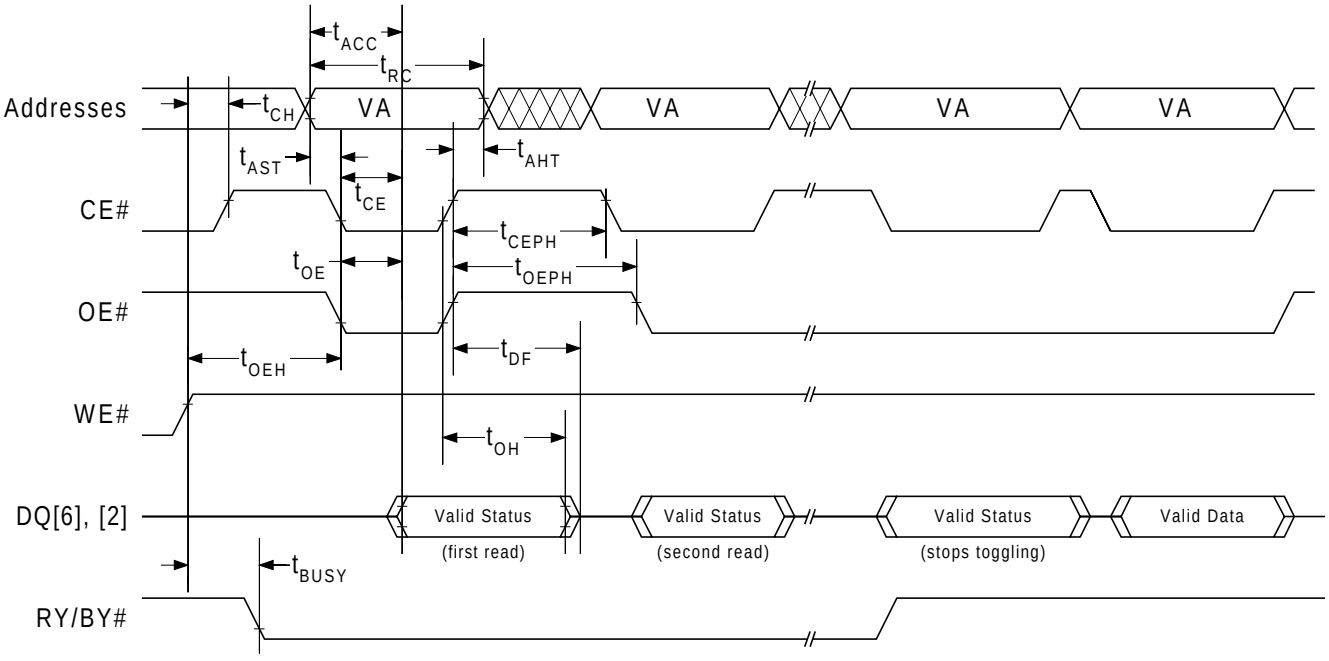
Figure 21. Sector/Chip Erase Operation Timings

AC CHARACTERISTICS



Notes:
1. VA = Valid Address for reading Data# Polling status data (see Write Operation Status section).
2. Illustration shows first status cycle after command sequence, last status read cycle and array data read cycle.

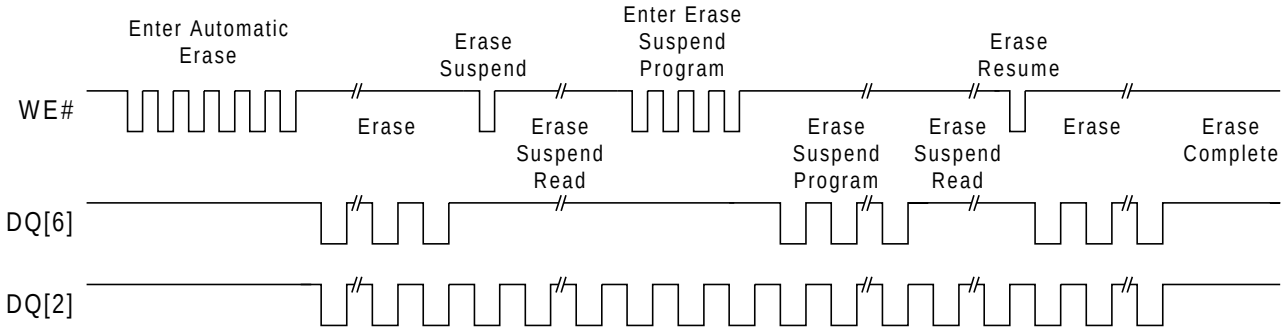
Figure 22. Data# Polling Timings (During Automatic Algorithms)



Notes:
1. VA = Valid Address for reading Toggle Bits (DQ[2], DQ[6]) status data (see Write Operation Status section).
2. Illustration shows first two status read cycles after command sequence, last status read cycle and array data read cycle.

Figure 23. Toggle Bit Timings (During Automatic Algorithms)

AC CHARACTERISTICS



Notes:
1. The system may use CE# or OE# to toggle DQ[2] and DQ[6]. DQ[2] toggles only when read at an address within an erase-suspended sector.

Figure 24. DQ[2] and DQ[6] Operation

Sector Protect and Unprotect, Temporary Sector Unprotect

Parameter		Description		Speed Option				Unit
JEDEC	Std			- 70	- 80	- 90	- 12	
	t_{VIDR}	V_{ID} Transition Time for Temporary Sector Unprotect [1]	Min	500				ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4				µs
	t_{VRST}	RESET# Setup Time for Sector Group Protect and Sector Unprotect	Min	1				µs
	t_{PROT}	Sector Group Protect Time	Max	150				µs
	t_{UNPR}	Sector Unprotect Time	Max	15				ms

Notes:
1. Not 100% tested.

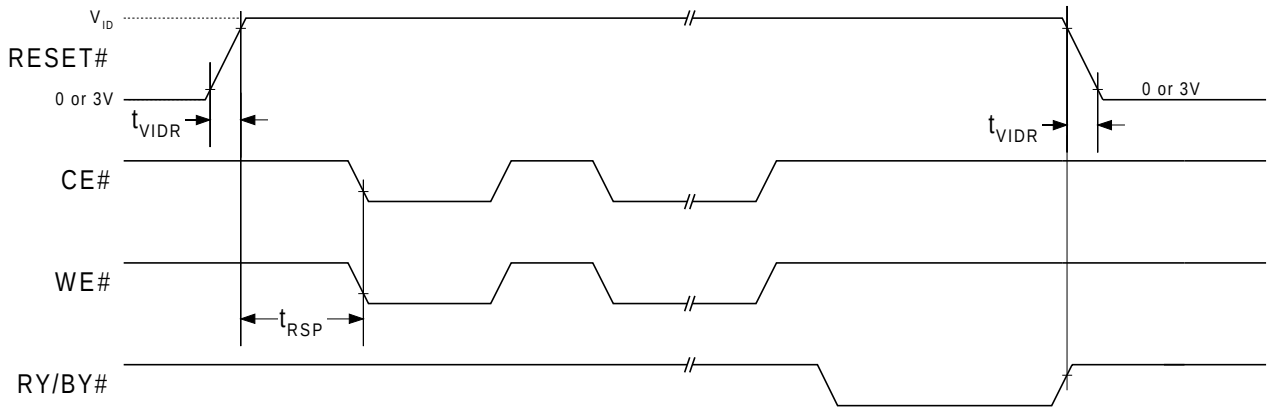
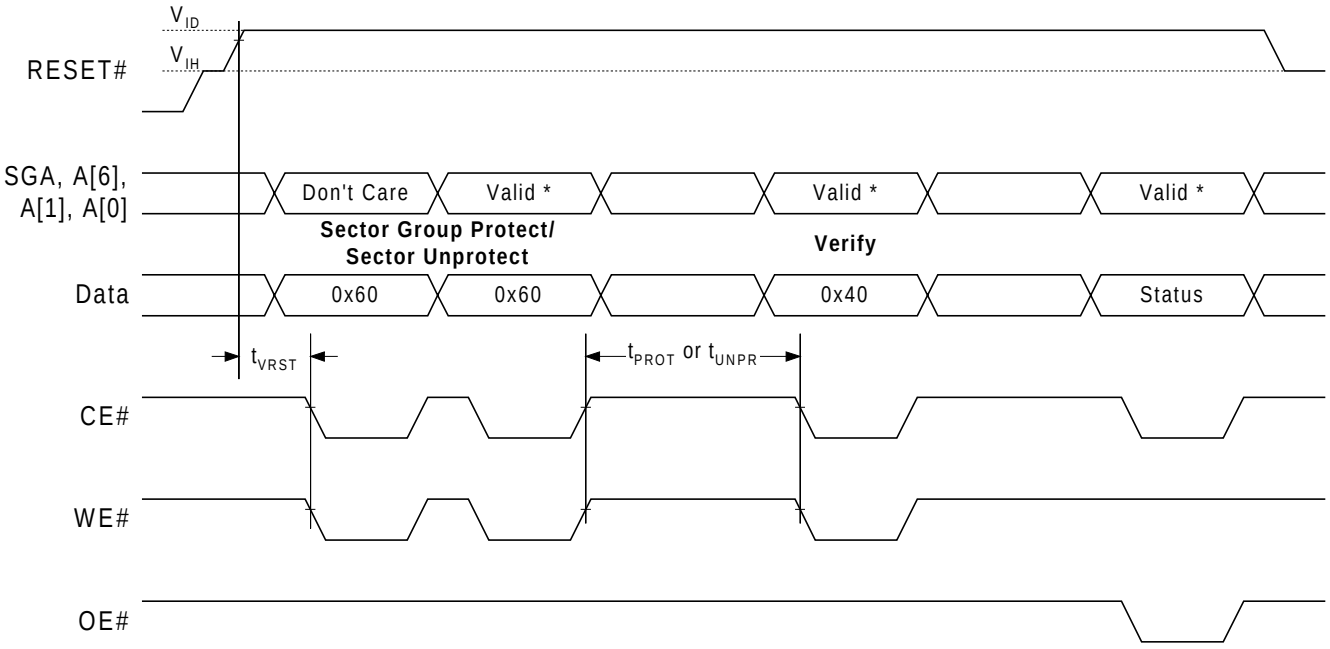


Figure 25. Temporary Sector Unprotect Timings

AC CHARACTERISTICS



Note: For Sector Group Protect, A[6] = 0, A[1] = 1, A[0] = 0. For Sector Unprotect, A[6] = 1, A[1] = 1, A[0] = 0.

Figure 26. Sector Group Protect and Sector Unprotect Timings

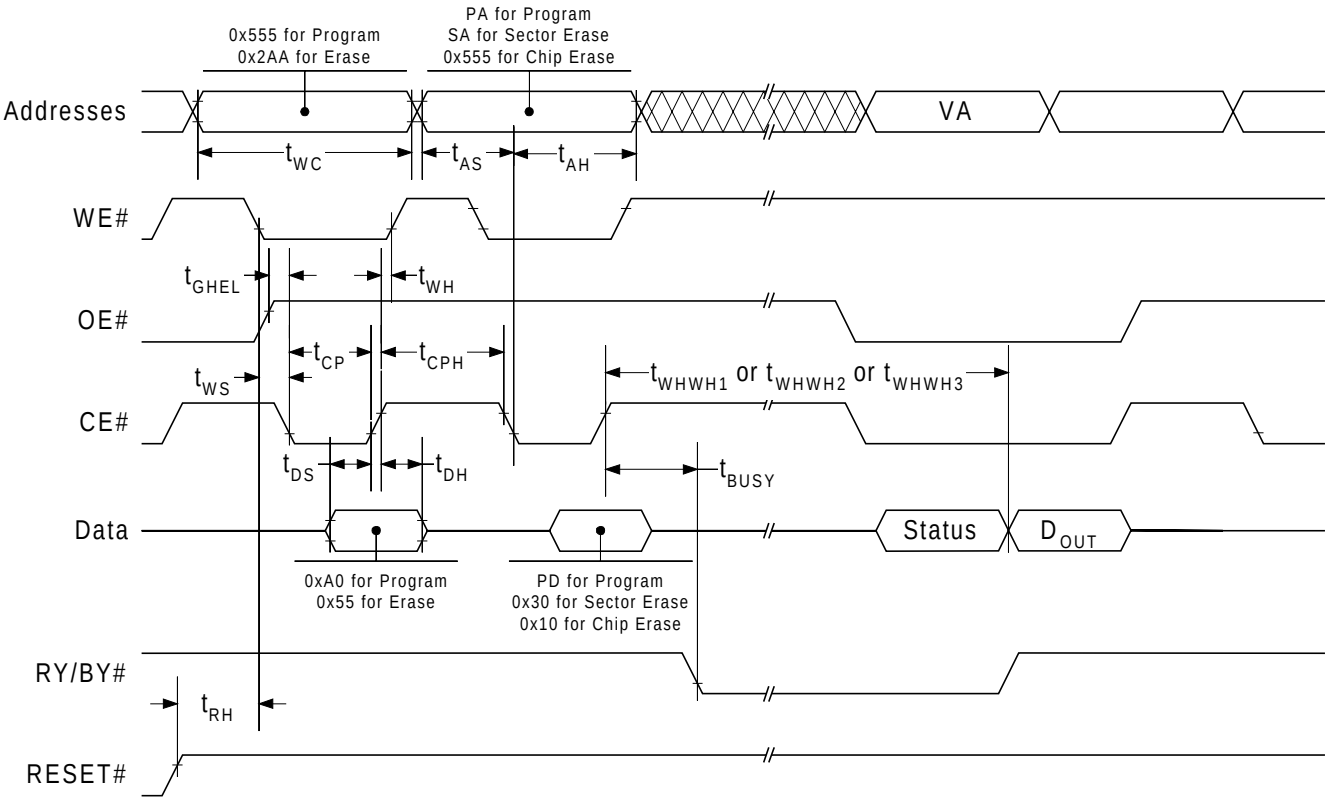
AC CHARACTERISTICS

Alternate CE# Controlled Erase/Program Operations

Parameter		Description		Speed Option				Unit
JEDEC	Std			- 70	- 80	- 90	- 12	
t_{AVAV}	t_{WC}	Write Cycle Time [1]	Min	70	80	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	45	45	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to CE# Low)	Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	35	35	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30				ns
	t_{BUSY}	CE# High to RY/BY# Delay	Min	90				ns

Notes:
1. Not 100% tested.
2. See Programming and Erase Operations table for Erase, Program and Endurance characterisitics.

AC CHARACTERISTICS



Notes:

1. PA = program address, PD = program data, VA = Valid Address for reading program or erase status (see Write Operation Status section), D_{OUT} = array data read at VA.
2. Illustration shows the last two cycles of the program or erase command sequence and the last status read cycle.
3. RESET# shown only to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

Figure 27. Alternate CE# Controlled Write Operation Timings

Latchup Characteristics

Description	Minimum	Maximum	Unit
Input voltage with respect to V_{SS} on all pins except I/O pins (including WP#/ACC, A[9], OE# and RESET#)	- 1.0	12.5	V
Input voltage with respect to V_{SS} on all I/O pins	- 1.0	V_{CC} + 1.0	V
V_{CC} Current	- 100	100	mA

Notes:
1. Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0V, one pin at a time.

TSOP Pin Capacitance

Symbol	Parameter	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions: T_A = 25 ºC, f = 1.0 MHz.

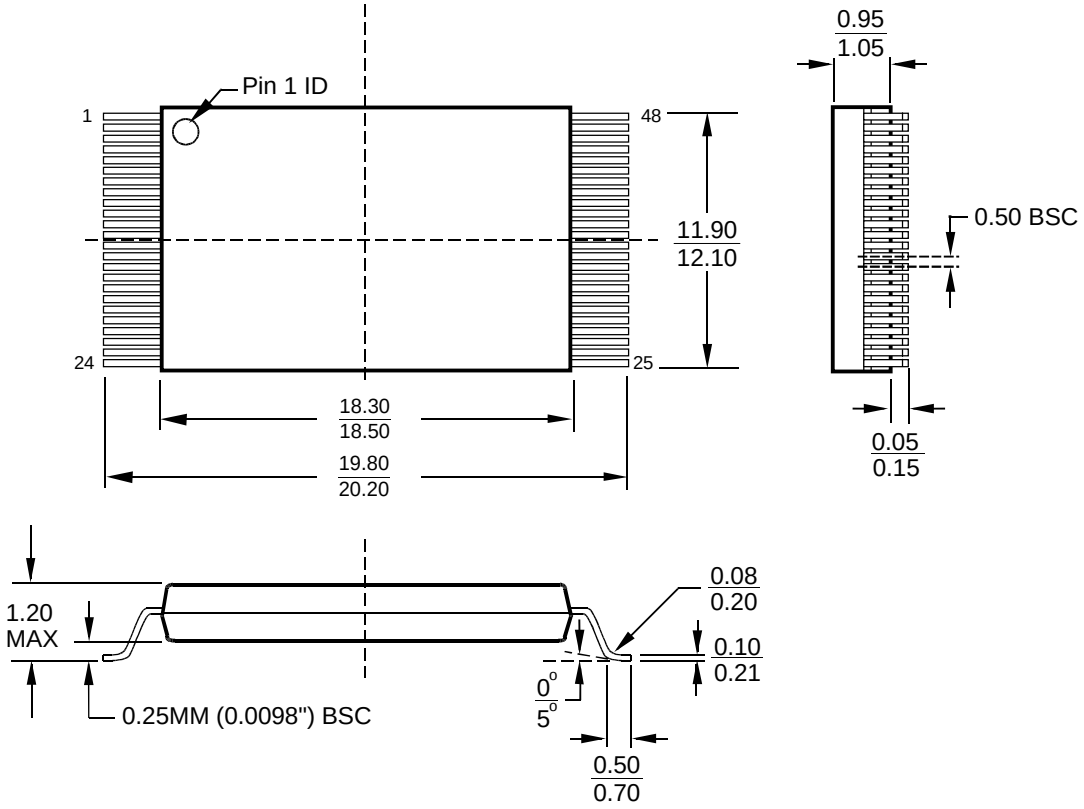
Data Retention

Parameter	Test Conditions	Minimum	Unit
Minimum Pattern Data Retention Time	150 ºC	10	Years
	125 ºC	20	Years

PACKAGE DRAWINGS

Physical Dimensions

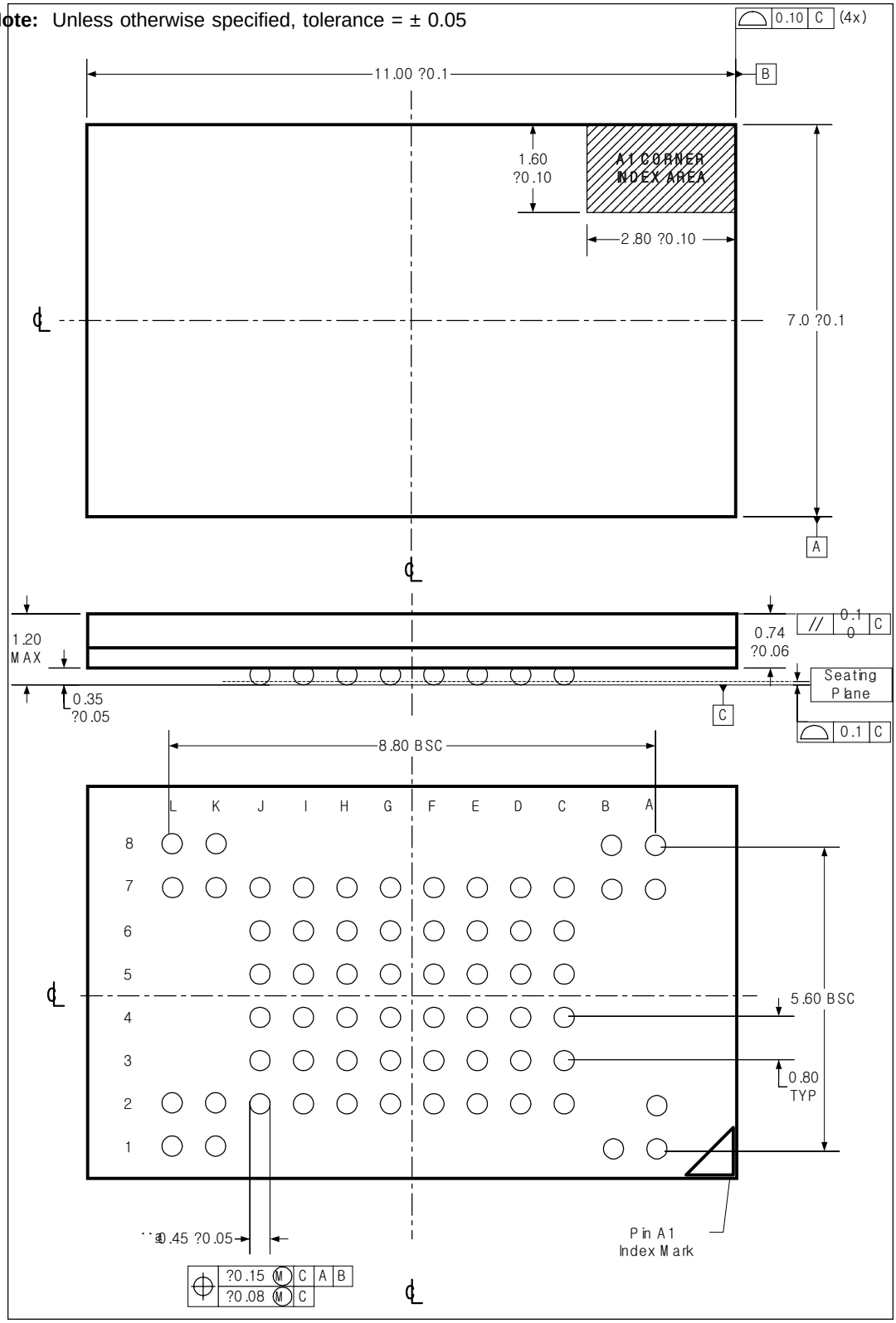
TSOP48 - 48-pin Thin Small Outline Package (measurements in millimeters)



PACKAGE DRAWINGS

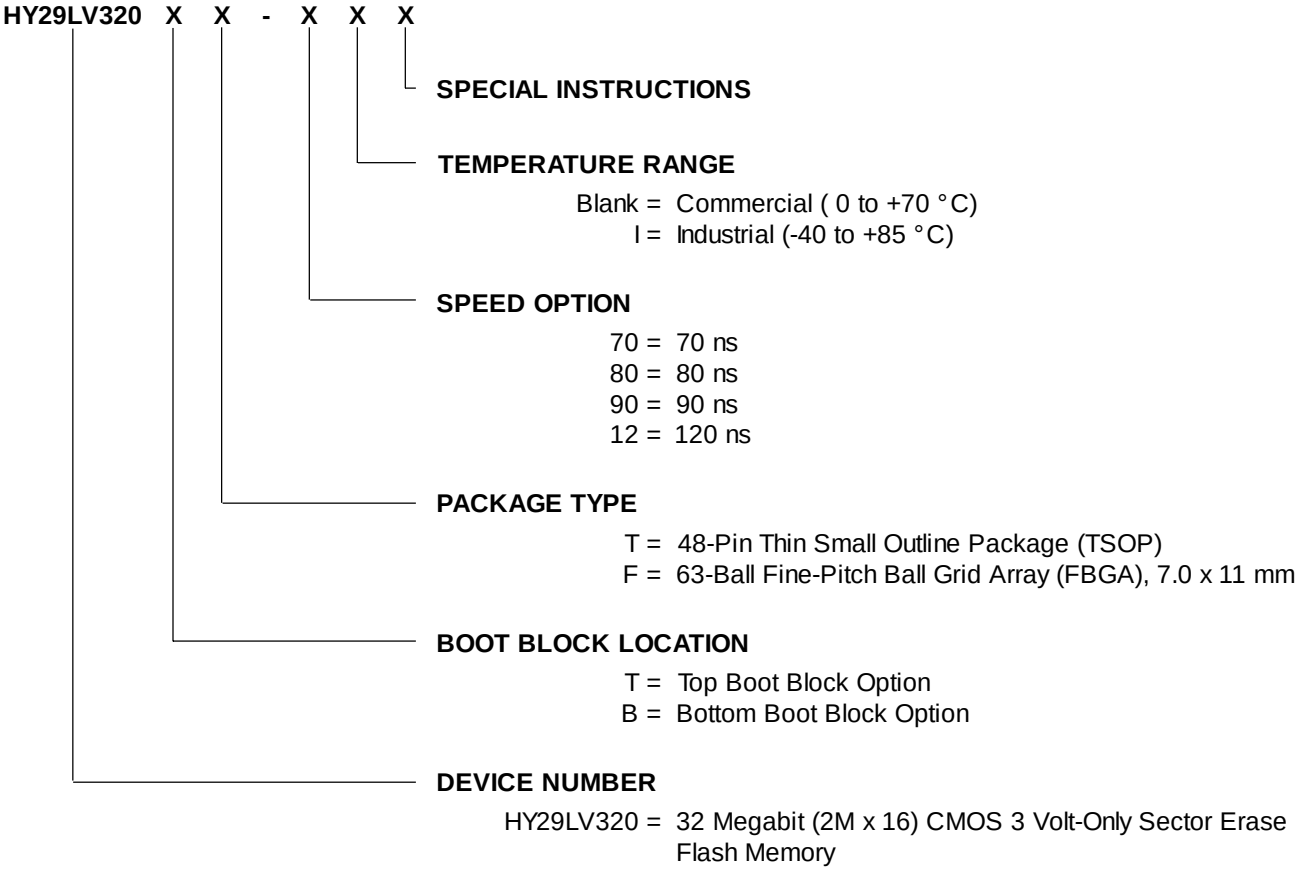
Physical Dimensions

FBGA63 - 63-Ball Fine-Pitch Ball Grid Array, 7.0 x 11 mm (measurements in millimeters)



ORDERING INFORMATION

Hynix products are available in several speeds, packages and operating temperature ranges. The ordering part number is formed by combining a number of fields, as indicated below. Refer to the 'Valid Combinations' table, which lists the configurations that are planned to be supported in volume. Please contact your local Hynix representative or distributor to confirm current availability of specific configurations and to determine if additional configurations have been released.



VALID COMBINATIONS

	Package and Speed							
	FBGA				TSOP			
Temperature	70 ns	80 ns	90 ns	120 ns	70 ns	80 ns	90 ns	120 ns
	Operating Voltage: 2.7 - 3.6 Volts							
Commercial	--	F-80	F-90	F-12	--	T-80	T-90	T-12
Industrial	F-70I	F-80I	F-90I	F-12I	T-70I	T-80I	T-90I	T-12I
	Operating Voltage: 3.0 - 3.6 Volts							
Commercial	F-70	--	--	--	T-70	--	--	--

Note:

1. The complete part number is formed by appending the suffix shown in the table to the Device Number. For example, the part number for a 90 ns, Industrial temperature range device in the TSOP package with the top boot block option is *HY29LV320TT-90I*.

Important Notice

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Revision Record

Rev.	Date	Details
1.0	4/01	Original issue.
1.1	7/01	-70 operating voltage specification changed to 2.7 - 3.6V for Industrial temperature grade. Changed WP#/ACC input rquirement to V_{IH} during sector group protect/unprotect operations. Changed sector and chip erase parameters and corresponding CFI data. Corrected Figure 22 and error in Table 9.
1.3	5/02	I_{LIT} (Input Load Current) spec for WP#/ACC pin eliminated. FBGA package spec changed from 48ball(12x7.25mm) with 0.3ball diameter to 63ball(11x7mm2) with 0.45 ball diameter for better reliability.

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