Direct Rambus™ RIMM™ Module

128 MBytes (64M x 16/18) based on 8Mx16/18

Overview

The Direct Rambus™ RIMM™ module is a general purpose high-performance memory subsystem suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

The 128MB Direct Rambus RIMM module consists of eight 128M Direct Rambus DRAM (Direct RDRAM™) devices. These are extremely high-speed CMOS DRAMs organized as 8M words by 16 or 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600MHz or 800MHz transfer rates while using conventional system and board design technologies. Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10ns per sixteen bytes).

The architecture of the Direct RDRAM allows the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAM's thirty-two banks support up to four simultaneous transactions.

Features

184-pin 1mm pin spacing
Card Size: 133.35mm x 31.75mm x 1.27mm
(5.25” x 1.25” x 0.050”)
128MB Direct RDRAM storage
Each RDRAM has 32banks, for 256banks total on module
Gold plated contacts
RDRAMs use Chip Scale Package (CSP)
Serial Presence Detect support
Operates from a 2.5 volt supply (±5%)
Low power and powerdown self refresh modes
Separate Row and Column buses for higher efficiency

Key Timing Parameters/Part Numbers

The following table lists the frequency and latency bins available from RIMM modules. An optional -LP designator is used to indicate low power modules.

Organization	I/O Freq. MHz	t_{rac} (Row Access Time) ns	Part Number
64M x 16	600	53	HYMR11664-653
64M x 16	800	45	HYMR11664-845
64M x 16	800	40	HYMR11664-840
64M x 18	600	53	HYMR11864-653
64M x 18	800	45	HYMR11864-845
64M x 18	800	40	HYMR11864-840

Form Factor

The Direct Rambus RIMM modules are offered in a 184-pin 1mm pin pitch form factor suitable for desktop and other system applications.

Pinouts and Pin Names

Pin	Pin Name	Pin	Pin Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTMN	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTM	B14	NC
A15	Gnd	B15	Gnd
A16	NC	B16	LROW2
A17	Gnd	B17	Gnd
A18	LROW1	B18	LROW0
A19	Gnd	B19	Gnd
A20	LCOL4	B20	LCOL3
A21	Gnd	B21	Gnd
A22	LCOL2	B22	LCOL1
A23	Gnd	B23	Gnd
A24	LCOL0	B24	LDQB0
A25	Gnd	B25	Gnd
A26	LDQB1	B26	LDQB2
A27	Gnd	B27	Gnd
A28	LDQB3	B28	LDQB4
A29	Gnd	B29	Gnd
A30	LDQB5	B30	LDQB6
A31	Gnd	B31	Gnd
A32	LDQB7	B32	LDQB8
A33	Gnd	B33	Gnd
A34	LSCK	B34	LCMD
A35	Vcmos	B35	Vcmos
A36	SOUT	B36	SIN
A37	Vcmos	B37	Vcmos
A38	NC	B38	NC
A39	Gnd	B39	Gnd
A40	NC	B40	NC
A41	Vdd	B41	Vdd
A42	Vdd	B42	Vdd
A43	NC	B43	NC
A44	NC	B44	NC
A45	NC	B45	NC
A46	NC	B46	NC

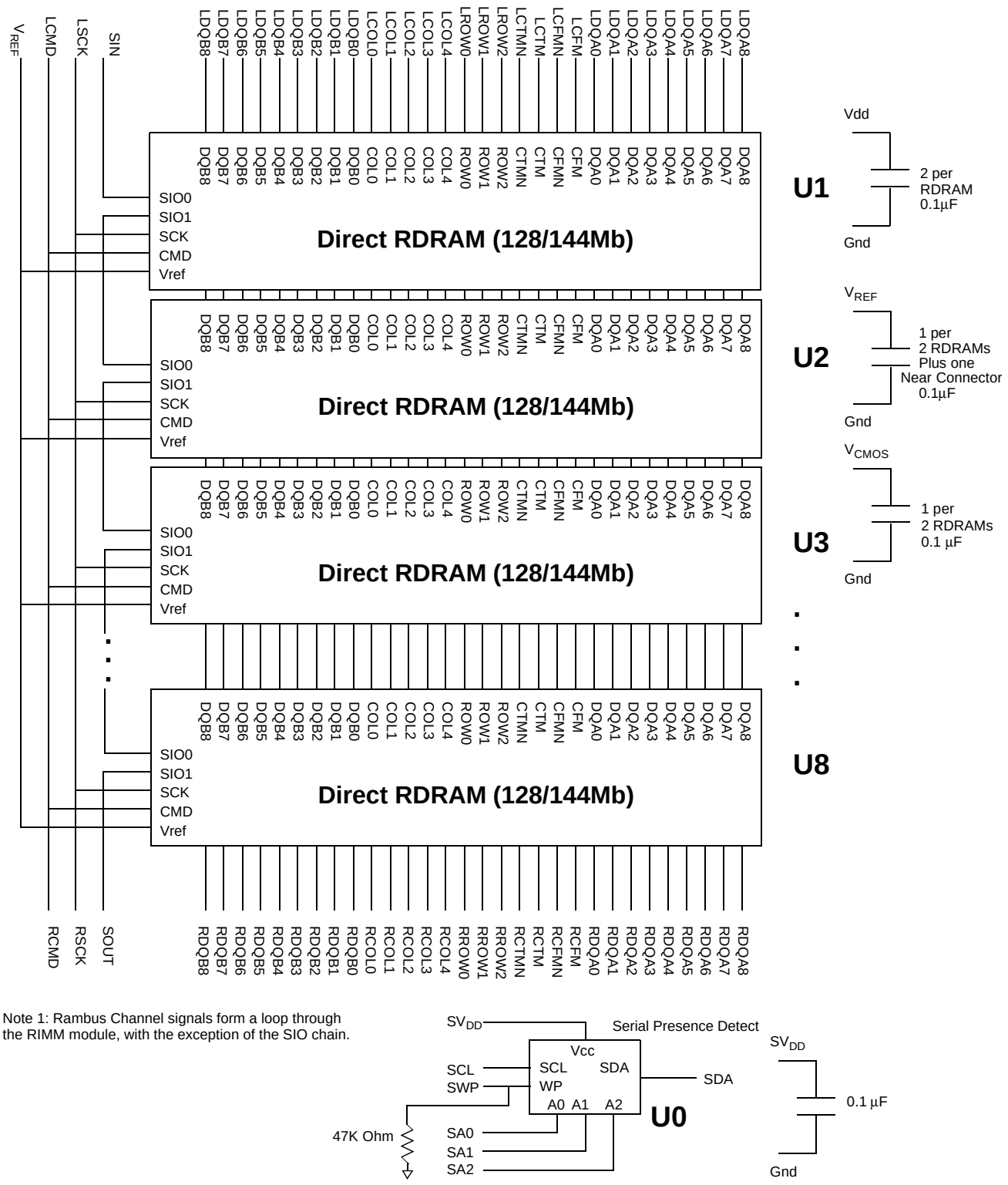
Pin	Pin Name	Pin	Pin Name
A47	NC	B47	NC
A48	NC	B48	NC
A49	NC	B49	NC
A50	NC	B50	NC
A51	Vref	B51	Vref
A52	Gnd	B52	Gnd
A53	SCL	B53	SA0
A54	Vdd	B54	Vdd
A55	SDA	B55	SA1
A56	SVdd	B56	SVdd
A57	SWP	B57	SA2
A58	Vdd	B58	Vdd
A59	RSCK	B59	RCMD
A60	Gnd	B60	Gnd
A61	RDQB7	B61	RDQB8
A62	Gnd	B62	Gnd
A63	RDQB5	B63	RDQB6
A64	Gnd	B64	Gnd
A65	RDQB3	B65	RDQB4
A66	Gnd	B66	Gnd
A67	RDQB1	B67	RDQB2
A68	Gnd	B68	Gnd
A69	RCOL0	B69	RDQB0
A70	Gnd	B70	Gnd
A71	RCOL2	B71	RCOL1
A72	Gnd	B72	Gnd
A73	RCOL4	B73	RCOL3
A74	Gnd	B74	Gnd
A75	RROW1	B75	RROW0
A76	Gnd	B76	Gnd
A77	NC	B77	RROW2
A78	Gnd	B78	Gnd
A79	RCTM	B79	NC
A80	Gnd	B80	Gnd
A81	RCTMN	B81	RCFMN
A82	Gnd	B82	Gnd
A83	RDQA0	B83	RCFM
A84	Gnd	B84	Gnd
A85	RDQA2	B85	RDQA1
A86	Gnd	B86	Gnd
A87	RDQA4	B87	RDQA3
A88	Gnd	B88	Gnd
A89	RDQA6	B89	RDQA5
A90	Gnd	B90	Gnd
A91	RDQA8	B91	RDQA7
A92	Gnd	B92	Gnd

Pin Definition

Signal	Pins	I/O	Type	Description
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, A82, A84, A86, A88, A90, A92, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B39, B52, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80, B82, B84, B86, B88, B90, B92			Ground reference for RDRAM core and interface. 72 pins.
LCFM	B10	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B34	**I**	**V_{CMOS}**	Serial Command Pin. Pin used to read from and write to the control registers. Also used for power management.
LCOL4.. LCOL0	A20, B20, A22, B22, A24	**I**	**RSL**	Column bus. 5-pin bus containing control and address information for column accesses.
LCTM	A14	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A12	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8.. LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	**I/O**	**RSL**	Data bus A. A 9-pin bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on x16 devices
LDQB8.. LDQB0	B32, A32, B30, A30, B28, A28, B26, A26, B24	**I/O**	**RSL**	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on x16 devices.
LROW2.. LROW0	B16, A18, B18	**I**	**RSL**	Row bus. 3-pin bus containing control and address information for row accesses.
LSCK	A34	**I**	**V_{CMOS}**	Clock input. Pin used to read from and write to the control registers.
NC	A16, B14, A38, B38, A40, B40, A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50, A77, B79			These pins are not connected. These 24 pins are all reserved for future use.
RCFM	B83	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	B81	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.

Signal	Pins	I/O	Type	Description
RCMD	B59	**I**	**V_{CMOS}**	Serial Command Input. Pin used to read from and write to the control registers. Also used for power management.
RCOL4.. RCOL0	A73, B73, A71, B71, A69	**I**	**RSL**	Column bus. 5-pin bus containing control and address information for column accesses.
RCTM	A79	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	A81	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8.. RDQA0	A91, B91, A89, B89, A87, B87, A85, B85, A83	**I/O**	**RSL**	Data bus A. A 9-pin bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on x16 devices.
RDQB8.. RDQB0	B61, A61, B63, A63, B65, A65, B67, A67, B69	**I/O**	**RSL**	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on x16 devices.
RROW2.. RROW0	B77, A75, B75	**I**	**RSL**	Row bus. 3-pin bus containing control and address information for row accesses.
RSCK	A59	**I**	**V_{CMOS}**	Clock input. Pin used to read from and write to the control registers.
SA0	B53	**I**	**SV_{DD}**	Serial Presence Detect Address 0.
SA1	B55	**I**	**SV_{DD}**	Serial Presence Detect Address 1.
SA2	B57	**I**	**SV_{DD}**	Serial Presence Detect Address 2.
SCL	A53	**I**	**SV_{DD}**	Serial Presence Detect Clock.
SDA	A55	**I/O**	**SV_{DD}**	Serial Presence Detect Data (Open Collector I/O).
SIN	B36	**I/O**	**V_{CMOS}**	Serial I/O. Pin for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	A36	**I/O**	**V_{CMOS}**	Serial I/O. Pin for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{DD}	A56, B56			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	A57	**I**	**SV_{DD}**	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A35, B35, A37, B37			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A41, A42, A54, A58, B41, B42, B54, B58			Supply voltage for the RDRAM core and interface logic.
Vref	A51, B51			Logic threshold reference voltage for RSL signals.

Functional Diagram



Note 1: Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to Gnd	- 0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	- 0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	- 50	100	°C

DC Recommended Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O pin power supply - 2.5V controllers: - for 1.8V controllers:	2.5 - 0.13 1.8 - 0.1	2.5 + 0.25 1.8 + 0.2	V V
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	V
V_{IL}	RSL input low voltage	V_{REF} - 0.5	V_{REF} - 0.2	V
V_{IH}	RSL input high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL,CMOS}$	CMOS input low voltage	- 0.3	$0.5V_{CMOS}$ - 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	$0.5V_{CMOS}$ + 0.25	V_{CMOS} + 0.3	V
$V_{OL,CMOS}$	CMOS output low voltage @ $I_{OL,CMOS}$ = 1mA		0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$ = -0.25mA	V_{CMOS} - 0.3		V
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-40	40	µA
$I_{SCK,CMD}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-40	40	µA
$I_{SIN,SOUT}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10.0	10.0	µA

AC Electrical Specifications

Symbol	Parameter and Conditions	Min	Max	Unit
Z	Module Impedance	25.2	30.8	Ohms
T_{PD}	Propagation Delay, all RSL signals	-	1.2	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to an average clock delay [a]	-0.01	0.01	ns
$\Delta T_{PD-CMOS}$	Propagation delay variation of SCK and CMD signals with respect to an average clock delay [a]	-0.1	0.1	ns
V_{α}/V_{IN}	Attenuation Limit		4.0	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input risetime 20%-80%)		0.8	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input risetime 20%-80%)		1	%

a. Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

I_{DD} - V_{DD} Supply Current Profile

I_{DD}	RIMM module power test conditions	-600 Max	-800 Max	Unit
I_{DD1}	All RDRAMs in powerdown, self-refresh mode	TBD/TBD[a]		mA
I_{DD2}	All RDRAMs in NAP mode	TBD		mA
I_{DD3}	All RDRAMs in Standby mode, no commands	TBD	TBD	mA
I_{DD4}	All RDRAMs in Active mode, no commands	TBD	TBD	mA
I_{DD5}	All RDRAMs running refresh cycles, with $t_{RC} = t_{RC,MIN}$	TBD	TBD	mA
I_{DD6}	All RDRAMs running refresh cycles, with $t_{RC} = t_{REF}$/# of rows	TBD	TBD	mA
I_{DD7}	One RDRAM cycling t_{RC} = min, 1 bank, no COL packets, remainder of RDRAMs in Standby	TBD	TBD	mA
I_{DD8}	One RDRAM cycling t_{RC} = min, 1 bank, two dualocts per activate (32-byte transfers), remainder of RDRAMs in Standby	TBD	TBD	mA
I_{DD9}	One RDRAM burst read/write, 1 bank open, full bandwidth, COL address changing every dualoct, remainder of RDRAMs in Standby	TBD	TBD	mA

a. For modules with a -LP designator.

I_{CMOS} - V_{CMOS} Supply Current Profile

I_{CMOS}	RIMM module power test conditions	Max	Unit
I_{CMOS1}	Current when RDRAMs are in powerdown, self-refresh state	TBD	mA
I_{CMOS2}	Current when CMOS pins are used for register read/write operations (f=1MHz)	TBD	mA
I_{CMOS3}	Current when CMOS pins are used for power management operations (f=100MHz)	TBD	mA

Timing Parameters

The following timing parameters are from the RDRAMs pins, not the RIMM. Please refer to the RDRAM datasheet for detailed timing diagrams.

Parameter	Description	Min -40 -800	Min -45 -800	Min -53 -600	Max	Units
t_{RC}	Row Cycle time of RDRAM banks -the interval between ROWA packets with ACT commands to the same bank.	28	28	28	-	t_{CYCLE}
t_{RAS}	RAS-asserted time of RDRAM bank - the interval between ROWA packet with ACT command and next ROWR packet with PRER[a] command to the same bank.	20	20	20	60µs[b]	t_{CYCLE}
t_{RP}	Row Precharge time of RDRAM banks - the interval between ROWR packet with PRER[a] command and next ROWA packet with ACT command to the same bank.	8	8	8	-	t_{CYCLE}
t_{PP}	Precharge-to-precharge time of RDRAM device - the interval between successive ROWR packets with PRER[a] commands to any banks of the same device.	8	8	8	-	t_{CYCLE}
t_{RR}	RAS-to-RAS time of RDRAM device - the interval between successive ROWA packets with ACT commands to any banks of the same device.	8	8	8	-	t_{CYCLE}
t_{RCD}	RAS-to-CAS Delay - the interval from ROWA packet with ACT command to COLC packet with RD or WR command). Note - the RAS-to-CAS delay seen by the RDRAM core ($t_{RCD,CORE}$) is equal to $t_{RCD,CORE} = 1 + t_{RCD}$ because of differences in the row and column paths through the RDRAM interface.	7	9	7	-	t_{CYCLE}
t_{CAC}	CAS Access delay - the minimum interval from RD command to Q read data.	8	8	8	12	t_{CYCLE}
t_{CWD}	CAS Write Delay (interval from WR command to D write data.	6	6	6	6	t_{CYCLE}
t_{CC}	CAS-to-CAS time of RDRAM bank - the interval between successive COLC commands).	4	4	4	-	t_{CYCLE}
t_{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet.	4	4	4	4	t_{CYCLE}
t_{RTR}	Interval from COLC packet with WR command to COLC packet which causes retire, and to COLM packet with bytemask.	8	8	8	-	t_{CYCLE}
t_{OFFP}	The interval (offset) from COLC packet with RDA command, or from COLC packet with retire command (after WRA automatic precharge), or from COLX packet with PREX command to the equivalent ROWR packet with PRER.	4	4	4	4	t_{CYCLE}
t_{RDP}	Interval from last COLC packet with RD command to ROWR packet with PRER.	4	4	4	-	t_{CYCLE}
t_{RTP}	Interval from last COLC packet with automatic retire command to ROWR packet with PRER.	4	4	4	-	t_{CYCLE}

a. Or equivalent PREC or PREX command.
b. This is a constraint imposed by the core, and is therefore in units of µs rather than t_{CYCLE}.

Serial Presence Detect Contents

To be determined

Layout Drawing

The following defines the RIMM module dimensions. All units are in millimeters with inches in brackets[ ], where appropriate.

The maximum height of the module is 31.75mm(1.25”).