Ordering number : ENN*5924B

CMOS IC

LC87F5164A

8-Bit Single Chip Microcontroller with 64K-Byte FEPROM and 1024-Byte RAM On Chip

Preliminary

Overview

The LC87F5164A microcontroller is 8-bit single chip microcontroller with the following on-chip functional blocks:

- CPU: Operable at a minimum bus cycle time of 100ns
- 64K bytes flash ROM (re-writeable on board)
- 1024 byte RAM
- two high performance 16 bit timer/counters (can be divided into 8 bit units)
- two 8 bit timers with prescalers
- timer for use as date/time clock
- two synchronous serial I/O ports (with automatic block transmit/receive function)
- one asynchronous/synchronous serial I/O port
- 12-bit PWM × 2
- 8-channel × 8-bit AD converter
- high speed 8-bit parallel interface
- 19-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read Only Memory (Flash ROM)
- single 5V power supply, writeable on-board.
- block erase in 128 byte units
- 65536 × 8 bits (LC87F5164A)

(2) Bus Cycle Time
- 100ns (10MHz)

Note: The bus cycle time indicates ROM read time.

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TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(3) Minimum Instruction Cycle Time : 300ns (10MHz)

(4) Ports

- Input/output ports		
Each bit data direction programmable	59	(P1n,P2n,P3n,P70 to P73,P8n,PAn,PBn,PCn,S2Pn)
Nibble data direction programmable	8	(P0n)
- Input ports	2	(XT1,XT2)
- PWM Output ports	2	(PWM0,PWM1)
- Oscillator pins	2	(CF1,CF2)
- Reset pin	1	($\overline{\text{RES}}$)
- Power supply	6	(VSS1 to 3,VDD1 to 3)

(5) Timers

- Timer0: 16 bit timer/counter with capture register
  - Mode 0: 2 channel 8 bit timer with programmable 8 bit prescaler and 8 bit capture register
  - Mode 1: 8 bit timer with 8 bit programmable prescaler and 8 bit capture register + 8 bit counter with 8 bit capture register
  - Mode 2: 16 bit timer with 8 bit programmable prescaler and 16 bit capture register
  - Mode 3: 16 bit counter with 16 bit capture register
- Timer1: PWM/16 bit timer/counter (with toggle output)
  - Mode 0: 8 bit timer (with toggle output) + 8 bit timer counter (with toggle output)
  - Mode 1: 2 channel 8 bit PWM
  - Mode 2: 16 bit timer/counter (with toggle output)
  - Mode 3: 16 bit timer (with toggle output) Lower order 8 bits can be used as PWM output.
- Timer4: 8-bit timer with 6-bit prescaler
- Timer5: 8-bit timer with 6-bit prescaler
- Base timer
  1. The clock signal can be selected from any of the following: sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output for timer 0.
  2. Interrupts can be selected to occur at one of five different times.

(6) SIO

- SIO0: 8 bit synchronous serial interface
  1. LSB first/MSB first function available
  2. Internal 8-bit baud-rate generator (maximum transmit clock period 4/3 T_{CYC})
  3. Continuous automatic data communications (1 - 256 bits)
- SIO1: 8 bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8 bit serial IO (2-wire or 3-wire, transmit clock 2 - 512 T_{CYC})
  - Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8 - 2048 T_{CYC})
  - Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 - 512 T_{CYC})
  - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)
- SIO2: 8 bit synchronous serial interface
  1. LSB-first
  2. Built in 8-bit baud-rate generator (Maximum clock period 4/3 T_{CYC})
  3. Continuous automatic data communication (1 - 32 bytes)

(7) AD converter

- 8-bits × 8-channels

(8) PWM

- 2 channel synchronous variable 12 bit PWM

(9) Parallel interface

- RS, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS0}}$ - $\overline{\text{CS2}}$ Outputs (reversible polarity)
- read/write possible in 1 T_{CYC}

(10) Remote control receiver circuit (connected to P73/INT3/T0IN terminal)

- Noise rejection function (noise rejection filter time constant can selected from 1/32/128 T_{CYC})

(11) Watchdog timer
- The watchdog timer period set by external RC.
- Watchdog timer can be set to produce interrupt, system reset

(12) Interrupts
- 19-source, 10-vectored interrupts:
  1. Three level (low, high and highest) multiple interrupts are supported. During interrupt handling, an equal or lower level interrupt request is refused.
  2. If interrupt requests to two or more vector addresses occur at once, the higher level interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/Base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1/SIO2
9	00043H	H or L	ADC
10	0004BH	H or L	Port 0/T4/T5/PWM0, 1

• Priority Level: X>H>L
• For equal priority levels, vector with lowest address takes precedence.

(13) Subroutine stack levels
- 512 levels max. Stack is located in RAM

(14) Multiplication and divsion
- 16 bit × 8 bit (executed in 5 cycles)
- 24 bit × 16 bit (12 cycles)
- 16 bit ÷ 8 bit (8 cycles)
- 24 bit ÷16 bit (12 cycles)

(15) Oscillation circuits
- On-chip RC oscillation circuit used for system clock
- On-chip CF oscillation circuit used for system clock
- On-chip Crystal oscillation circuit used for system clock and time-base clock

(16) Standby function
- HALT mode

  HALT mode is used to reduce power consumption. Program execution is stopped. Peripheral circuits still operate.
  1. Oscillation circuits are not stopped automatically
  2. Release on system reset
- HOLD mode

  HOLD mode is used to reduce the power dissipation. Both program execution and peripheral circuits are stopped.
  1. CF, RC and crystal oscillation circuits stop automatically
  2. Release occurs on any of the following conditions
     • input to the reset pin goes low
     • a specified level is input to at least one of INT0, INT1, INT2, INT4, INT5
     • an interrupt condition arises at port 0

- X’tal HOLD mode

  X’tal HOLD mode is used to reduce power consumption. Program execution is stopped. All peripheral circuits except the base timer are stopped.

  1. CF and RC oscillation circuits stop automatically
  2. Crystal oscillator is maintained in its state at HOLD mode inception.
  3. Release occurs on any of the following conditions
     - input to the reset pin goes low
     - a specified level is input to at least one of INT0, INT1, INT2, INT4, INT5
     - an interrupt condition arises at port 0
     - an interrupt condition arises at the base-timer

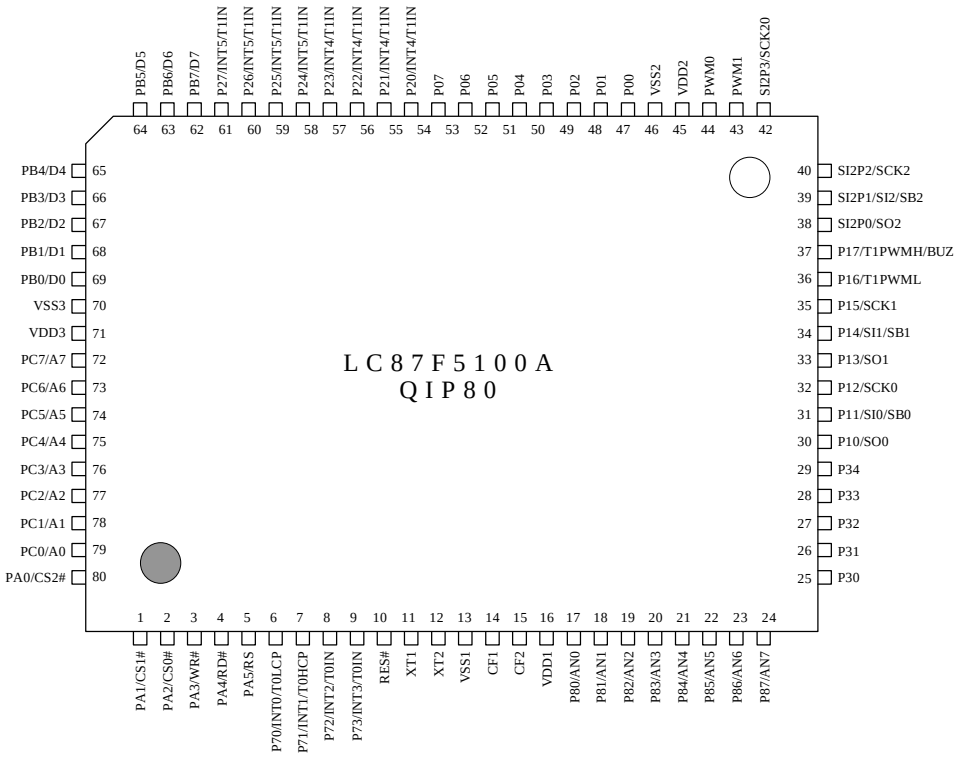
(17) Factory shipment

- delivery form QFP80E
- delivery form SQFP80

(18) Development Tools

- Evaluation chip : LC876099
- Emulator : EVA87000 + ECB875100 (Evaluation chip board) + POD875100 (POD)

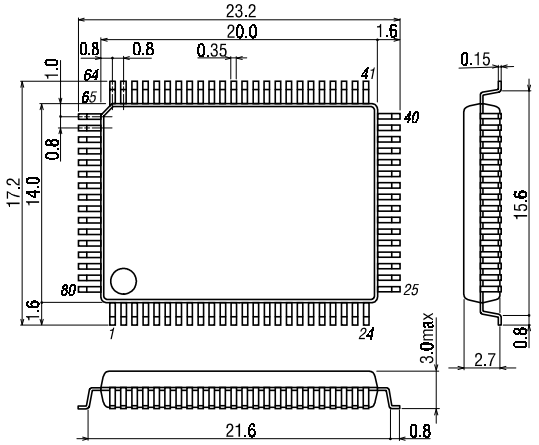
Pin Assignment



Package Dimension

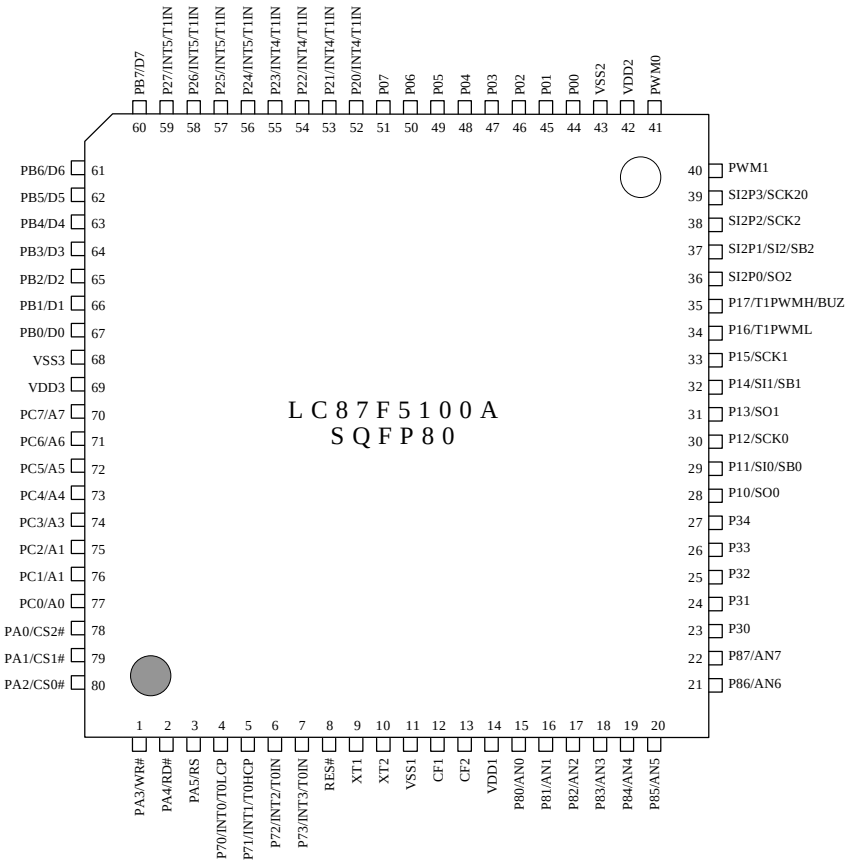
(unit : mm)

3174



SANYO : QIP-80E

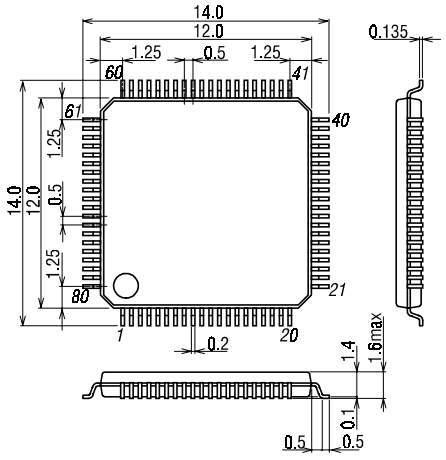
Pin Assignment



Package Dimension

(unit : mm)

3220

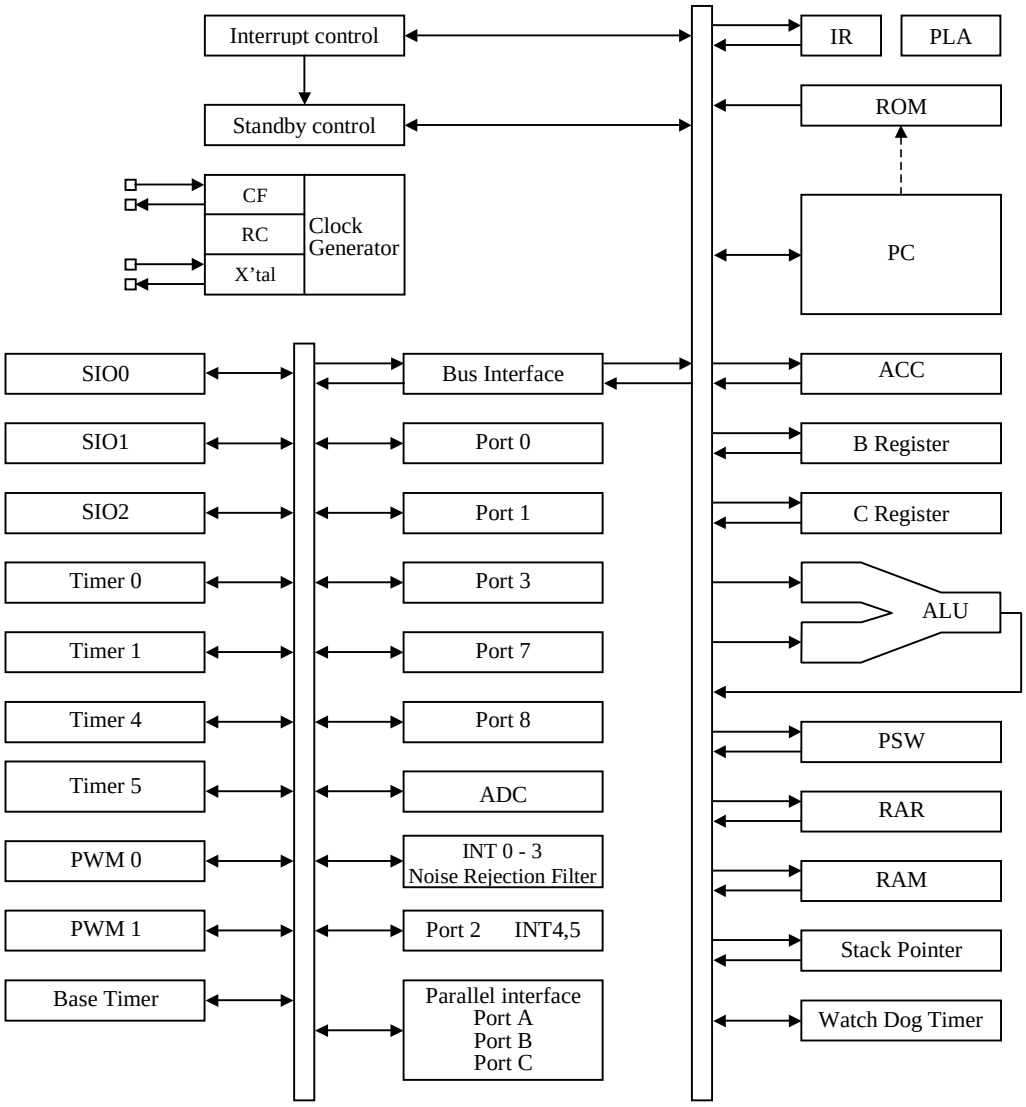


SANYO : SQFP-80

QIP	NAME	SQFP
1	PA1/ $\overline{CS1}$	79
2	PA2/ $\overline{CS0}$	80
3	PA3/ $\overline{WR}$	1
4	PA4/ $\overline{RD}$	2
5	PA5/RS	3
6	P70/INT0/T0LCP	4
7	P71/INT1/T0HCP	5
8	P72/INT2/T0IN	6
9	P73/INT3/T0IN	7
10	$\overline{RES}$	8
11	XT1	9
12	XT2	10
13	VSS1	11
14	CF1	12
15	CF2	13
16	VDD1	14
17	P80/AN0	15
18	P81/AN1	16
19	P82/AN2	17
20	P83/AN3	18
21	P84/AN4	19
22	P85/AN5	20
23	P86/AN6	21
24	P87/AN7	22
25	P30	23
26	P31	24
27	P32	25
28	P33	26
29	P34	27
30	P10/SO0	28
31	P11/SI0/SB0	29
32	P12/SCK0	30
33	P13/SO1	31
34	P14/SI1/SB1	32
35	P15/SCK1	33
36	P16/T1PWML	34
37	P17/T1PWMH/BUZ	35
38	SI2P0/SO2	36
39	SI2P1/SI2/SB2	37
40	SI2P2/SCK2	38

QIP	NAME	SQFP
41	SI2P3/SCK20	39
42	PWM1	40
43	PWM0	41
44	VDD2	42
45	VSS2	43
46	P00	44
47	P01	45
48	P02	46
49	P03	47
50	P04	48
51	P05	49
52	P06	50
53	P07	51
54	P20/INT4/T1IN	52
55	P21/INT4/T1IN	53
56	P22/INT4/T1IN	54
57	P23/INT4/T1IN	55
58	P24/INT5/T1IN	56
59	P25/INT5/T1IN	57
60	P26/INT5/T1IN	58
61	P27/INT5/T1IN	59
62	PB7/D7	60
63	PB6/D6	61
64	PB5/D5	62
65	PB4/D4	63
66	PB3/D3	64
67	PB2/D2	65
68	PB1/D1	66
69	PB0/D0	67
70	VSS3	68
71	VDD3	69
72	PC7/A7	70
73	PC6/A6	71
74	PC5/A5	72
75	PC4/A4	73
76	PC3/A3	74
77	PC2/A2	75
78	PC1/A1	76
79	PC0/A0	77
80	PA0/ $\overline{CS2}$	78

System Block Diagram



Pin Assignment

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Pin Function</th><th>Option</th></tr>
<tr><td>VSS1
VSS2
VSS3</td><td>-</td><td>Negative power supply</td><td>No</td></tr>
<tr><td>VDD1
VDD2
VDD3</td><td>-</td><td>Positive power supply</td><td>No</td></tr>
<tr><td>Port 0
P00 - P07</td><td>I/O</td><td>• 8-bit Input/output port
• Data direction can be specified in nibble units
• Use of pull-up resistor can be specified in nibble units
• HOLD-release input
• Input for port 0 interrupt</td><td>Yes</td></tr>
<tr><td>Port 1
P10 - P17</td><td>I/O</td><td>• 8-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• Other functions
P10: SIO0 data output
P11: SIO0 data input/bus input/output
P12: SIO0 clock input/output
P13: SIO1 data output
P14: SIO1 data input/bus input/output
P15: SIO1 clock input/output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/Buzzer output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 - P27</td><td>I/O</td><td>• 8-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• Other functions
P20-P23: INT4 input/HOLD release input/timer 1 event input /Timer 0L capture input/Timer 0H capture input
P24-P27: INT5 input/HOLD release input/timer 1 event input /Timer 0L capture input /Timer 0H capture input
Interrupt receiver format
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT5</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 - P34</td><td>I/O</td><td>• 5-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit</td><td>Yes</td></tr>
</table>

(Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>Port 7
P70 - P73</td><td>I/O</td><td>• 4-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• Other functions
P70: INT0 input/HOLD release input/Timer0L capture input
/Output for watchdog timer
P71: INT1 input/HOLD release input/Timer0H capture input
P72: INT2 input/HOLD release input/timer 0 event input
/Timer0L capture input
P73: INT3 input(noise rejection filter attached input)
/timer 0 event input/Timer0H capture input
Interrupt receiver format
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>No</td></tr>
<tr><td>Port 8
P80 - P87</td><td>I/O</td><td>• 8-bit Input/output port
• Data direction can be specified for each bit
• Other functions
P80-P87: AD input port</td><td>No</td></tr>
<tr><td>Port A
PA0 - PA5</td><td>I/O</td><td>• 6-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• Other functions
PA0: Parallel interface output $\overline{CS2}$
PA1: Parallel interface output $\overline{CS1}$
PA2: Parallel interface output $\overline{CS0}$
PA3: Parallel interface output $\overline{WR}$
PA4: Parallel interface output $\overline{RD}$
PA5: Parallel interface output RS</td><td>Yes</td></tr>
<tr><td>Port B
PB0 - PB7</td><td>I/O</td><td>• 8-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• Other functions
PB0-PB7: Parallel interface data input/output; address output</td><td>Yes</td></tr>
<tr><td>Port C
PC0 - PC7</td><td>I/O</td><td>• 8-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• Other functions
PC0-PC7: Parallel interface address output</td><td>Yes</td></tr>
<tr><td>SIO2 Port
SI2P0
- SI2P3</td><td>I/O</td><td>• 4-bit Input/output port
• Data direction can be specified for each bit
• Other functions
SI2P0: SIO2 data output
SI2P1: SIO2 data output/bus input/output
SI2P2: SIO2 clock input/output
SI2P3: SIO2 clock output</td><td>Yes</td></tr>
<tr><td>PWM0</td><td>O</td><td>PWM0 output port</td><td>No</td></tr>
<tr><td>PWM1</td><td>O</td><td>PWM1 output port</td><td>No</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset terminal</td><td>No</td></tr>
</table>

(Continued)

Name	I/O	Function description	Option
XT1	I	• Input for 32.768kHzcrystal oscillation • Other function Input port When not in use, connect to VDD1.	No
XT2	I/O	• Output for 32.768kHzcrystal oscillation • Other function General purpose input port When not in use, set to oscillation mode and leave open circuit	No
CF1	I	Input terminal for ceramic oscillator	No
CF2	O	Output terminal for ceramic oscillator	No

Port Output Configuration

Output configuration and pull-up resistor options are shown in the following table.
Input is possible even when port is set to output mode.

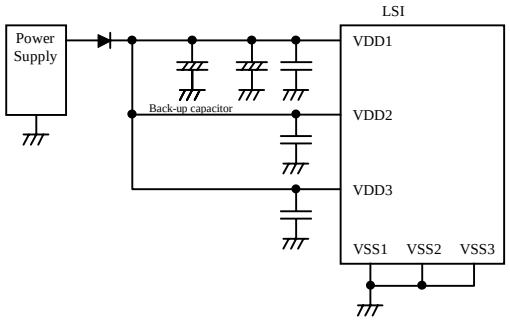
Terminal	Option applies to:	Option	Output Format	Pull-up resistor
P00-P07	1 bit units	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10-P17 P20-P27 P30-P34	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PA0-PA5 PB0-PB7(*) PC0-PC7	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	None	Nch-open drain	Programmable
P71-P73	-	None	CMOS	Programmable
P80-P87	-	None	Nch-open drain	None
SI2P0, SI2P2 SI2P3 PWM0, PWM1	-	None	CMOS	None
SI2P1	-	None	CMOS (When used as standard port) Nch-open drain (When used for SIO2 data)	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation	None

Note 1 Programmable pull-up resisters of Port 0 can be attatched in nibble units (P00-03, P04-07).

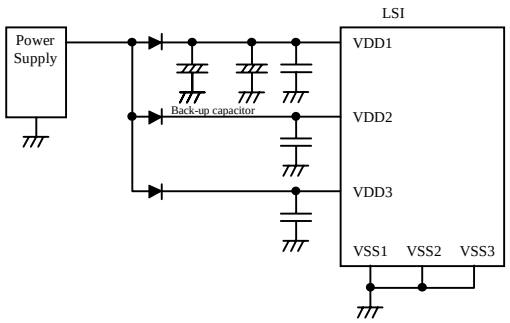
(*) When in parallel interface mode, PB0-PB7 output format is CMOS, regardless of any selected option.

Note: Connect as follows to reduce noise on VDD and increase the back-up time.
VSS1, VSS2 and VSS3 must be connected together and grounded.

Example 1 : In hold mode, during backup, port output ‘H’ level is supplied from the back-up capacitor.



Example 2 : During backup in hold mode output is not held high and its value in unsettled.



1. Absolute Maximum Ratings at Ta=25°C, VSS1=VSS2=VSS3=0V

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD1, VDD2, VDD3	VDD1=VDD2=VDD3		-0.3		+6.5	V
Input voltage		VI(1)	XT1, XT2, CF1			-0.3		VDD+0.3	
Output voltage		VO(1)	PWM0, PWM1			-0.3		VDD+0.3	
Input/output voltage		VIO(1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C SI2P00-SI2P03 PWM0, PWM1			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3 Ports A, B, C SI2P00-SI2P03 PWM0, PWM1	• CMOS output • For each pin.		-10			mA
		IOPH(2)	P71-P73	For each pin.		-5			
	Total output current	∑IOAH(1)	P71-P73	The total of all pins.		-5			
		∑IOAH(2)	Port 1 PWM0, PWM1 Port 3 SI2P00-SI2P03	The total of all pins.		-30			
		∑IOAH(3)	Ports 0, 2	The total of all pins.		-20			
		∑IOAH(4)	Port B	The total of all pins.		-20			
		∑IOAH(5)	Ports A, C	The total of all pins.		-20			
Low level output current	Peak output current	IOPL(1)	P02-P07 Ports 1, 2, 3 Ports A, B, C SI2P00-SI2P03 PWM0, PWM1	For each pin.				20	
		IOPL(2)	P00, P01	For each pin.				30	
		IOPL(3)	Ports 7, 8	For each pin.				15	
	Total output current	∑IOAL(1)	Port 7	The total of all pins.				5	
		∑IOAL(2)	Port 8	The total of all pins.				5	
		∑IOAL(3)	Port 1 PWM0, PWM1 Port 3 SI2P00-SI2P03	The total of all pins.				50	
		∑IOAL(4)	Ports 0, 2	The total of all pins.				70	
		∑IOAL(5)	Port B	The total of all pins.				40	
		∑IOAL(6)	Ports A, C	The total of all pins.				40	
Maximun power dissipation		Pdmax	QIP80E SQFP80	Ta=-20 to +70°C				350	mW
Operating temperature range		Topg				-20	to	70	°C
Storage temperature range		Tstg				-55	to	125	

2. Recommended Operating Range at Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating supply voltage range	VDD(1)	VDD1=VDD2 =VDD3	0.294μs≤ tCYC≤ 200μs		4.5		5.5	V
HOLD voltage	VHD	VDD1=VDD2 =VDD3	RAM and the register data are kept in HOLD mode.		2.0		5.5	
Input high voltage	VIH(1)	• Ports 1, 2 • SI2P00 - 03 • P71-P73 • P70 port input /interrupt		4.5 - 5.5	0.3VDD +0.7		VDD	
	VIH(2)	• Ports 0, 8 • Ports A, B, C		4.5 - 5.5	0.3VDD +0.7		VDD	
	VIH(3)	Port 70 Watchdog timer input		4.5 - 5.5	0.9VDD		VDD	
	VIH(4)	XT1, XT2, CF1, $\overline{RES}$		4.5 - 5.5	0.75VDD		VDD	
Input low voltage	VIL(1)	• Ports 1, 2 • SI2P00 - 03 • P71-P73 • P70 port input /interrupt		4.5 - 5.5	VSS		0.1VDD +0.4	
	VIL(2)	• Ports 0, 8 • Ports A, B, C		4.5 - 5.5	VSS		0.15VDD +0.4	
	VIL(5)	Port 70 Watchdog timer input		4.5 - 5.5	VSS		0.8VDD -1.0	
	VIL(6)	XT1, XT2, CF1, $\overline{RES}$		4.5 - 5.5	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 - 5.5	0.294		200	μs
External system clock frequency	FEXCF(1)	CF1	• CF2 open circuit • system clock divider set to 1/1 • external clock DUTY=50 ± 5%	4.5 - 5.5	0.1		10	MHz
			• CF2 open circuit • system clock divider set to 1/2	4.5 - 5.5	0.2		20.4	

(Note 1) The oscillation constant is shown in Tables 1 and 2.

3. Electrical Characteristics at Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Input high current	IIH(1)	• Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C • SI2P00-SI2P03 • $\overline{\text{RES}}$ • PWM0, PWM1	• Output disable • Pull-up resistor off • VIN=VDD (including off state leak current of output Tr.)	4.5 - 5.5			1	μA
	IIH(2)	XT1, XT2	When specified as an input port. VIN=VDD	4.5 - 5.5			1	
	IIH(3)	CF1	VIN=VDD	4.5 - 5.5			15	
Input low current	IIL(1)	• Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C • SI2P00-SI2P03 • $\overline{\text{RES}}$ • PWM0, PWM1	• Output disable • Pull-up resistor off • VIN=VSS (including off state leak current of output Tr.)	4.5 - 5.5	-1			
	IIL(2)	XT1, XT2	When specified as an input port VIN=VSS	4.5 - 5.5	-1			
	IIL(3)	CF1	VIN=VSS	4.5 - 5.5	-15			
Output high current	VOH(1)	• Ports 0, 1, 2, 3 • Ports B, C	IOH=-1.0mA	4.5 - 5.5	VDD-1			V
	VOH(2)	• SI2P00-SI2P03 • PWM0, PWM1	IOH=-0.1mA	4.5 - 5.5	VDD-0.5			
	VOH(3)	Port A	IOH=-5.0mA	4.5 - 5.5	VDD-1			
	VOH(4)		IOH=-0.4mA	4.5 - 5.5	VDD-0.5			
	VOH(5)	Port 7	IOH=-0.4mA	4.5 - 5.5	VDD-1			

(Continued)

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Output low current	VOL(1)	• Ports 0, 1, 2, 3 • Ports B, C	IOL=10mA	4.5 - 5.5			1.5	V
	VOL(2)	• SI2P00-SI2P03 • PWM0, PWM1	IOL=1.6mA	4.5 - 5.5			0.4	
	VOL(3)							
	VOL(4)	P00, P01	IOL=30mA	4.5 - 5.5			1.5	
	VOL(5)	Ports 7, 8	IOL=1mA	4.5 - 5.5			0.4	
	VOL(6)							
	VOL(7)	Port A	IOL=15mA	4.5 - 5.5			1.5	
	VOL(8)		IOL=2mA	4.5 - 5.5			0.4	
Pull-up resistor	Rpu	• Ports 0, 1, 2, 3 • Port 7 • Ports A, B, C	VOH=0.9VDD	4.5 - 5.5	15	40	70	kΩ
Hysteresis voltage	VHIS	• $\overline{\text{RES}}$		4.5 - 5.5		0.1VDD		V
Pin capacitance	CP	All pins	• Every other terminal connected to VSS. • f=1MHz • Ta=25°C	4.5 - 5.5		10		pF

4. Serial Input/Output Characteristics at Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter			Symbol	Pins	Conditions		VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tSCK(1)	SCK0(P12), SI2P2	Refer to figure 6		4.5 - 5.5	2			tCYC
		Low level pulse width	tSCKL(1)					1			
			tSCKLA(1)					1			
		High level pulse width	tSCKH(1)					1			
			tSCKHA(1)					3(SIO0) 5(SIO2)			
		Cycle	tSCK(2)	SCK1(P15)	Refer to figure 6		4.5 - 5.5	2			
		Low level pulse width	tSCKL(2)					1			
		High level pulse width	tSCKH(2)					1			
	Output clock	Cycle	tSCK(3)	SCK0(P12), SI2P2 SI2P3	• CMOS output option • Refer to figure 6		4.5 - 5.5	4/3			
		Low level pulse width	tSCKL(3)						1/2		tSCK
			tSCKLA(2)			SCK0(P12) SIO0			3/4		
						SI2P2, SI2P3 SIO2			1		
		High level pulse width	tSCKH(3)						1/2		
			tSCKHA(2)			SCK0(P12) SIO0			2		
						SI2P2, SI2P3 SIO2			7/4		
		Cycle	tSCK(4)	SCK1(P15)	• CMOS output option • Refer to figure 6		4.5 - 5.5	2			tCYC
		Low level pulse width	tSCKL(4)						1/2		tSCK
		High level pulse width	tSCKH(4)						1/2		
Serial input	Data set-up time		tsDI	SB0(P11), SB1(P14), SI2P1 SI0 SI1	• Data set-up to SI0CLK • Refer to figure 6		4.5 - 5.5	0.03			µs
	Data hold time		thDI					0.03			
Serial output	Output delay time		tdD0	SO0(P10), SO1(P13), SB0(O11), SB1(P14), SI2P0, SI2P1	• Data set-up to SI0CLK • When port is open drain: Time delay from SI0CLK trailing edge to the SO data change. • Refer to figure 6		4.5 - 5.5			1/3tCYC +0.05	

5. Parallel Input/ Output Characteristics at Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Note: Port A terminals used as RS, $\overline{WR}$, $\overline{RD}$ and $\overline{CS}$ should be set to CMOS format.
Please refer to figures 8 and 9 for parallel output timing waveforms.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Write cycle, Read cycle	tC(1)			4.5 - 5.5		1		tCYC
Address set-up time	tsA(1)	• $\overline{WR}$ (PA3), PB0-PB7 • $\overline{RD}$ (PA4), PC0-PC7	From address set-up until control signal changes	4.5 - 5.5	1/3tCYC -30ns			tCYC & ns
	tsA(2)	$\overline{RD}$ (PA4), PC0-PC7		4.5 - 5.5	2/3tCYC -30ns			
Address hold time	thA(1)	$\overline{RD}$ (PA4), PC0-PC7	From change of $\overline{RD}$ until address change	4.5 - 5.5	1/6tCYC			
	thA(2)	$\overline{WR}$ (PA3), PC0-PC7	From change of $\overline{WR}$ until address change	4.5 - 5.5	5			ns
RS set-up tie	tsRS(1)	$\overline{WR}$ (PA3), RS(PA5), $\overline{CS}$ (PAX)	From change of RS, $\overline{CS}$ until change in $\overline{WR}$	4.5 - 5.5	1/6tCYC -15ns			tCYC & ns
	tsRS(2)	$\overline{RD}$ (PA4), RS(PA5)	from change of RS until change in $\overline{RD}$	4.5 - 5.5	1/6tCYC -15ns			
	tsRS(3)	$\overline{RD}$ (PA4), RS(PA5)		4.5 - 5.5	1/3tCYC -15ns			
$\overline{CS}$ set-up time	tsCS(1)	$\overline{RD}$ (PA4), $\overline{CS}$ (PAX)	From change in $\overline{CS}$ until change in $\overline{RD}$	4.5 - 5.5	1/3tCYC -15ns			
	tsCS(2)	$\overline{WR}$ (PA3), $\overline{CS}$ (PAX)	From change in $\overline{CS}$ until change in $\overline{WR}$	4.5 - 5.5	2/3tCYC -15ns			
RS hold time	thRS(1)	$\overline{WR}$ (PA3), RS(PA5)	From change in $\overline{WR}$ until change in RS	4.5 - 5.5	0			ns
	thRS(2)	$\overline{RD}$ (PA4), RS(PA5), $\overline{CS}$ (PAX)	From change in $\overline{RD}$ until change in RS, $\overline{CS}$	4.5 - 5.5	1/6tCYC			tCYC & ns
	thRS(3)	$\overline{RD}$ (PA4), RS(PA5), $\overline{CS}$ (PAX)		4.5 - 5.5	0			ns
$\overline{CS}$ hold time	thCS(1)	$\overline{RD}$ (PA4), RS(PA5)	From change in $\overline{RD}$ until change in $\overline{CS}$	4.5 - 5.5	1/6tCYC			tCYC & ns
	thCS(2)	$\overline{WR}$ (PA3), RS(PA5)	From change in $\overline{WR}$ until change in $\overline{CS}$	4.5 - 5.5	0			ns
$\overline{WR}$ 'H' pulse width	tWRH(1)	$\overline{WR}$ (PA3)		4.5 - 5.5	1/6tCYC -5ns	1/6 tCYC		tCYC & ns
	tWRH(2)	$\overline{WR}$ (PA3)		4.5 - 5.5	2/3tCYC -5ns	2/3 tCYC		
$\overline{WR}$ 'L' pulse width	tWRL(1)	$\overline{WR}$ (PA3)		4.5 - 5.5	1/6tCYC -5ns	1/6 tCYC		
	tWRL(2)	$\overline{WR}$ (PA3)		4.5 - 5.5	1/3tCYC -5ns	1/3 tCYC		

(Continued)

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
$\overline{RD}$ 'H' pulse width	tRDH(1)	$\overline{RD}$ (PA4)		4.5 - 5.5	1/6tCYC -5ns	1/6 tCYC		tCYC & ns
	tRDH(2)	$\overline{RD}$ (PA4)		4.5 - 5.5	1/3tCYC -5ns	1/3 tCYC		
$\overline{RD}$ 'L' pulse width	tRDL(1)	$\overline{RD}$ (PA4)		4.5 - 5.5	1/3tCYC -5ns	1/3 tCYC		
	tRDL(2)	$\overline{RD}$ (PA4)		4.5 - 5.5	1/2tCYC -5ns	1/2 tCYC		
Data write permission delay	tdDT(1)	$\overline{RD}$ (PA4), PB0-PB7	Time for permission, from $\overline{RD}$ leading edge until input data set-up (Note 1)	4.5 - 5.5			1/6tCYC -15ns	
	tdDT(2)	$\overline{RD}$ (PA4), PB0-PB7		4.5 - 5.5			1/3tCYC -15ns	
Input data set-up time	tsDTR(1)	$\overline{RD}$ (PA4), PB0-PB7	From input data set-up to $\overline{RD}$ leading edge. (Note 2)	4.5 - 5.5	40			ns
Input data hold time	thDTR(1)	$\overline{RD}$ (PA4), PB0-PB7	From $\overline{RD}$ leading edge until input data hold	4.5 - 5.5	0			ns
Output data set-up time	tsDTW(1)	$\overline{RD}$ (PA4), PB0-PB7	From output data set-up until $\overline{WR}$ leading edge	4.5 - 5.5	1/3tCYC -30ns			tCYC & ns
Output data set-up time	tsDTW(2)	$\overline{RD}$ (PA4), PB0-PB7		4.5 - 5.5	1/3tCYC -30ns			
Output data hold time	thDTW(1)	$\overline{RD}$ (PA4), PB0-PB7	From $\overline{WR}$ leading edge until output data hold	4.5 - 5.5	0			ns
	thDTW(2)			4.5 - 5.5	0			

Note 1 : Time until incorrect data of Low is disappeared.
Note 2 : Incorrect data of Low is not output in the period between tRDL(1) - tdDT(1).

6. Pulse Input Conditions at Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72) INT4(P20-P23) INT5(P24-P27)	• Interrupt acceptable • Events to timer 0 and 1 can be input.	4.5 - 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (The noise rejection clock select to 1/1.)	• Interrupt acceptable • Events to timer 0 can be input.	4.5 - 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (The noise rejection clock select to 1/32.)	• Interrupt acceptable • Events to timer 0 can be input.	4.5 - 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (The noise rejection clock select to 1/128.)	• Interrupt acceptable • Events to timer 0 can be input.	4.5 - 5.5	256			
	tPIL(5)	$\overline{RES}$	Reset acceptable	4.5 - 5.5	200			µs

7. AD Converter Characteristics at Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Resolution	N	AN0(P80) - AN7(P87)		4.5 - 5.5		8		bit
Absolute precision	ET		(Note 2)	4.5 - 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time =32 × tCYC (ADCR2=0) (Note 3)	4.5 - 5.5	15.10 (tCYC= 0.588µs)		97.92 (tCYC= 3.06µs)	µs
			AD conversion time =64 × tCYC (ADCR2=1) (Note 3)	4.5 - 5.5	15.10 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			4.5 - 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 - 5.5			1	µA
	IAINL		VAIN=VSS	4.5 - 5.5	-1			

(Note 2) Absolute precision not including quantizing error (±1/2 LSB).

(Note 3) Conversion time means time from executing AD conversion instruction to loading complete digital value to register.

8. Current Dissipation Characteristics at Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current flow during basic operation (Note 4)	IDDOP(1)	VDD1 =VDD2 =VDD3	• FmCF=10MHz for Ceramic resonator oscillation • FmX'tal=32.768kHz for crystal oscillation • System clock: CF oscillation • Internal RC oscillation stopped. • Divider: 1/1	4.5 - 5.5		18	35	mA
	IDDOP(2)		• CF1=20MHz for external clock • FmX'tal=32.768kHz for crystal oscillation • System clock : CF1 • Internal RC oscillation stopped. • Divider 1/2	4.5 - 5.5		18	35	
Current flow: HALT mode (Note 4)	IDDHALT(1)	VDD1 =VDD2 =VDD3	HALT mode • FmCF=10MHz for ceramic resonator oscillation • FmX'tal=32.768kHz for crystal oscillation • System clock: CF oscillation • Internal RC oscillation stopped. • Divider 1/1	4.5 - 5.5		6	12	mA
	IDDHALT(2)		• CF1=20MHz external clock • FmX'tal=32.768kHz for crystal oscillation • System clock : CF1 • Internal RC oscillation stopped. • Divider 1/2	4.5 - 5.5		7	14	
Current flow: HOLD mode (Note 4)	IDDHOLD(1)	VDD1	HOLD mode • CF1=VDD or open circuit (when using external clock)	4.5 - 5.5		0.01	25	μA
Current flow: Date/time clock HOLD mode	IDDHOLD(2)	VDD1	Date/time clock HOLD mode • CF1=VDD or open circuit (when using external clock) • FmX'tal=32.768kHz for crystal oscillation	4.5 - 5.5		35	100	μA

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

9. F-ROM Write Characteristics at Ta=+10°C to +55°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
On-board write current	IDDFW(1)	VDD1	• 128-byte write • including erase current	4.5 - 5.5		30	65	mA
Write time	tFW(1)		• 128-byte write • including data erase • Excluding time to fetch 128 byte data	4.5 - 5.5		4.2	7.0	mS

Main system clock oscillation circuit characteristics

The characteristics in the table bellow is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer.

Table 1. Main system clock oscillation circuit characteristics using ceramic resonator

Frequency	Manufacturer	Oscillator	Circuit Parameters			Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rd1		typ	max	
10MHz	Murata	CSA10.0MTZ	33pF	33pF	0Ω	4.5 to 6.0V	0.05ms	0.50ms	
		CST10.0MTW	(30pF)	(30pF)	0Ω	4.5 to 6.0V	0.05ms	0.50ms	Built in C1,C2
	Kyocera	KBR-10.0M	33pF	33pF	0Ω	4.5 to 6.0V	0.05ms	0.50ms	
4MHz	Murata	CSA4.00MG	33pF	33pF	0Ω	4.5 to 6.0V	0.05ms	0.50ms	
		CST4.00MGW	(30pF)	(30pF)	0Ω	4.5 to 6.0V	0.05ms	0.50ms	Built in C1,C2
	Kyocera	KBR-4.0MSA	33pF	33pF	0Ω	4.5 to 6.0V	0.05ms	0.50ms	

*The oscillation stabilizing time is a period until the oscillation becomes stable after VDD becomes higher than minimum operating voltage. (Refer to Figure4)

Subsystem clock oscillation circuit characteristics

The characteristics in the table bellow is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer.

Table 2. Subsystem clock oscillation circuit characteristics using crystal oscillator

Frequency	Manufacturer	Oscillator	Circuit Parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C3	C4	Rf	Rd2		typ	max	
32.768kHz	Seiko EPSON	C-002Rx	12pF	15pF	OPEN	300kΩ	4.5 to 6.0V			

*The oscillation stabilizing time is a period until the oscillation becomes stable after executing the instruction which starts the sub-clock oscillation or after releasing the HOLD mode. (Refer to Figure4)

(Notes) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

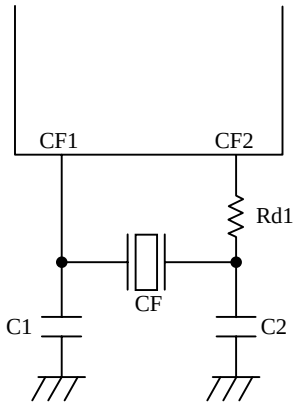


Figure 1 Ceramic oscillation circuit

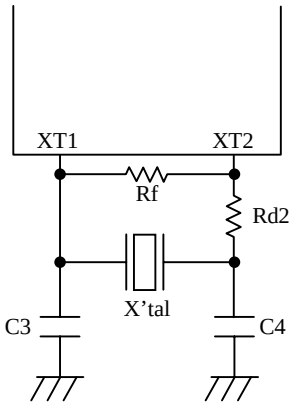


Figure 2 Crystal oscillation circuit

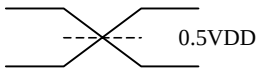
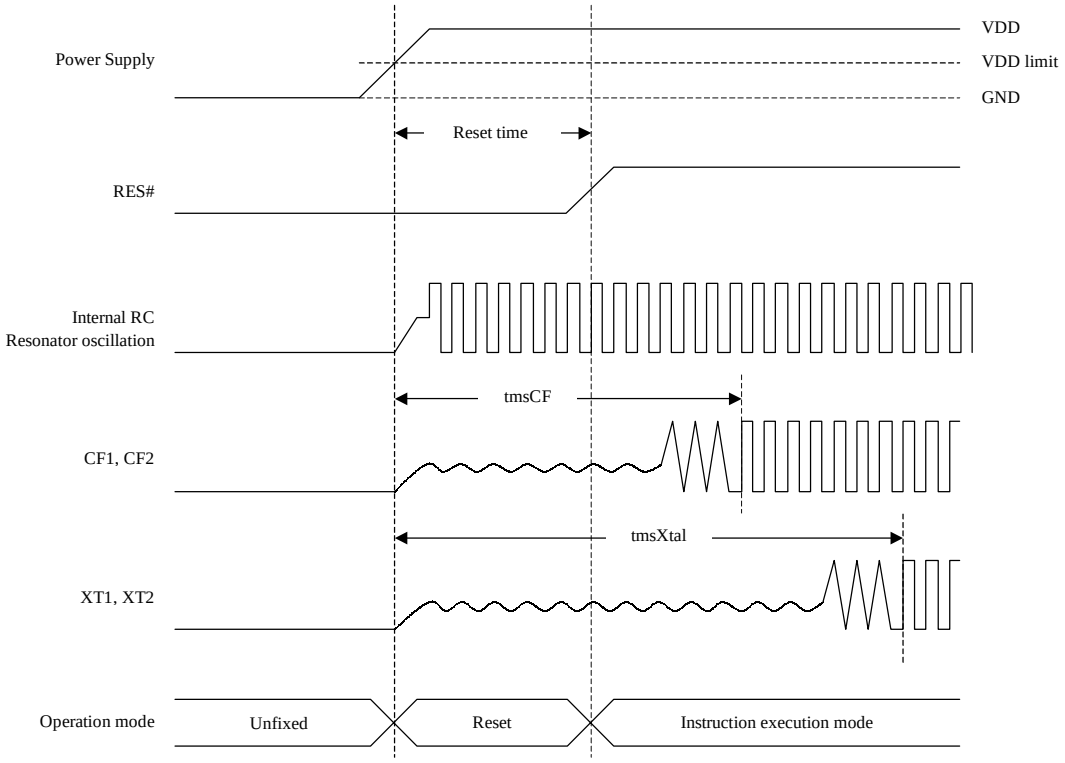
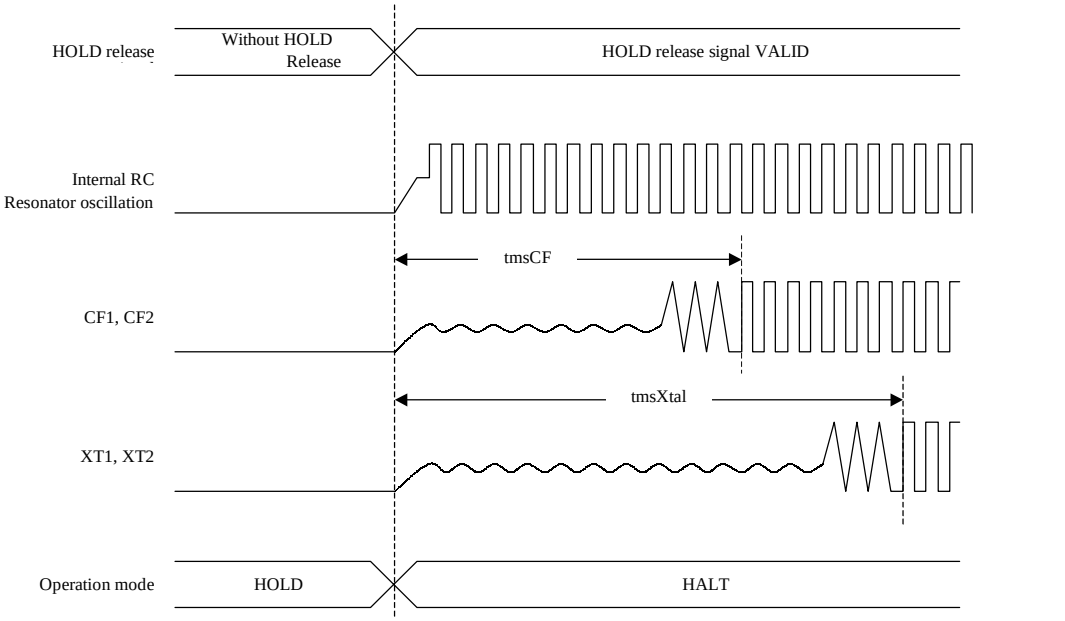


Figure 3 AC timing measurement point

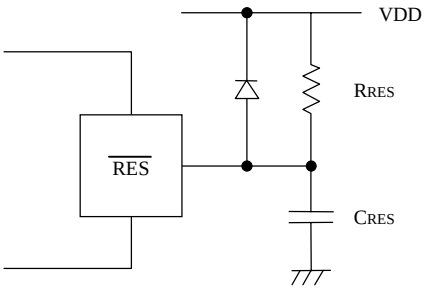


Reset time and oscillation stable time



HOLD release signal and oscillation stable time

Figure 4 Oscillation stabilizing time



(Note) Set CRES, RRES values such that reset time exceeds 200μs.

Figure 5 Reset circuit

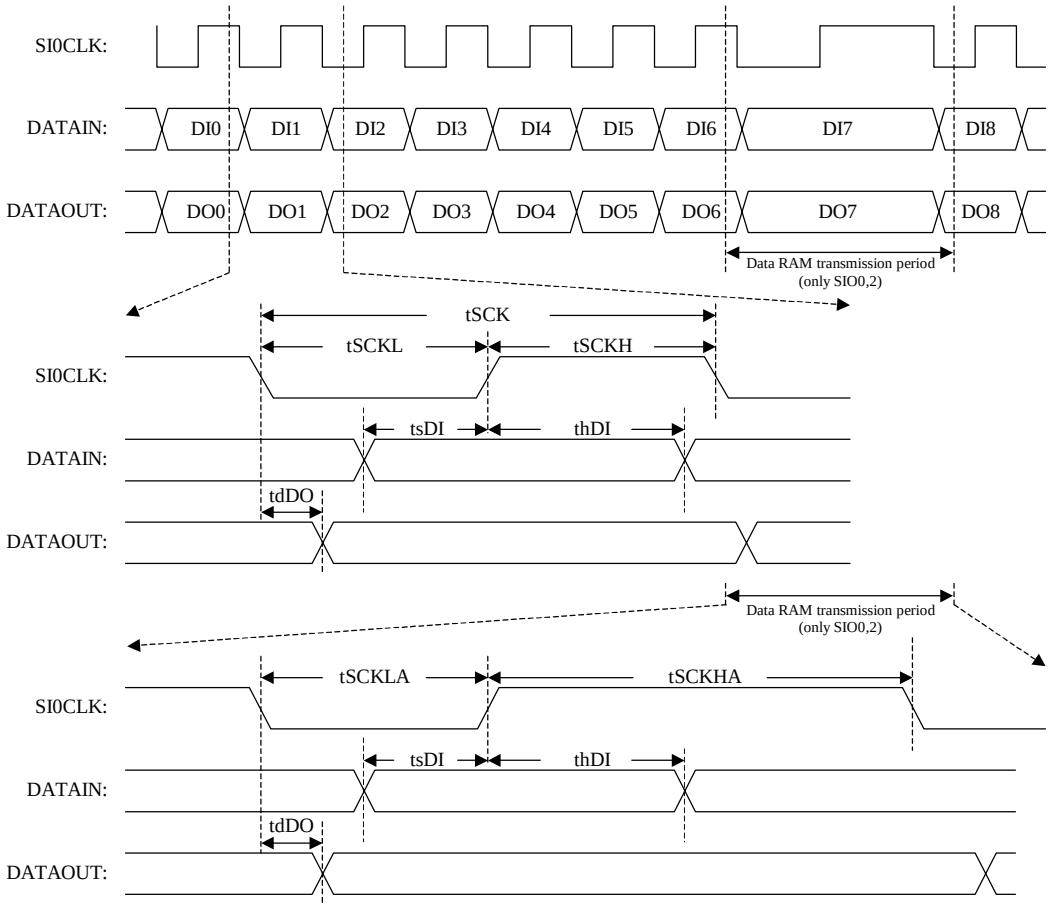


Figure 6 Serial input/output test condition

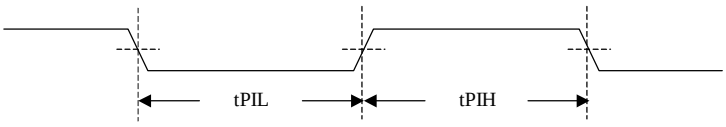
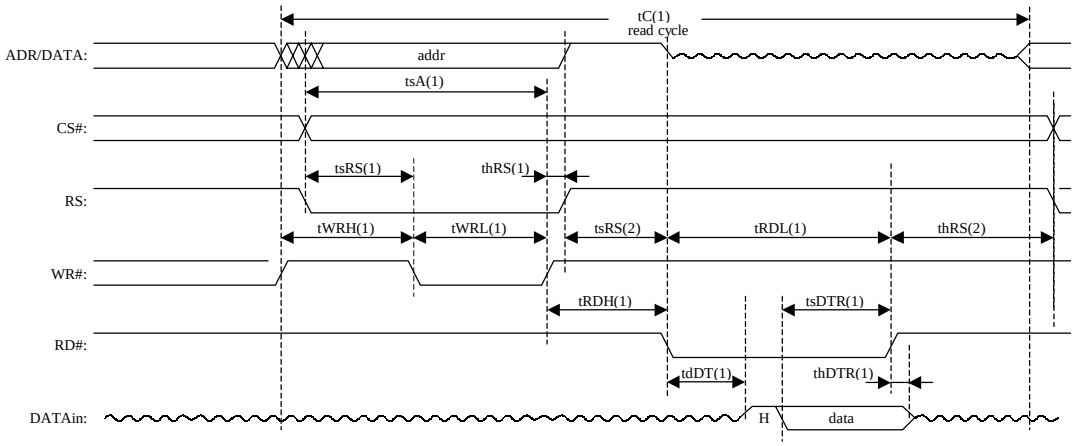


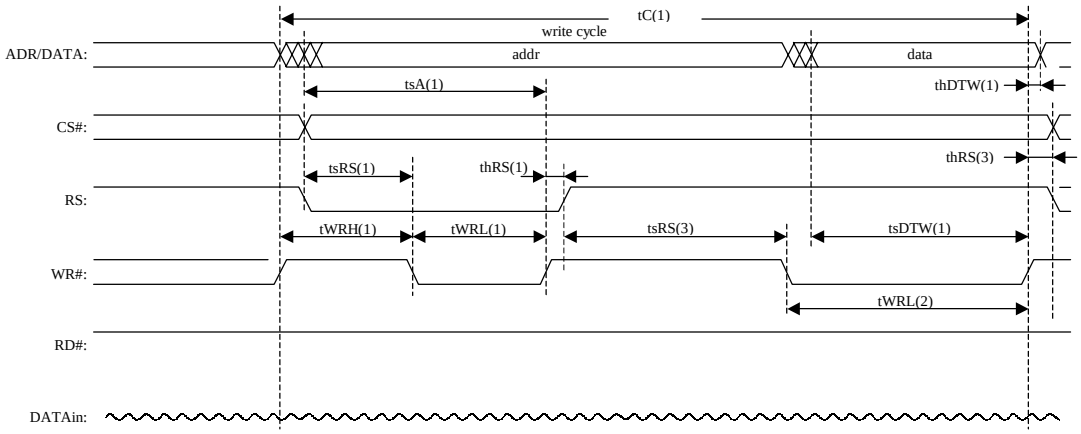
Figure 7 Pulse input timing condition

• Parallel Input/Output timing waveform : Indirect Setting, Read Mode



Note: Port A terminals used as RS, $\overline{WR}$, $\overline{RD}$ and $\overline{CS}$ should be set to CMOS format.

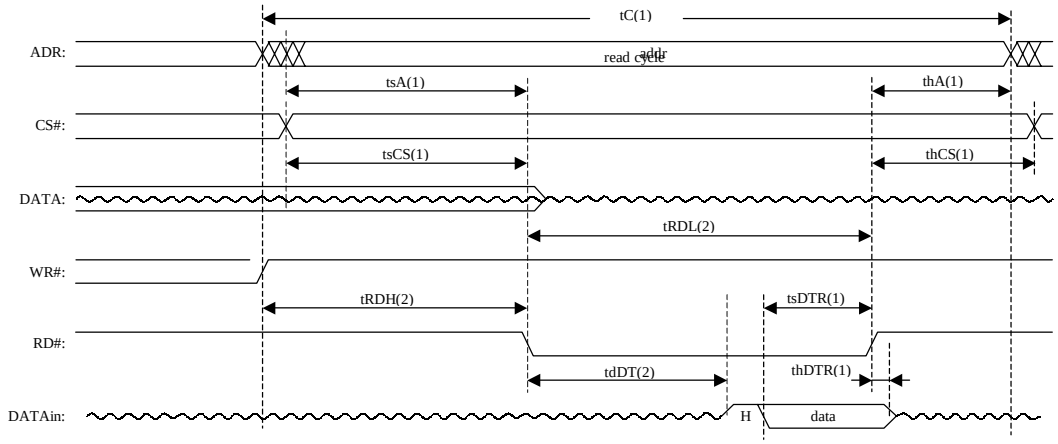
• Parallel Input/Output timing waveform : Indirect Setting, Write Mode



Note: Port A terminals used as RS, $\overline{WR}$, $\overline{RD}$ and $\overline{CS}$ should be set to CMOS format.

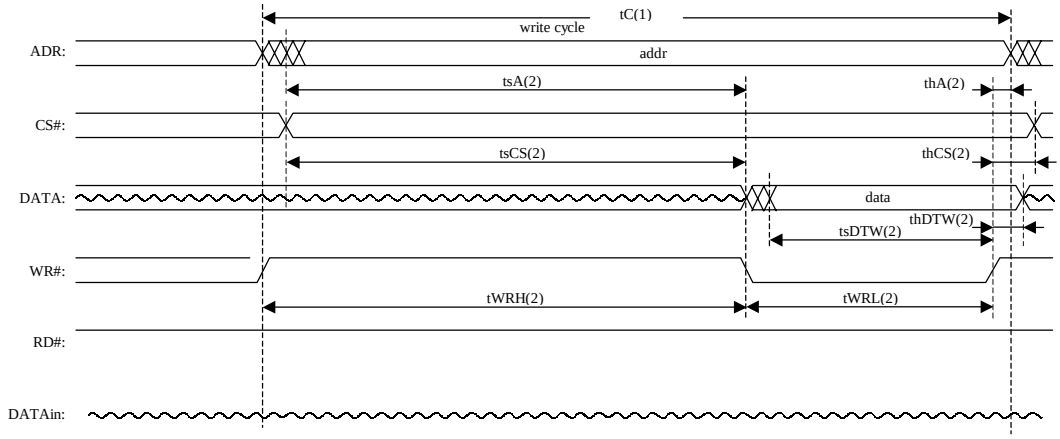
Figure 8 Indirect mode: Parallel Timing Waveforms

• Parallel Input/Output timing waveform : Direct Setting, Read Mode



Note: Port A terminals used as RS, $\overline{WR}$, $\overline{RD}$ and $\overline{CS}$ should be set to CMOS format.

• Parallel Input/Output timing waveform : Direct Setting, Write Mode



Note: Port A terminals used as RS, $\overline{WR}$, $\overline{RD}$ and $\overline{CS}$ should be set to CMOS format.

Figure 9 Direct Mode: Parallel Input/Output Timing Diagrams

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