

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS
524,288-WORD BY 16-BIT/1,048,576-WORD BY 8-BIT FULL CMOS STATIC RAM

DESCRIPTION

The TC55W800FT is a 8,388,608-bit static random access memory (SRAM) organized as 524,288 words by 16 bits/1,048,576 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.3V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 0.5 μ A standby current (at V_{DD}=3V, Ta=25°C, maximum) when chip enable ($\overline{CE1}$) is asserted high or ($\overline{CE2}$) is asserted low. There are three control inputs. $\overline{CE1}$ and $\overline{CE2}$ are used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. Data byte control pin (LB, UB) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to 85°C, the TC55W800FT can be used in environments exhibiting extreme temperature conditions. The TC55W800FT is available in a plastic 48-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 9.9 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.3V
- Power down features using $\overline{CE1}$ and $\overline{CE2}$
- Data retention supply voltage of 1.5 to 3.3V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby current (maximum)

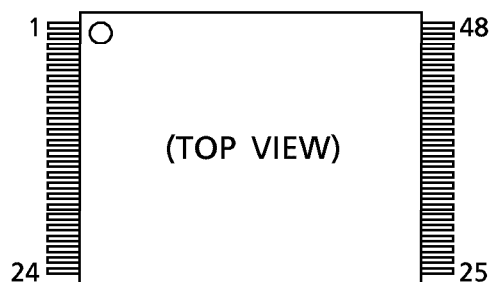
3.3V	10 μ A
3.0V	5 μ A

- Access Times (maximum):

	TC55W800FT	
	-55	-70
Access Time	55 ns	70 ns
$\overline{CE1}$ Access Time	55 ns	70 ns
$\overline{CE2}$ Access Time	55 ns	70 ns
\overline{OE} Access Time	30 ns	35 ns

- Package:
TSOP I 48-P-1220-0.50 (FT) (Weight : 0.52 g typ)

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 to A18	Address Inputs (Word Mode)
A-1 to A18	Address Inputs (Byte Mode)
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Input
R/W	Read / Write Control Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
I/O1 to I/O16	Data Inputs / Outputs
\overline{BYTE}	Byte($\times 8$ mode) Enable Input
V _{DD}	Power
GND	Ground
NC	No Connection

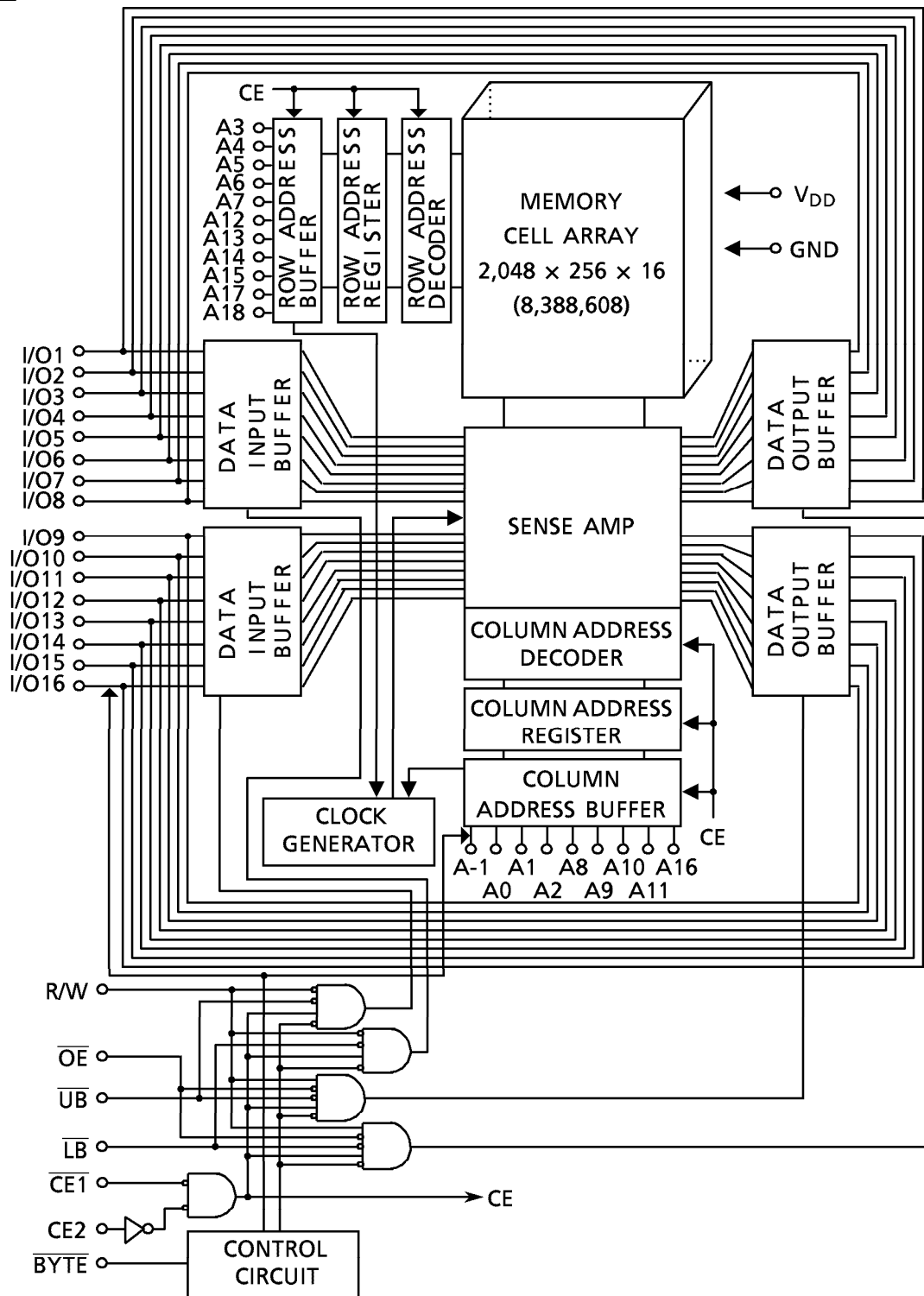
(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A15	A14	A13	A12	A11	A10	A9	A8	NC	NC	R/W	$\overline{CE2}$	NC	\overline{UB}	\overline{LB}	A18
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A17	A7	A6	A5	A4	A3	A2	A1	A0	$\overline{CE1}$	GND	\overline{OE}	I/O1	I/O9	I/O2	I/O10
Pin No.	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Pin Name	I/O3	I/O11	I/O4	I/O12	V _{DD}	I/O5	I/O13	I/O6	I/O14	I/O7	I/O15	I/O8	I/O16 / A-1	GND	\overline{BYTE}	A16

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BLOCK DIAGRAM



OPERATING MODE

MODE	CE1	CE2	OE	R/W	BYTE	LB	UB	I/O1 to 8	I/O9 to 15	I/O16	POWER
Read	L	H	L	H	L	*	*	D _{OUT}	High-Z	A-1	I _{DDO}
	L	H	L	H	H	L	L	D _{OUT}	D _{OUT}	D _{OUT}	I _{DDO}
	L	H	L	H	H	H	L	High-Z	D _{OUT}	D _{OUT}	I _{DDO}
	L	H	L	H	H	L	H	D _{OUT}	High-Z	High-Z	I _{DDO}
Write	L	H	*	L	L	*	*	D _{IN}	High-Z	A-1	I _{DDO}
	L	H	*	L	H	L	L	D _{IN}	D _{IN}	D _{IN}	I _{DDO}
	L	H	*	L	H	H	L	High-Z	D _{IN}	D _{IN}	I _{DDO}
	L	H	*	L	H	L	H	D _{IN}	High-Z	High-Z	I _{DDO}
Output Deselect	L	H	*	H	L	*	*	High-Z	High-Z	A-1	I _{DDO}
	L	H	*	H	H	L	L	High-Z	High-Z	High-Z	I _{DDO}
	L	H	*	H	H	H	L	High-Z	High-Z	High-Z	I _{DDO}
	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	I _{DDO}
Standby	H	*	*	*	H or L	*	*	High-Z	High-Z	High-Z	I _{DDS}
	*	L	*	*	H or L	*	*	High-Z	High-Z	High-Z	I _{DDS}

Note: x = don't care. H = logic high. L = logic low.

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 4.2	V
V _{IN}	Input Voltage	- 0.3 to 4.2	V
V _{I/O}	Input/Output Voltage	- 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg}	Storage Temperature	- 55 to 150	°C
T _{opr}	Operating Temperature	- 40 to 85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = - 40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	2.3	-	3.3	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3	-	V _{DD} × 0.22	V
V _{DH}	Data Retention Supply Voltage	1.5	-	3.3	V

DC CHARACTERISTICS (Ta = - 40° to 85°C, V_{DD} = 2.3 to 3.3V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT				
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}	-	-	± 1.0	μA				
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5 V	- 0.5	-	-	mA				
I _{OL}	Output Low Current	V _{OL} = 0.4 V	2.1	-	-	mA				
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} V _{OUT} = 0 V to V _{DD}	-	-	± 1.0	μA				
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} and I _{OUT} = 0 mA Other Input = V _{IH} /V _{IL} BYTE = V _{DD} or 0 V	Tcycle	55ns	-	-	60	mA		
I _{DDO2}				70ns	-	-	50			
				1 μs	-	-	10			
				55ns	-	-	55			
I _{DDO2}	Operating Current	CE1 = 0.2 V and CE2 = V _{DD} - 0.2 V and R/W = V _{DD} - 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} - 0.2 V/0.2 V BYTE = V _{DD} or 0 V	Tcycle	70ns	-	-	45			
				1 μs	-	-	5			
				I _{DDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL} , BYTE = V _{DD} or 0 V	-	-	2	mA
				I _{DDS2} (Note)			CE1 = V _{DD} - 0.2 V or CE2 = 0.2 V, V _{DD} = 1.5 to 3.3 V BYTE = V _{DD} or 0 V	V _{DD} = 3.0V ± 10%	Ta = 25°C	-
Ta = - 40 to 85°C	-	-	10							
V _{DD} = 3.0V	Ta = 25°C	-	0.05					0.5		
	Ta = - 40 to 40°C	-	-		1					
I _{DDS2} (Note)	Standby Current	CE1 = V _{DD} - 0.2 V or CE2 = 0.2 V, V _{DD} = 1.5 to 3.3 V BYTE = V _{DD} or 0 V	V _{DD} = 3.0V ± 10%	Ta = - 40 to 85°C	-	-	5			
				Ta = - 40 to 85°C	-	-	5			

Note: In standby mode with CE1 ≥ V_{DD} - 0.2V, these limits are assured for the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.7$ to 3.3V)READ CYCLE

SYMBOL	PARAMETER	TC55W800FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	55	–	70	–	ns
t_{ACC}	Address Access Time	–	55	–	70	
t_{CO1}	Chip Enable ($\overline{CE1}$) Access Time	–	55	–	70	
t_{CO2}	Chip Enable (CE2) Access Time	–	55	–	70	
t_{OE}	Output Enable Access Time	–	30	–	35	
t_{BA}	Data Byte Control Access Time	–	30	–	35	
t_{COE}	Chip Enable Low to Output Active	5	–	5	–	
t_{OEE}	Output Enable Low to Output Active	0	–	0	–	
t_{BE}	Data Byte Control Low to Output Active	0	–	0	–	
t_{OD}	Chip Enable High to Output High-Z	–	25	–	30	
t_{ODO}	Output Enable High to Output High-Z	–	25	–	30	
t_{BD}	Data Byte Control High to Output High-Z	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC55W800FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	55	–	70	–	ns
t_{WP}	Write Pulse Width	45	–	50	–	
t_{CW}	Chip Enable to End of Write	50	–	60	–	
t_{BW}	Data Byte Control to End of Write	45	–	50	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W Low to Output High-Z	–	25	–	30	
t_{OEW}	R/W High to Output Active	0	–	0	–	
t_{DS}	Data Setup Time	25	–	30	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

Output load: 30 pF + 1TTL Gate

Input pulse level: 0.4 V, 2.4 V

Timing measurements: $V_{DD} \times 0.5$

Reference level: $V_{DD} \times 0.5$

t_R, t_F : 5 ns

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.3$ to 3.3V)

READ CYCLE

SYMBOL	PARAMETER	TC55W800FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO1}	Chip Enable ($\overline{CE1}$) Access Time	–	70	–	85	
t_{CO2}	Chip Enable (CE2) Access Time	–	70	–	85	
t_{OE}	Output Enable Access Time	–	35	–	45	
t_{BA}	Data Byte Control Access Time	–	35	–	45	
t_{COE}	Chip Enable Low to Output Active	5	–	5	–	
t_{OEE}	Output Enable Low to Output Active	0	–	0	–	
t_{BE}	Data Byte Control Low to Output Active	0	–	0	–	
t_{OD}	Chip Enable High to Output High-Z	–	30	–	35	
t_{ODO}	Output Enable High to Output High-Z	–	30	–	35	
t_{BD}	Data Byte Control High to Output High-Z	–	30	–	35	
t_{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC55W800FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	55	–	
t_{CW}	Chip Enable to End of Write	60	–	70	–	
t_{BW}	Data Byte Control to End of Write	50	–	55	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W Low to Output High-Z	–	30	–	35	
t_{OEW}	R/W High to Output Active	0	–	0	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

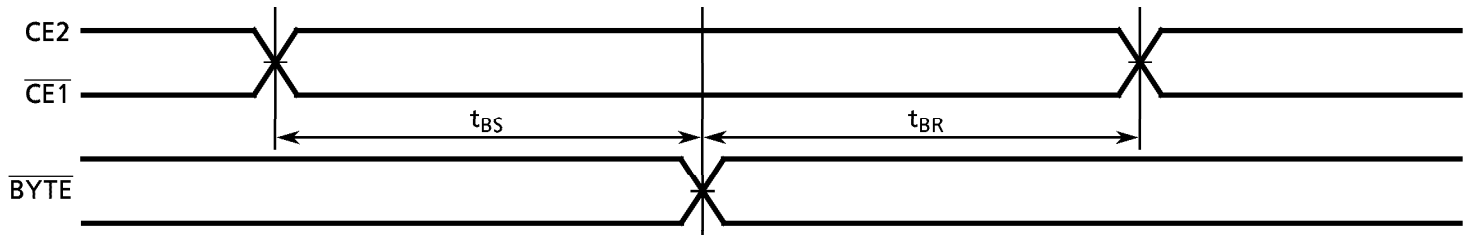
Output load: 30 pF + 1TTL Gate
 Input pulse level: $V_{DD} - 0.2\text{V}$, 0.2V
 Timing measurements: $V_{DD} \times 0.5$
 Reference level: $V_{DD} \times 0.5$
 t_R, t_F : 5 ns

BYTE FUNCTION

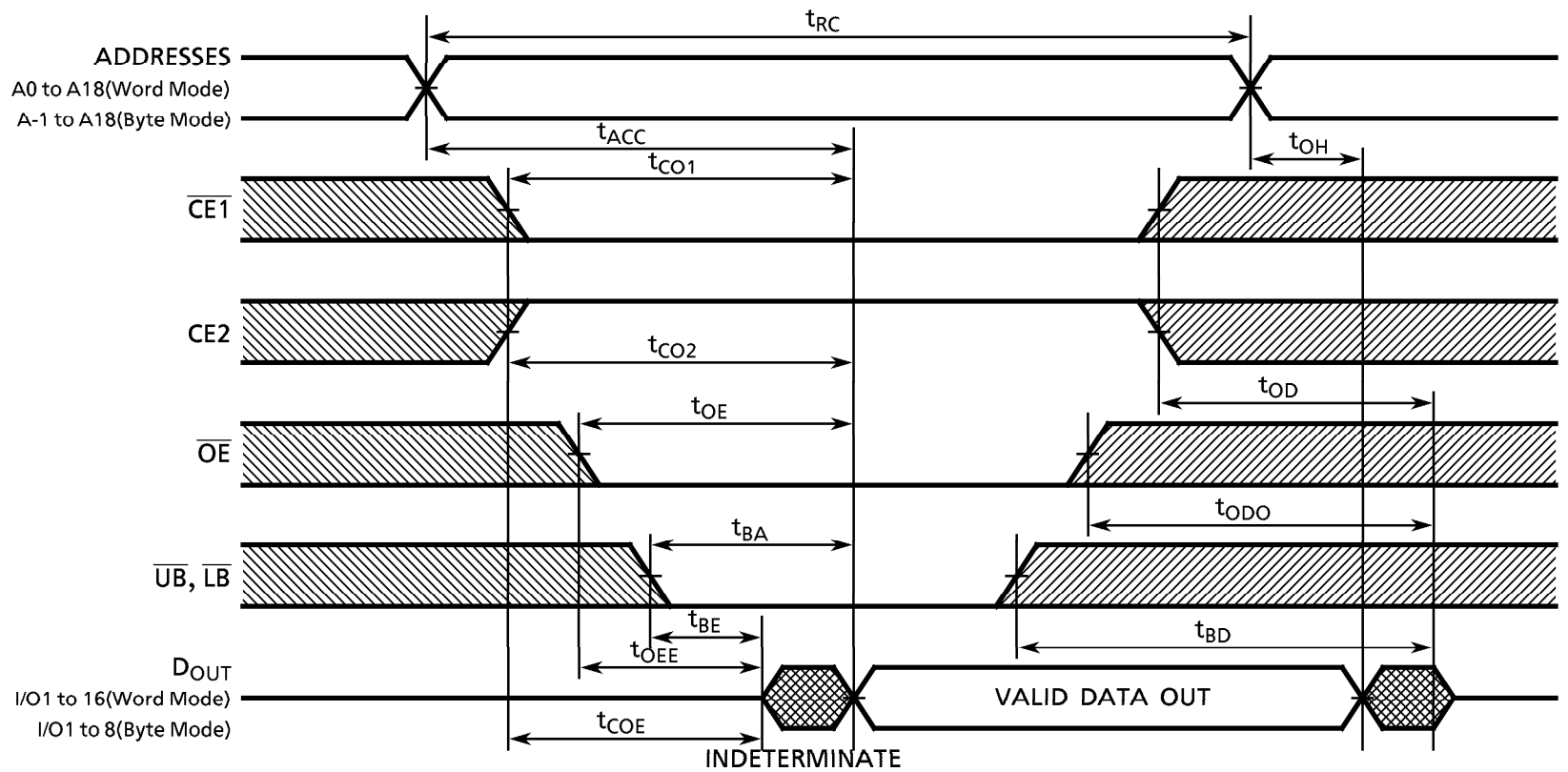
SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{BS}	BYTE Setup Time	5	–	ms
t_{BR}	BYTE Recovery Time	5	–	ms

TIMING DIAGRAMS

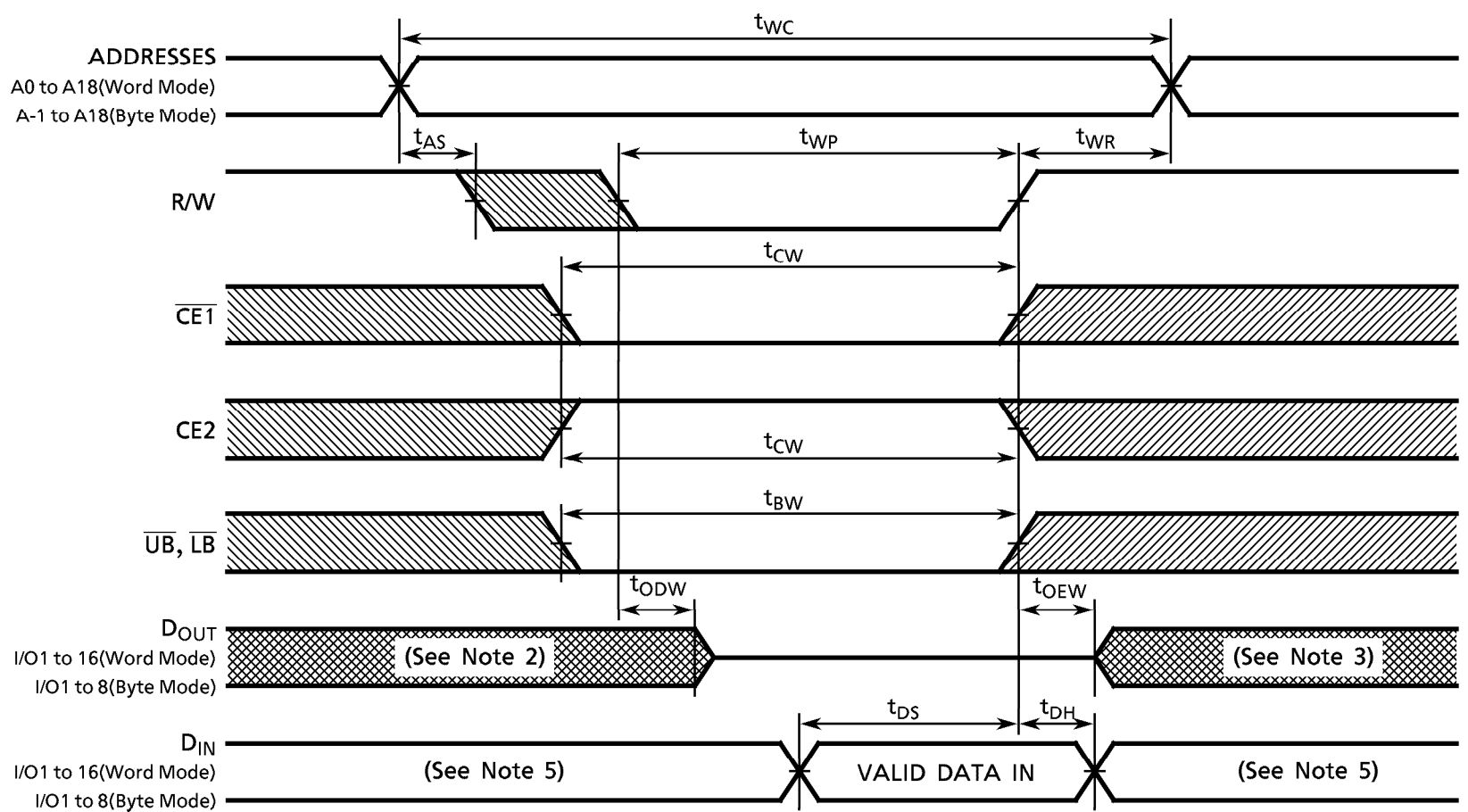
BYTE



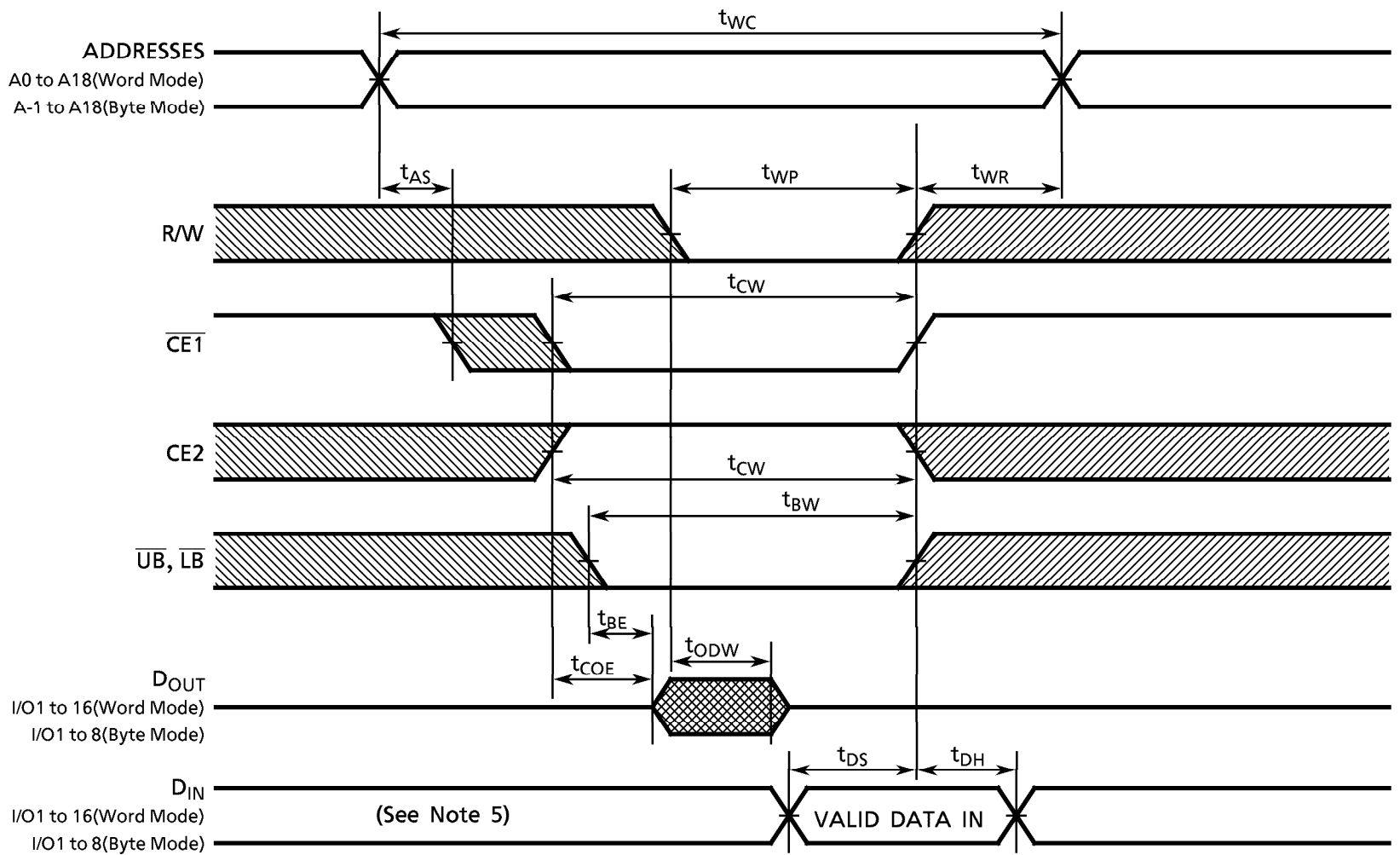
READ CYCLE (See Note 1)



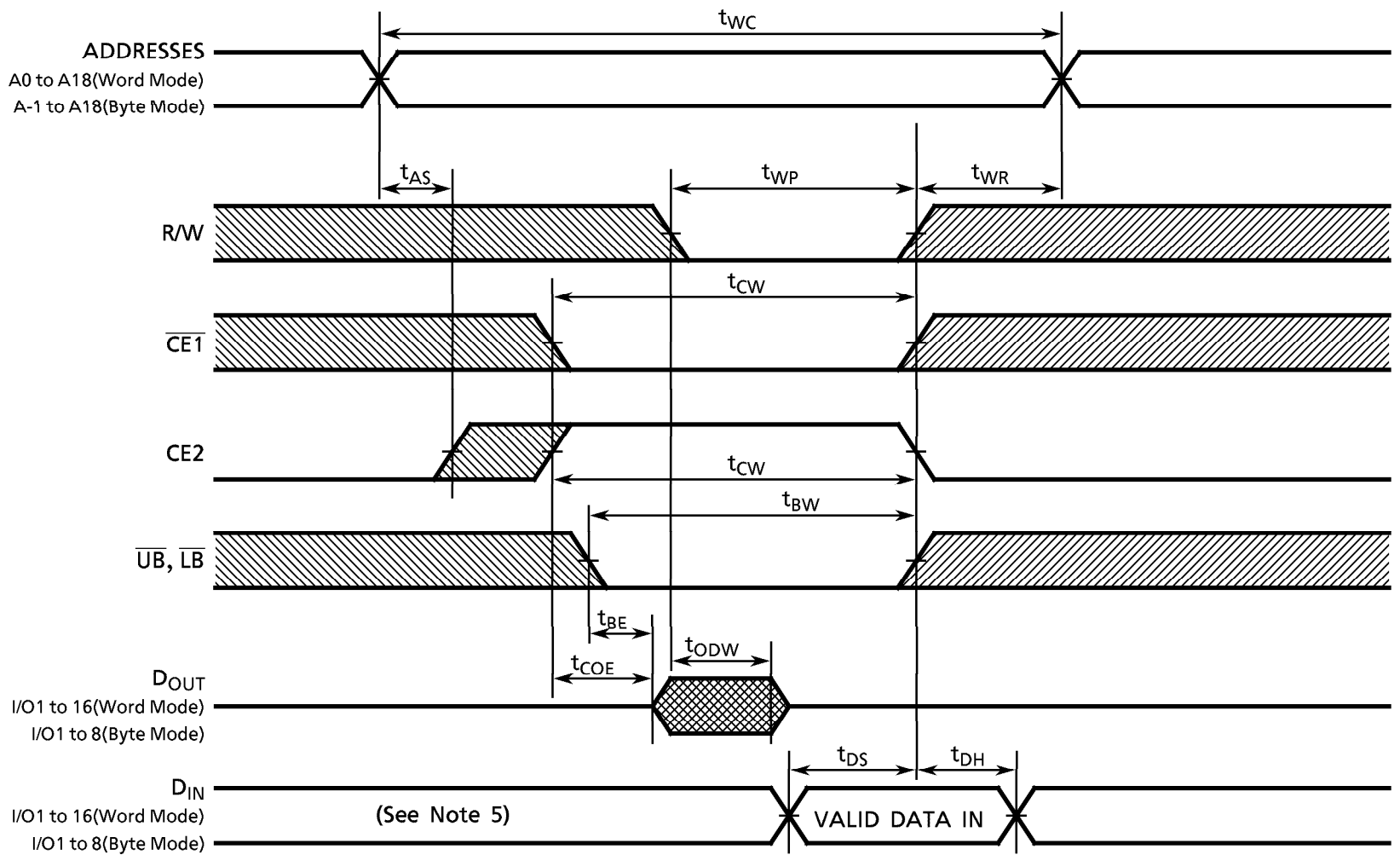
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



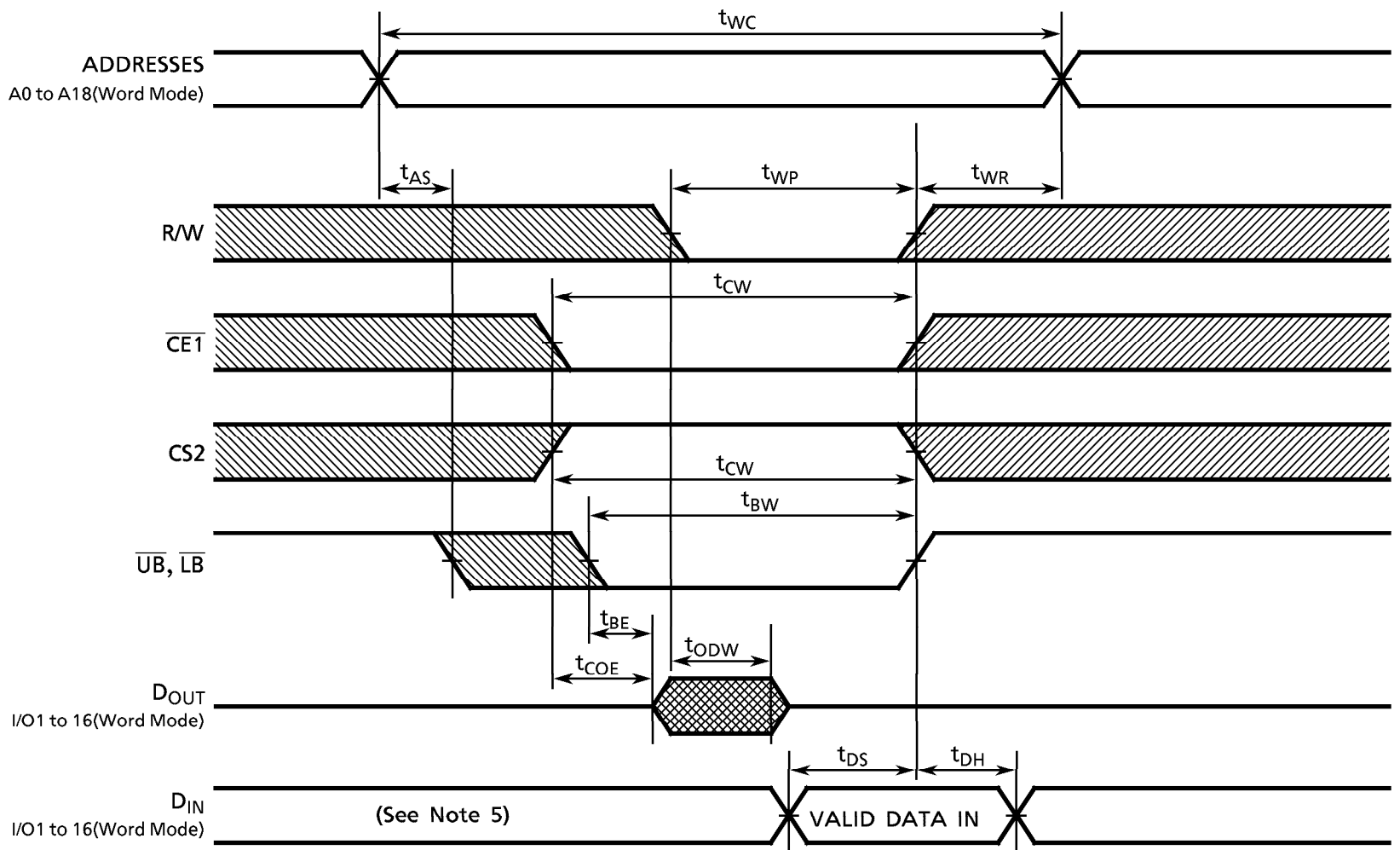
WRITE CYCLE 2 (CE1 CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



WRITE CYCLE 4 (\overline{UB} , \overline{LB} CONTROLLED) (See Note 4)



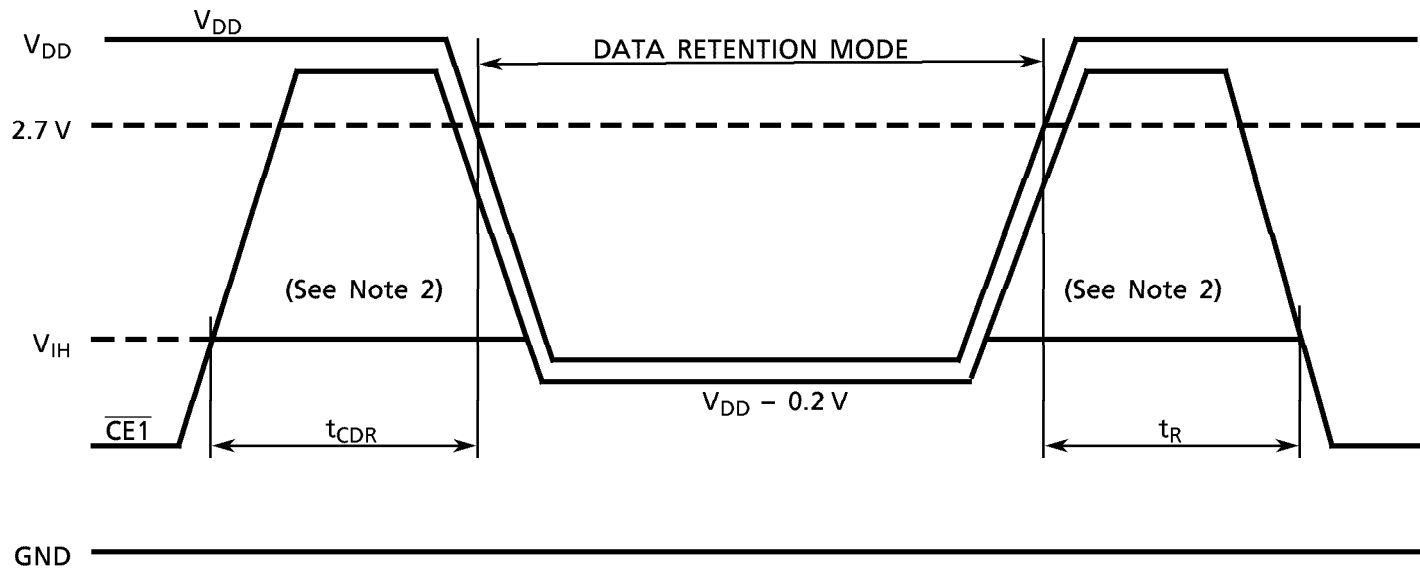
- Note:
- (1) R/W remains HIGH for the read cycle.
 - (2) If $\overline{CE1}$ goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
 - (3) If $\overline{CE1}$ goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
 - (4) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
 - (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

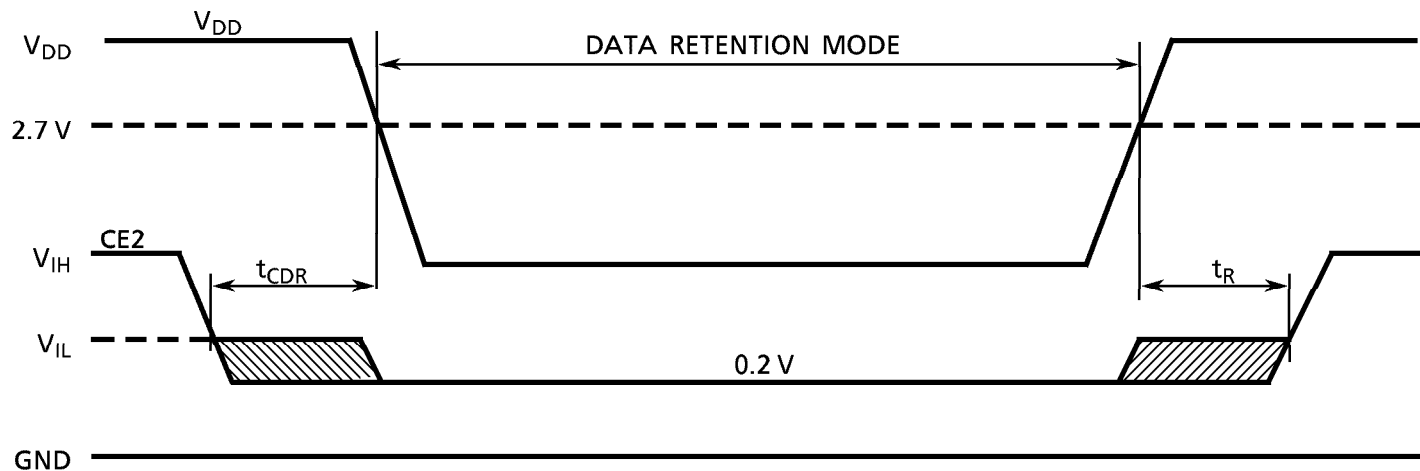
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V _{DH}	Data Retention Supply Voltage		1.5	-	3.3	V	
I _{DDS2}	Standby Current	V _{DH} = 3.3 V	Ta = -40° to 85°C	-	-	10	μA
		V _{DH} = 3.0 V	Ta = -40° to 40°C	-	-	1	
			Ta = -40° to 85°C	-	-	5	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	-	-	nS	
t _R	Recovery Time		t _{RC} (See Note)	-	-	nS	

Note: Read cycle time

CE1 CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



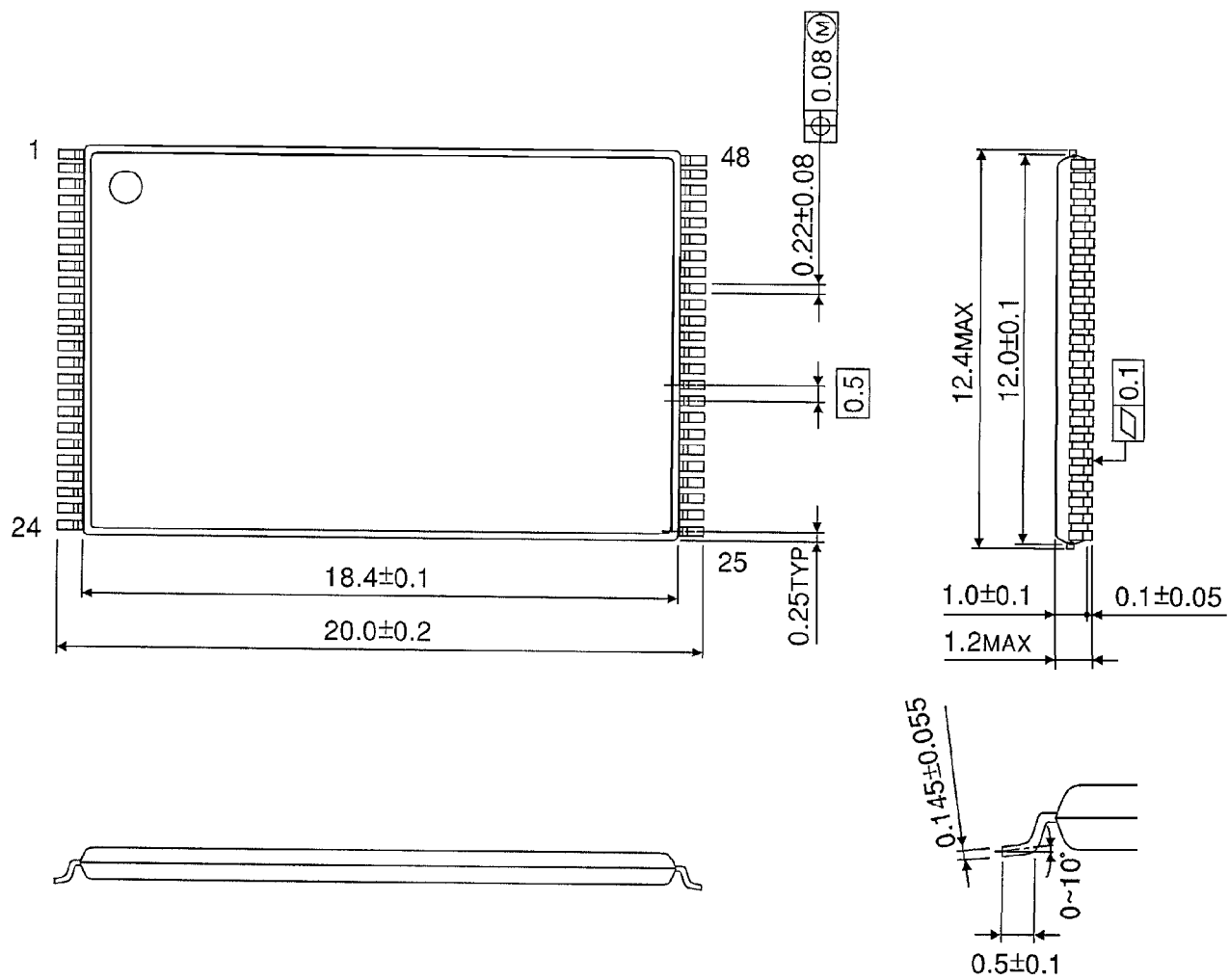
Note: (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when $CE2 \leq 0.2\text{ V}$ or $CE2 \geq V_{DD} - 0.2\text{ V}$.

(2) When $\overline{CE1}$ is operating at the V_{IH} level, the operating current is given by I_{DDS1} during the transition of V_{DD} from 2.7 to 2.3 V.

(3) In CE2 controlled data retention mode, minimum standby current mode is entered when $CE2 \leq 0.2\text{ V}$.

PACKAGE DIMENSIONS (TSOP I 48-P-1220-0.50)

Units in mm



Weight: 0.52 g (typ)