NEC

MOS INTEGRATED CIRCUIT
μPD23C24000

24M-BIT MASK-PROGRAMMABLE ROM
3M-WORD BY 8-BIT (BYTE MODE) / 1.5M-WORD BY 16-BIT (WORD MODE)

Description

The μPD23C24000 is a 25,165,824 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 3,145,728 words by 8 bits, WORD mode : 1,572,864 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C24000 are packed in 44-pin plastic SOP.

Features

- Word organization
  3,145,728 words by 8 bits (BYTE mode)
  1,572,864 words by 16 bits (WORD mode)
- Operating supply voltage : 5.0 V ± 0.5 V

Operating supply voltage V_{CC}	Access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
5.0 V ± 0.5 V	120	70	100

Ordering Information

Part number	Package
μPD23C24000GX-xxx	44-pin plastic SOP (600 mil)

(xxx : ROM code suffix No.)

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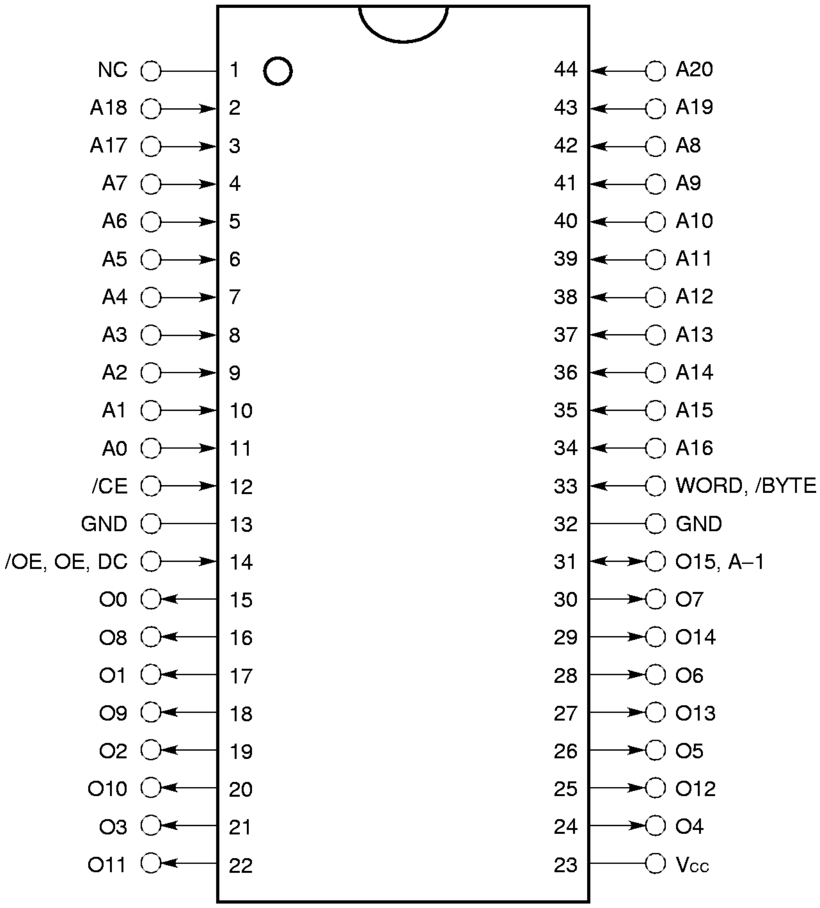
The mark ★ shows major revised points.

Pin Configuration (Marking Side)

/xxx indicates active low signal.

44-pin Plastic SOP (600 mil)
[μPD23C24000GX]



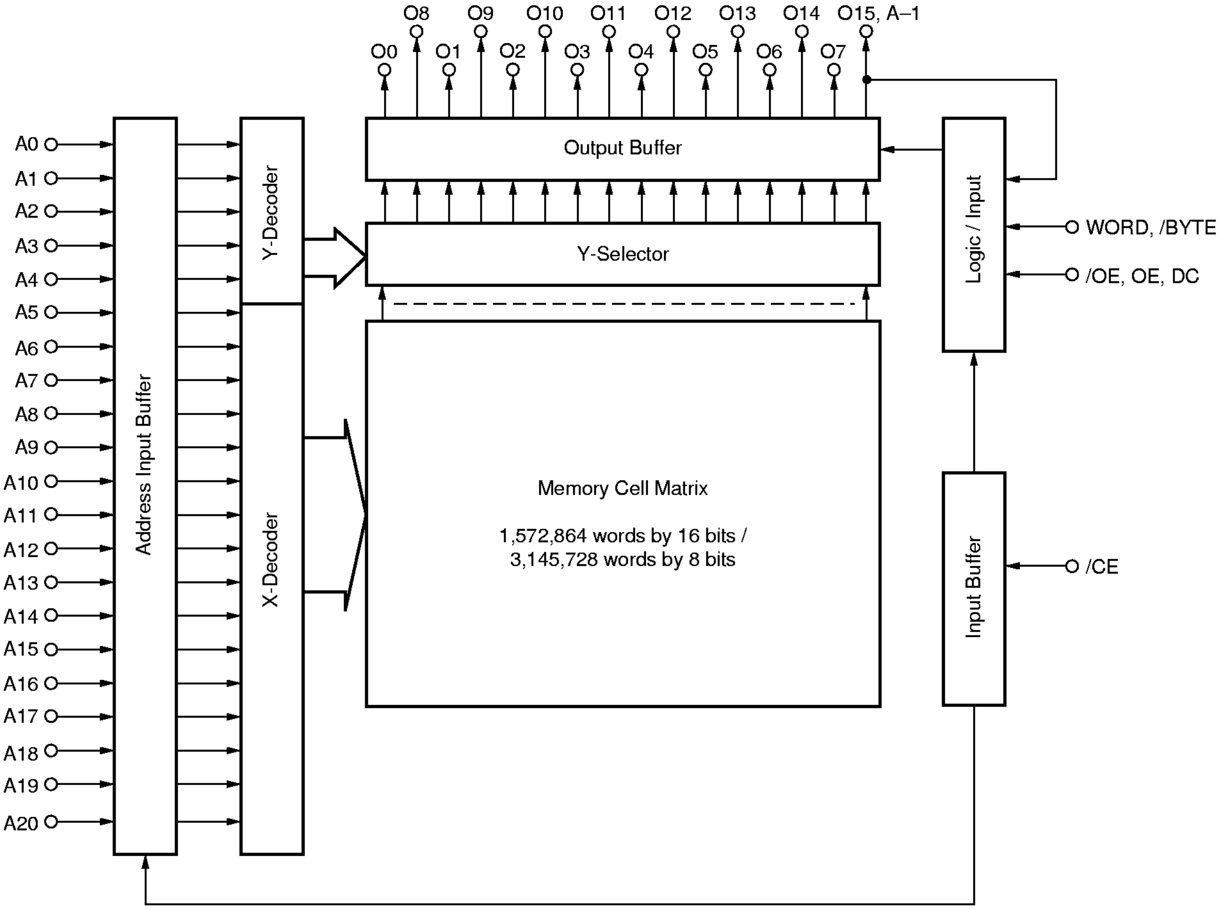
A0 - A20	:	Address inputs
O0 - O7, O8 - O14	:	Data Outputs
O15, A–1	:	Data 15 Output (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	:	Mode select
/CE	:	Chip Enable
/OE, OE	:	Output Enable
Vcc	:	Supply Voltage
GND	:	Ground
NC Note	:	No Connection
DC	:	Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching BYTE mode and WORD mode. **High level** : WORD mode (1.5M-word by 16-bit) **Low level** : BYTE mode (3M-word by 8-bit)
A0 to A20 (Address input)	Input	Address bus. A0 to A20 are used differently in the WORD mode and the BYTE mode. **WORD mode (1.5M-word by 16-bit)** A0 to A20 are used as 21 bits address signals. **BYTE mode (3M-word by 8-bit)** A0 to A20 are used as the upper 21 bits of total 22 bits of address signal. (The least significant bit (A–1) is combined to O15.)
O0 to O7, O8 to O14 (Data output)	Output	Output data bus. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. **WORD mode (1.5M-word by 16-bit)** The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A–1.) **BYTE mode (3M-word by 8-bit)** 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance. When A19 = "1" and A20 = "1", the output data is the same as when A19 = "0" and A20 = "1".
O15, A–1 (Data output 15, LSB address input)	Output, Input	O15, A–1 are used differently in the WORD mode and the BYTE mode. **WORD mode (1.5M-word by 16-bit)** The most significant output data bus (O15). **BYTE mode (3M-word by 8-bit)** The least significant address bus (A–1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level**: High impedance **Low level** : Data out
/OE, OE, DC (Output Enable, Don't Care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
GND	–	Ground
NC	–	Not internally connected (The signal can be connected).

Block Diagram



Mask Option

The active levels of output enable pin (/OE, OE, DC) are mask programmable and optional, and can be selected from among "0" "1" "×" shown in the table below.

Option	/OE, OE, DC	OE active level
0	/OE	L
1	OE	H
×	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option : ×)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

Remark L : Low level input
H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +7.0	V
Input voltage	V_I		–0.3 to V_{CC} + 0.3	V
Output voltage	V_O		–0.3 to V_{CC} + 0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 5.0 V ± 0.5 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.2		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
High level output voltage	V_{OH1}	I_{OH} = –400 μA	2.4			V
	V_{OH2}	I_{OH} = –100 μA	V_{CC} – 0.5			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}	–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected	–10		+10	μA
Power supply current	I_{CC1}	/CE = V_{IL} (Active mode), I_O = 0 mA			70	mA
Standby current	I_{CC2}	/CE = V_{IH} (Standby mode)			1.5	mA
	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)			100	μA

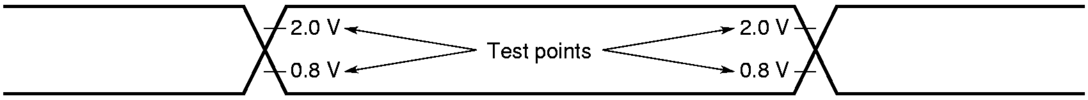
AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 5.0 V ± 0.5 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Address access time	t_{ACC}				120	ns
Chip enable access time	t_{CE}				120	ns
Output enable access time	t_{OE}				50	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		25	ns
WORD, /BYTE access time	t_{WB}				120	ns

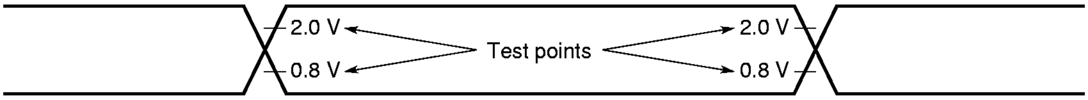
Remark t_{DF} is the time from inactivation of /CE or /OE, OE to high-impedance state output.

AC Test Conditions

Input Waveform (Rise / Fall Time ≤ 5 ns)



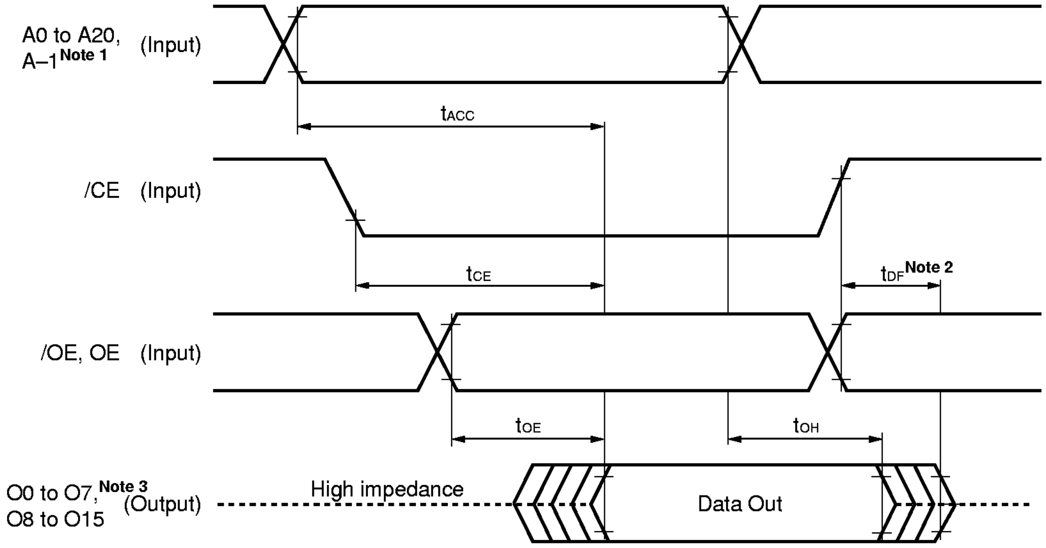
Output Waveform



Output Load

1 TTL + 100 pF

Read Cycle Timing Chart

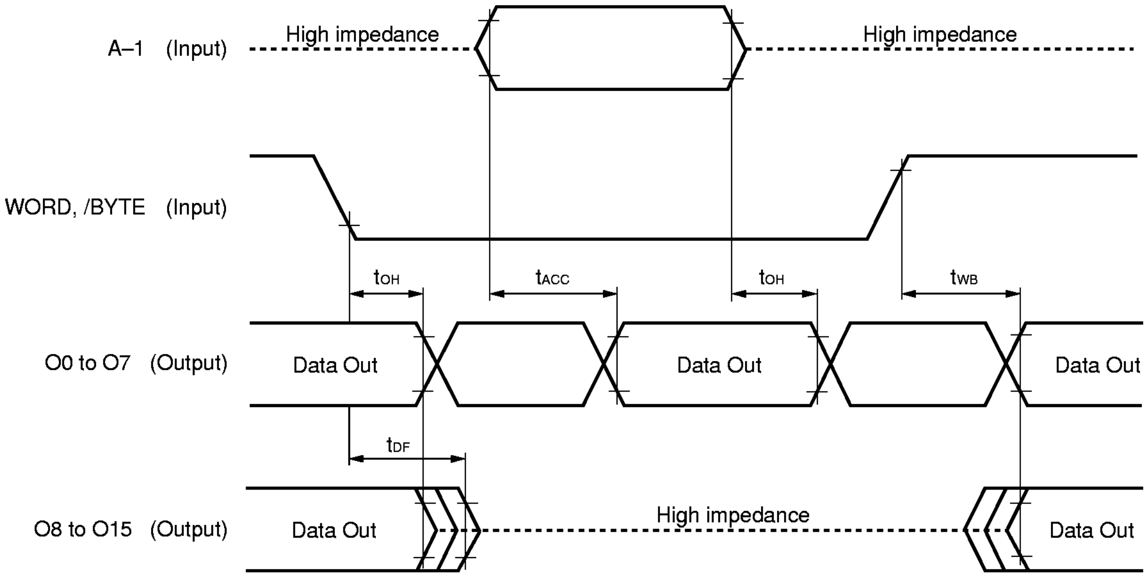


Notes 1. During WORD mode, A–1 is O15.

2. tDF is specified when one of /CE, /OE, OE is inactivated.

3. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

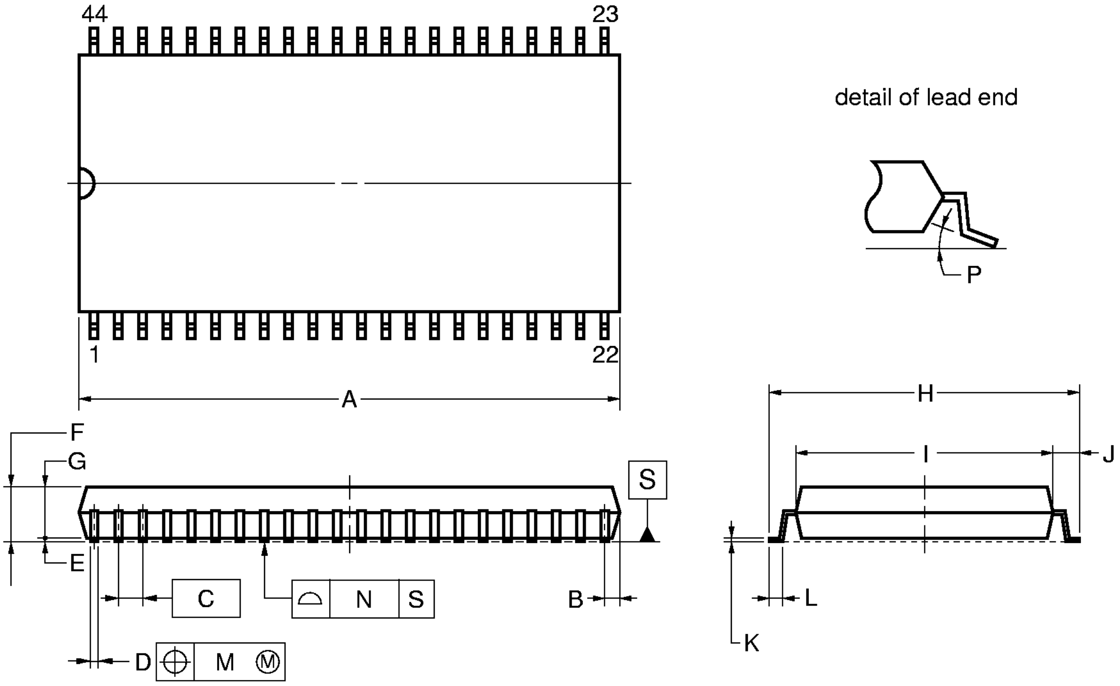
WORD, /BYTE Switch Timing Chart



Remark /OE, OE and /CE : Active.

Package Drawing

44 PIN PLASTIC SOP (600 mil)



NOTE

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$27.83^{+0.4}_{-0.05}$	$1.096^{+0.016}_{-0.003}$
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	$0.017^{+0.003}_{-0.004}$
E	0.15±0.1	0.006±0.004
F	3.0 MAX.	0.119 MAX.
G	2.7±0.05	$0.106^{+0.003}_{-0.002}$
H	16.04±0.3	$0.631^{+0.013}_{-0.012}$
I	13.24±0.1	$0.521^{+0.005}_{-0.004}$
J	1.4±0.2	0.055±0.008
K	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P44GX-50-600A-3

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C24000.

Types of Surface Mount Device

μPD23C24000GX : 44-pin plastic SOP (600 mil)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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NEC devices are classified into the following three quality grades:
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Standard:	Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
Special:	Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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Anti-radioactive design is not implemented in this product.

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