DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD26411

1M-BIT SRAM AND 2M-BIT MASK ROM COMBO CHIP
SRAM (128K-WORD BY 8-BIT) / MASK ROM (256K-WORD BY 8-BIT)

Description

The μPD26411 is a memory device combined 1,048,576 bits (131,072 words x 8 bits) CMOS static RAM and 2,097,152 bits (262,144 words x 8 bits) mask programmable ROM on one chip.

The μPD26411 is packed in 32-pin plastic TSOP (I).

Features

- Word organization
  - Static RAM : 131,072 words x 8 bits
  - Mask ROM : 262,144 words x 8 bits
- Power supply : V_{CC} = 1.8 to 3.3 V
- Access time (MAX.)
  - 500 ns : V_{CC} = 1.8 to 2.2 V
  - 375 ns : V_{CC} = 2.2 to 2.7 V
  - 250 ns : V_{CC} = 2.7 to 3.3 V
- ROM enable input : /ROMCS
- RAM enable input : /RAMCS

Ordering Information

Part Number	Package
μPD26411GZ-×××-KJH	32-pin plastic TSOP (I) (8 x 20 mm) (Normal bent)
μPD26411GZ-×××-KKH	32-pin plastic TSOP (I) (8 x 20 mm) (Reverse bent)

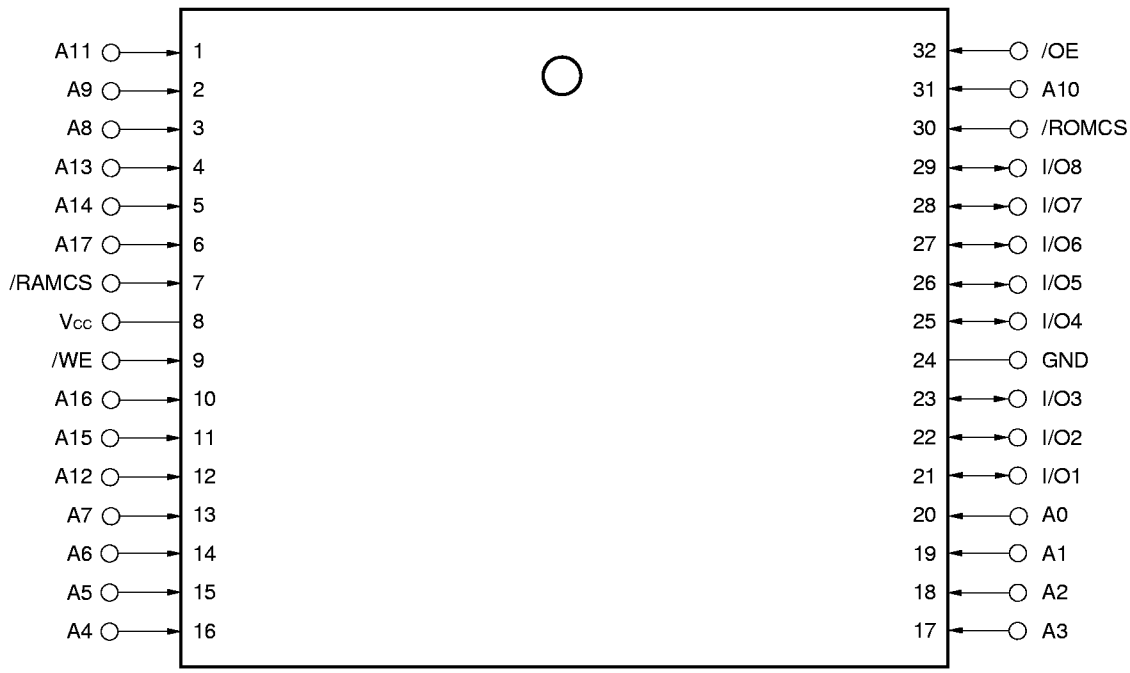
(××× : ROM code suffix)

Document No. M13604EJ1V0DS00 (1st edition)
Date Published June 1998 NS CP (K)
Printed in Japan

Pin Configuration (Marking Side)

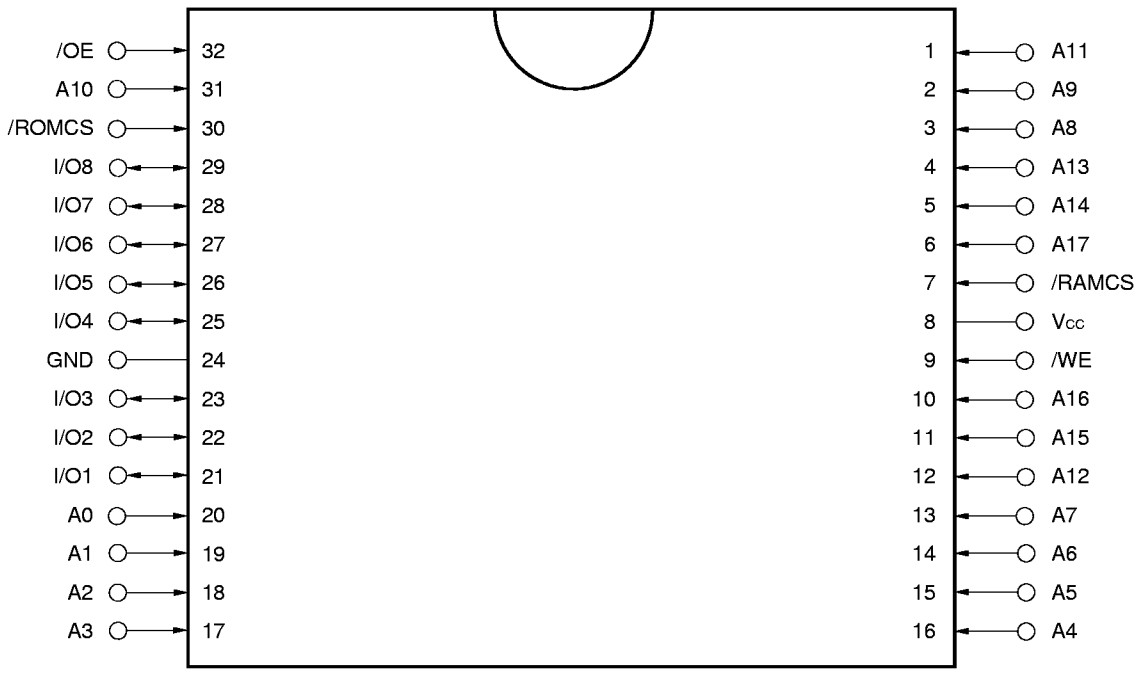
/xxx indicates active low signal.

32-pin plastic TSOP (I) (8 × 20 mm) (Normal bent)



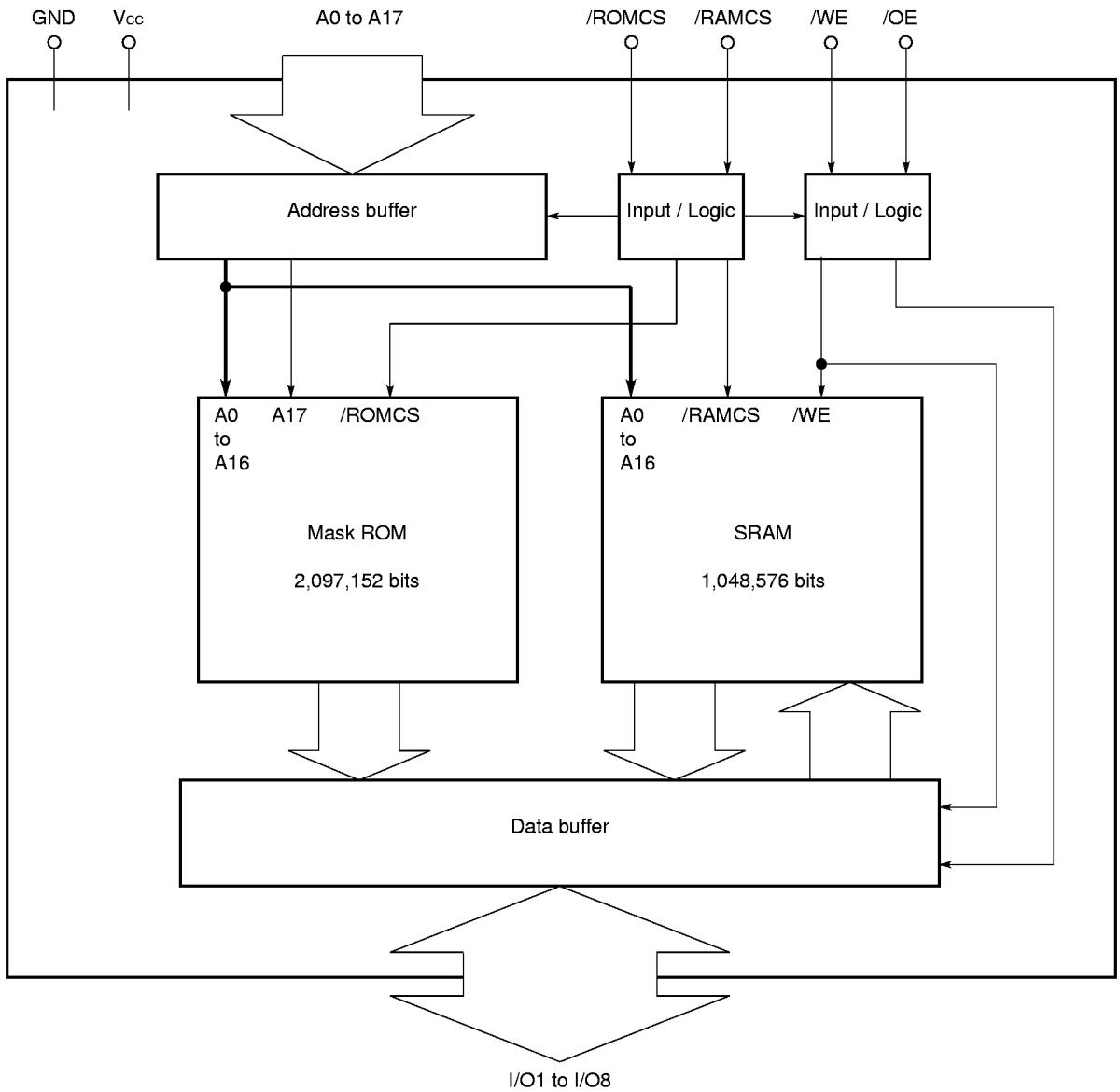
A0 - A17	:	Address inputs
I/O1 - I/O8	:	Data inputs/outputs
/OE	:	Output Enable
/WE	:	Write Enable
/ROMCS	:	ROM Enable
/RAMCS	:	RAM Enable
Vcc	:	Power supply
GND	:	Ground

32-pin plastic TSOP (I) (8 ×20 mm) (Reverse bent)



A0 - A17	:	Address inputs
I/O1 - I/O8	:	Data inputs/outputs
/OE	:	Output Enable
/WE	:	Write Enable
/ROMCS	:	ROM Enable
/RAMCS	:	RAM Enable
V_{CC}	:	Power supply
GND	:	Ground

Block Diagram



Truth Table

Address (A0 to A17)	/ROMCS	/RAMCS	/WE	/OE	I/O1 to I/O8	Mode
x	H	H	x	x	High impedance	Standby
	L	L	x	x		–
A0 to A17	L	H	x	H	High impedance	Output floating
	L	H	x	L	Data out	ROM read
Only A0 to A16 are valid	H	L	H	H	High impedance	Output floating
	H	L	H	L	Data out	RAM read
	H	L	L	x	Data in	RAM write

Remark H : High level, L : Low level, x : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input / Output voltage	V_T		–0.3 to V_{CC} + 0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			10	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN}: Input voltage.

2. These parameters are periodically sampled an1d not 100% tested.

DC Characteristics

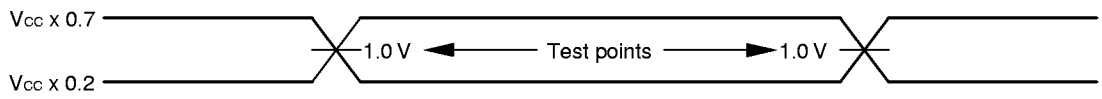
Parameter	Symbol	Test condition	Cycle = 500 ns		Cycle = 375 ns		Cycle = 250 ns		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		1.8	2.2	2.2	2.7	2.7	3.3	V
High level input voltage	V_{IH}		V_{CC} x 0.7	V_{CC} + 0.3	V_{CC} x 0.7	V_{CC} + 0.3	V_{CC} x 0.7	V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3	V_{CC} x 0.2	–0.3	+0.5	–0.3	+0.5	V
High level output voltage	V_{OH}	I_{OH} = –100 μA	V_{CC} – 0.4		V_{CC} – 0.4		V_{CC} – 0.4		V
Low level output voltage	V_{OL}	I_{OL} = +100 μA		0.4		0.4		0.4	V
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0	+1.0	–1.0	+1.0	–1.0	+1.0	μA
Output leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}	–1.0	+1.0	–1.0	+1.0	–1.0	+1.0	μA
Operating supply current ROM selected	IccROM	/ROMCS = V_{IL}, /RAMCS = V_{IH}, $I_{I/O}$ = 0 mA, V_{IH} = V_{CC} – 0.2 V, V_{IL} = 0.2 V, Cycle = MAX.		4		6		10	mA
Operating supply current RAM selected	IccRAM	/ROMCS = V_{IH}, /RAMCS = V_{IL}, $I_{I/O}$ = 0 mA, V_{IH} = V_{CC} – 0.2 V, V_{IL} = 0.2 V, Cycle = MAX.		4		6		10	mA
Standby supply current	IccS	/ROMCS = V_{IH}, /RAMCS = V_{IH}, V_{IH} = V_{CC} – 0.2 V, V_{IL} = 0.2 V		6.5		8		10	μA

AC Characteristics

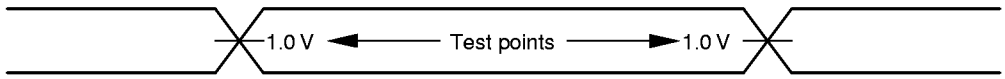
AC Test Conditions

[Vcc = 1.8 to 2.2 V]

Input waveform (Rise and fall time ≤ 5 ns)

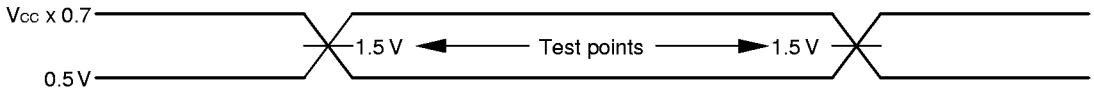


Output waveform

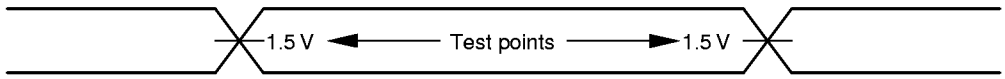


[Vcc = 2.2 to 3.3 V]

Input waveform (Rise and fall time ≤ 5 ns)



Output waveform



Output load

1TTL + 30 pF

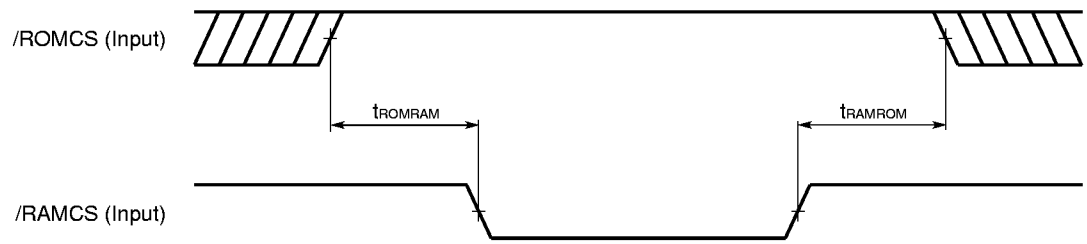
ROM - RAM Selection

ROM - RAM Selection Cycle (V_{CC} = 1.8 to 3.3 V, T_A = –10 to +70 °C)

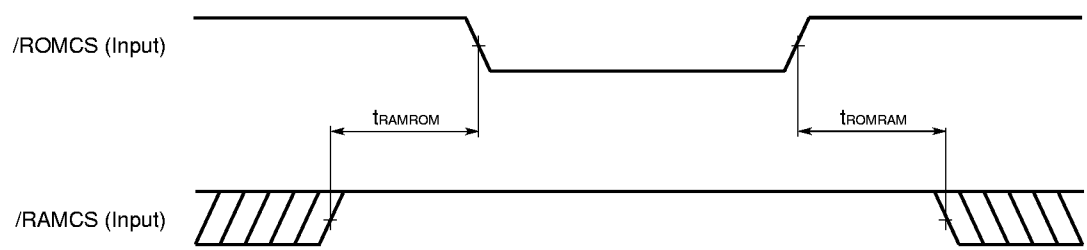
Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Disable /ROMCS to enable /RAMCS time	t_{ROMRAM}		10			ns
Disable /RAMCS to enable /ROMCS time	t_{RAMROM}		10			ns

ROM – RAM Selection Timing Chart

ROM ⟶ RAM



RAM ⟶ ROM



ROM Selected (/ROMCS = L, /RAMCS = H)

ROM Read Cycle (1) (V_{CC} = 1.8 to 2.2 V, T_A = –10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}		500			ns
Address access time	t_{ACC}				500	ns
Chip enable access time	t_{ROMCS}				500	ns
Output enable access time	t_{OE}				250	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		175	ns
/ROMCS to output low impedance	t_{LZ}		10			ns
/OE to output low impedance	t_{OLZ}		5			ns

Remark t_{DF} is the time from inactivation of /ROMCS or /OE to high-impedance state output.

ROM Read Cycle (2) (V_{CC} = 2.2 to 2.7 V, T_A = –10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}		375			ns
Address access time	t_{ACC}				375	ns
Chip enable access time	t_{ROMCS}				375	ns
Output enable access time	t_{OE}				175	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		125	ns
/ROMCS to output low impedance	t_{LZ}		10			ns
/OE to output low impedance	t_{OLZ}		5			ns

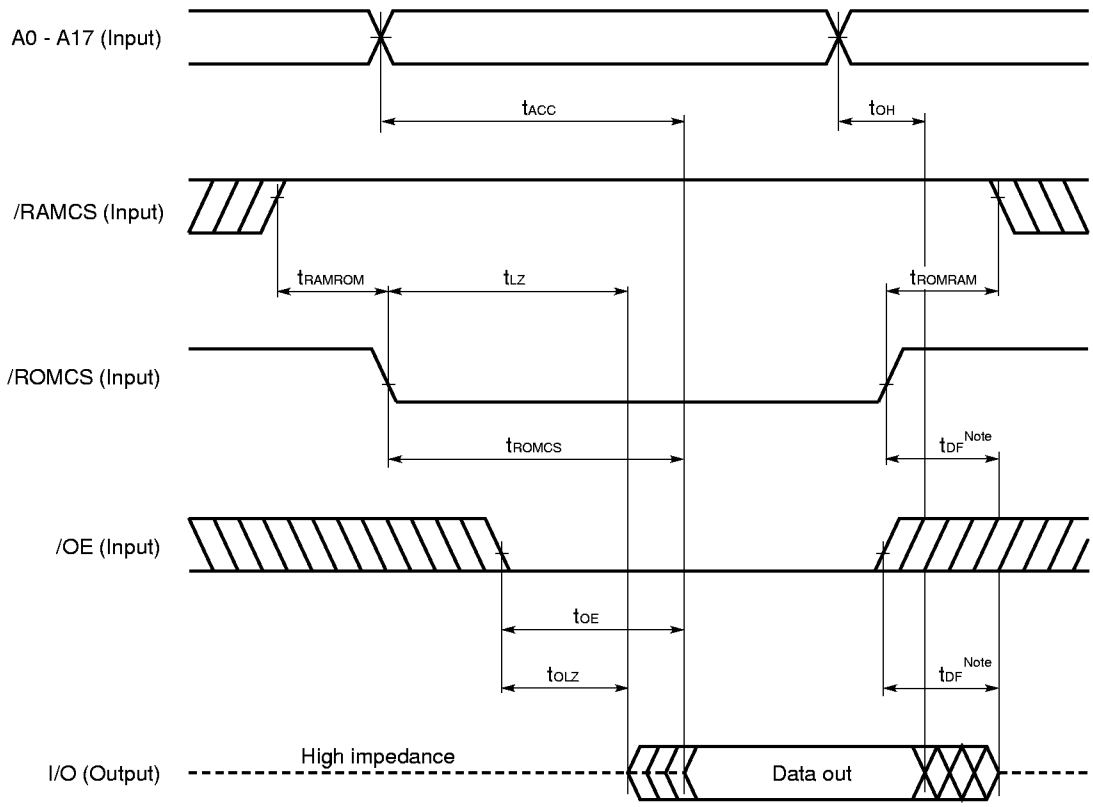
Remark t_{DF} is the time from inactivation of /ROMCS or /OE to high-impedance state output.

ROM Read Cycle (3) (V_{CC} = 2.7 to 3.3 V, T_A = –10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}		250			ns
Address access time	t_{ACC}				250	ns
Chip enable access time	t_{ROMCS}				250	ns
Output enable access time	t_{OE}				100	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		100	ns
/ROMCS to output low impedance	t_{LZ}		10			ns
/OE to output low impedance	t_{OLZ}		5			ns

Remark t_{DF} is the time from inactivation of /ROMCS or /OE to high-impedance state output.

ROM Read Cycle Timing Chart



Note t_{DF} is specified when one of /ROMCS and /OE is inactivated.

RAM Selected (/ROMCS = H, /RAMCS = L)

RAM Read Cycle (1) (V_{CC} = 1.8 to 2.2 V, T_A = –10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}		500			ns
Address access time	t_{ACC}				500	ns
Chip enable access time	t_{RAMCS}				500	ns
Output enable access time	t_{OE}				250	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		175	ns
/RAMCS to output low impedance	t_{LZ}		10			ns
/OE to output low impedance	t_{OLZ}		5			ns

Remark t_{DF} is the time from inactivation of /RAMCS or /OE to high-impedance state output.

RAM Read Cycle (2) (V_{CC} = 2.2 to 2.7 V, T_A = –10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}		375			ns
Address access time	t_{ACC}				375	ns
Chip enable access time	t_{RAMCS}				375	ns
Output enable access time	t_{OE}				175	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		125	ns
/RAMCS to output low impedance	t_{LZ}		10			ns
/OE to output low impedance	t_{OLZ}		5			ns

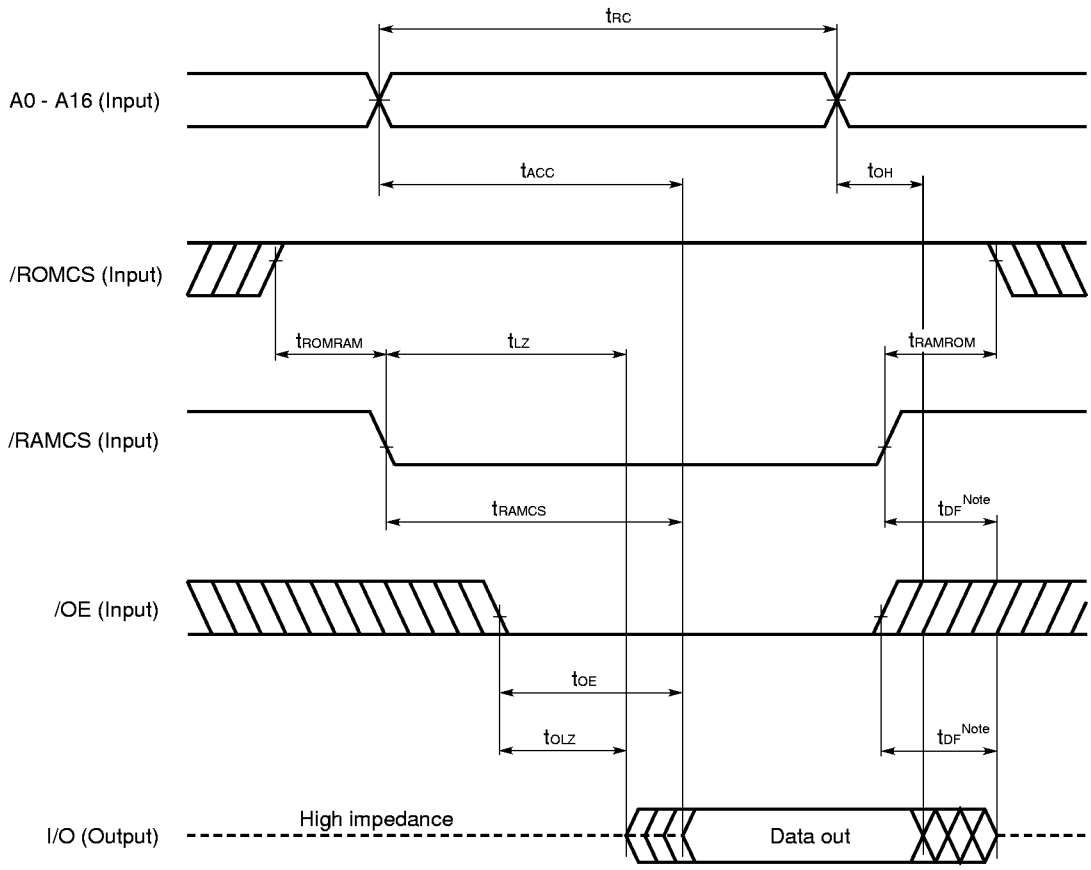
Remark t_{DF} is the time from inactivation of /RAMCS or /OE to high-impedance state output.

RAM Read Cycle (3) (V_{CC} = 2.7 to 3.3 V, T_A = –10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Read cycle time	t_{RC}		250			ns
Address access time	t_{ACC}				250	ns
Chip enable access time	t_{RAMCS}				250	ns
Output enable access time	t_{OE}				100	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		100	ns
/RAMCS to output low impedance	t_{LZ}		10			ns
/OE to output low impedance	t_{OLZ}		5			ns

Remark t_{DF} is the time from inactivation of /RAMCS or /OE to high-impedance state output.

RAM Read Cycle Timing Chart



Note t_{DF} is specified when one of /RAMCS and /OE is inactivated.

Remark In read cycle, /WE should be fixed to high level.

RAM Write Cycle (1) (V_{CC} = 1.8 to 2.2 V, T_A = −10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Write cycle time	t_{WC}		500			ns
Chip enable to end write	t_{RAMCW}		300			ns
Address valid to end of write	t_{AW}		300			ns
Address setup time	t_{AS}		0			ns
Write pulse width	t_{WP}		300			ns
Write recovery time	t_{WR}		0			ns
Data valid to end of write	t_{DW}		125			ns
Data hold time	t_{DH}		0			ns
/WE to output in high impedance	t_{WHZ}				125	ns
Output active from end of write	t_{OW}		5			ns

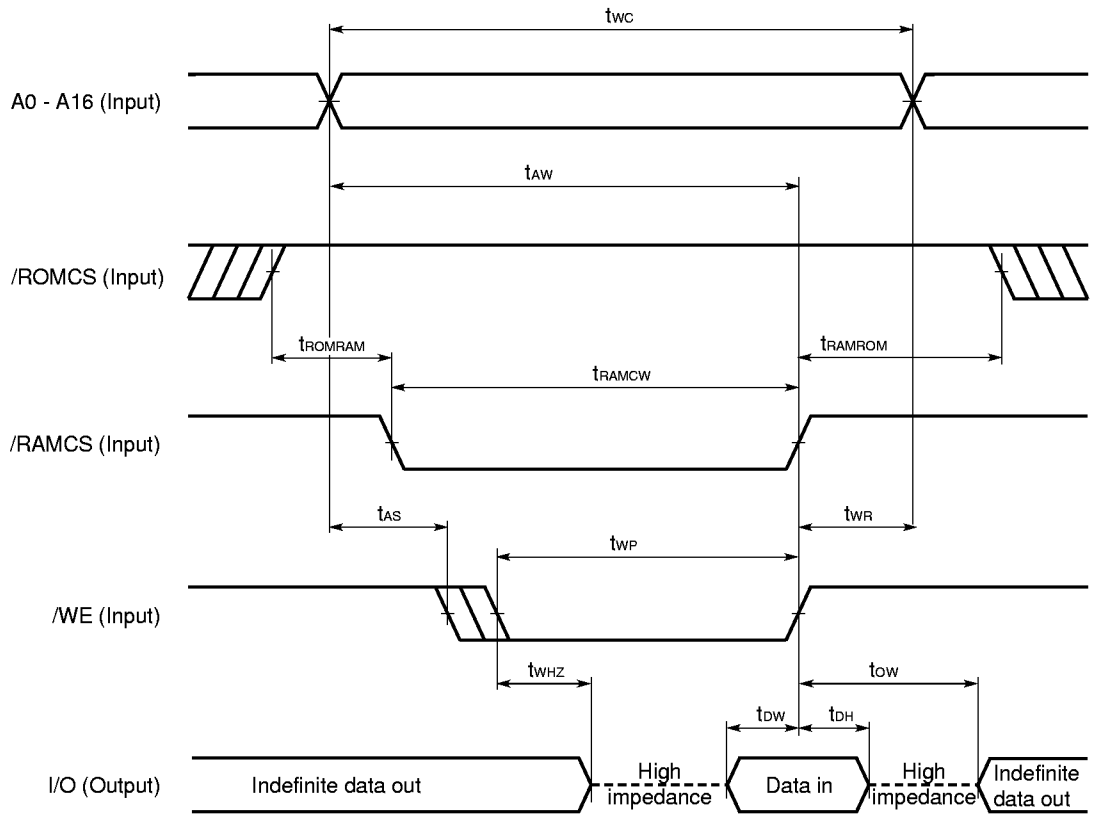
RAM Write Cycle (2) (V_{CC} = 2.2 to 2.7 V, T_A = −10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Write cycle time	t_{WC}		375			ns
Chip enable to end write	t_{RAMCW}		250			ns
Address valid to end of write	t_{AW}		250			ns
Address setup time	t_{AS}		0			ns
Write pulse width	t_{WP}		250			ns
Write recovery time	t_{WR}		0			ns
Data valid to end of write	t_{DW}		110			ns
Data hold time	t_{DH}		0			ns
/WE to output in high impedance	t_{WHZ}				100	ns
Output active from end of write	t_{OW}		5			ns

RAM Write Cycle (3) (V_{CC} = 2.7 to 3.3 V, T_A = −10 to +70 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Write cycle time	t_{WC}		250			ns
Chip enable to end write	t_{RAMCW}		200			ns
Address valid to end of write	t_{AW}		200			ns
Address setup time	t_{AS}		0			ns
Write pulse width	t_{WP}		200			ns
Write recovery time	t_{WR}		0			ns
Data valid to end of write	t_{DW}		100			ns
Data hold time	t_{DH}		0			ns
/WE to output in high impedance	t_{WHZ}				75	ns
Output active from end of write	t_{OW}		5			ns

RAM Write Cycle Timing Chart (/WE Controlled)



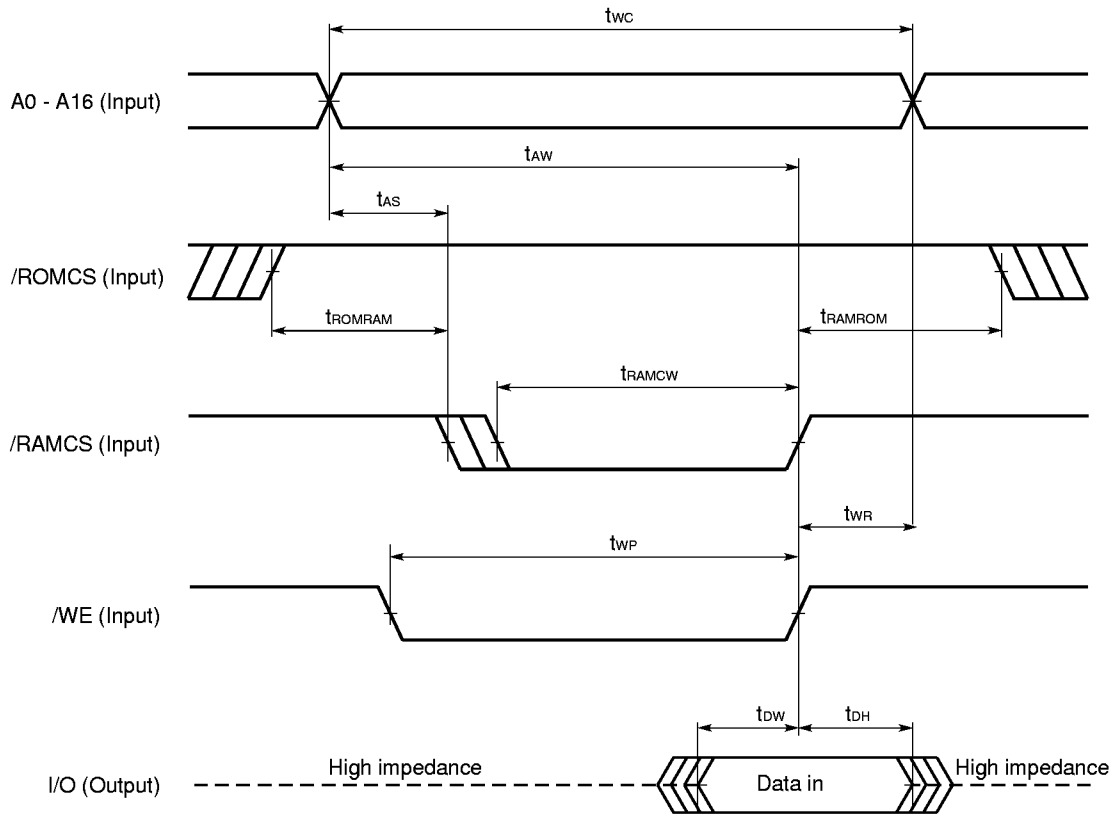
Cautions 1. /RAMCS or /WE should be fixed to high level during address transition.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remarks 1. Write operation is done during the overlap time of a low level /RAMCS and a low level /WE.

2. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

RAM Write Cycle Timing Chart (/RAMCS Controlled)



Cautions 1. /RAMCS or /WE should be fixed to high level during address transition.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

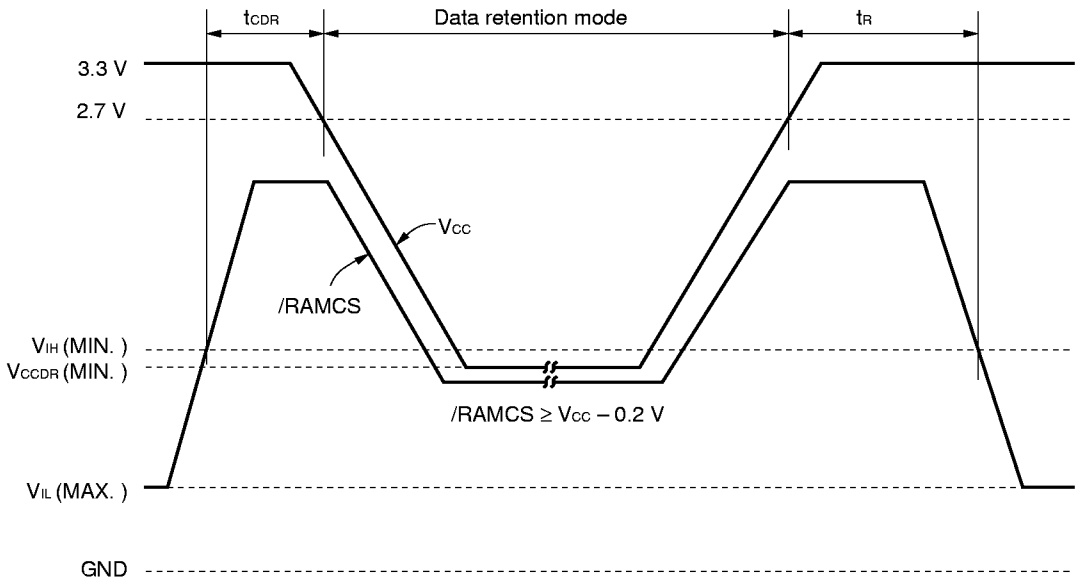
Remarks 1. Write operation is done during the overlap time of a low level /RAMCS and a low level /WE.

2. /OE = High level.

Low V_{CC} Data Retention Characteristics (T_A = –10 to + 70 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR}	/RAMCS ≥ V_{CC} – 0.2 V	1.5		3.3	V
Data retention supply current	I_{CCDR}	/RAMCS ≥ V_{CC} – 0.2 V, /ROMCS ≥ V_{CC} – 0.2 V , V_{CC} = 3.0 V			10	μA
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

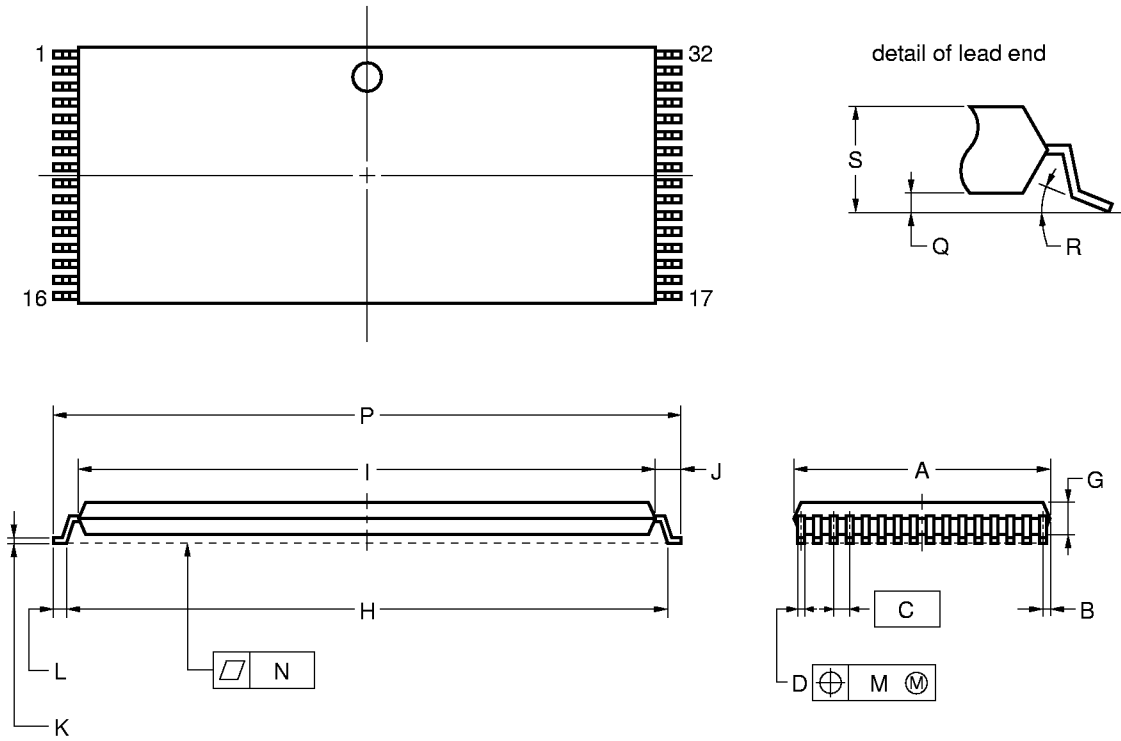
Data Retention Timing Chart



Remark The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

32 PIN PLASTIC TSOP (I) (8×20)



NOTES

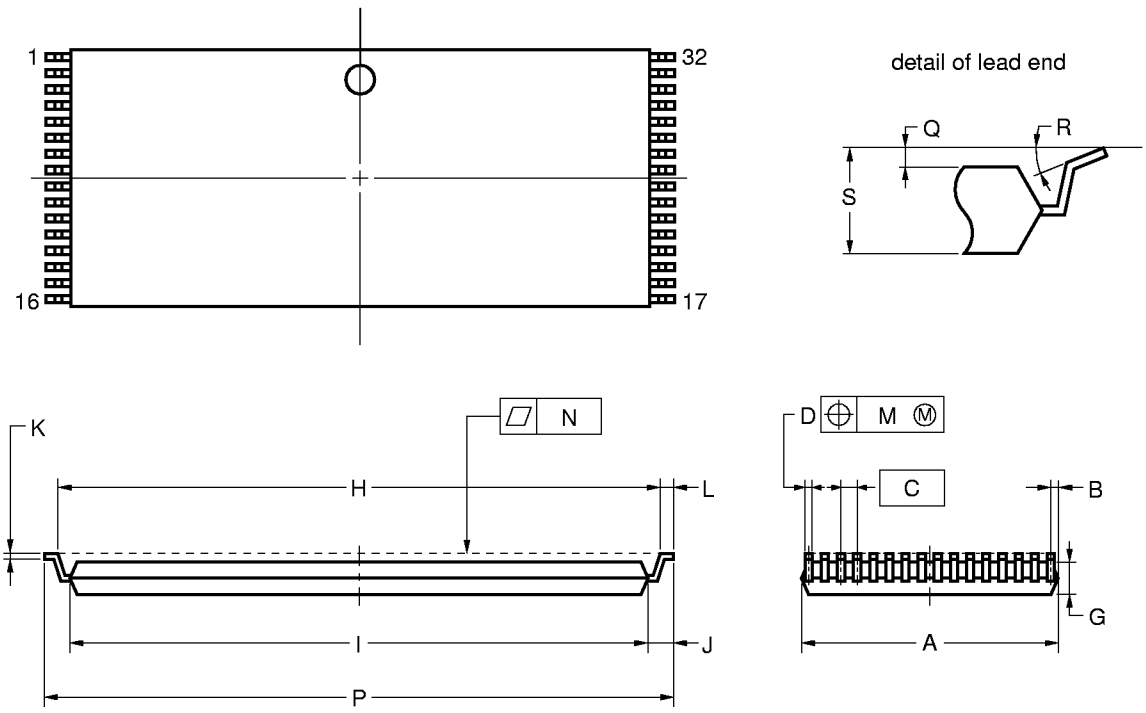
(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	19.0±0.2	0.748±0.008
I	18.4±0.2	$0.724^{+0.009}_{-0.008}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.1 MAX.	0.044 MAX.

S32GZ-50-KJH-3

32 PIN PLASTIC TSOP (I) (8×20)



NOTES

(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	19.0±0.2	0.748±0.008
I	18.4±0.2	$0.724^{+0.009}_{-0.008}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.1 MAX.	0.044 MAX.

S32GZ-50-KKH-3