REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV STATUS OF SHEETS																						
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REV STATUS OF SHEETS		**REV**															
		SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY   Thomas M. Hess

CHECKED BY   Thomas M. Hess

APPROVED BY   Monica L. Poelking

DRAWING APPROVAL DATE
94-04-18

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO   45444

MICROCIRCUIT, DIGITAL, CMOS, HISTOGRAMMMER/ACCUMULATING BUFFER MONOLITHIC SILICON

SIZE	CAGE CODE	5962-94573
A	**67268**	
SHEET	1	OF	17

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5962-E206-94

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1. SCOPE

1.1 **Scope**. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 **PIN**. The PIN shall be as shown in the following example:

```
   5962        -       94573        01          M           X           X
    |                    |           |          |           |           |
 _____          _____       _____    _____     _____      _____
Federal             RHA           Device      Device       Case        Lead
stock class      designator        type        class      outline     finish
designator       (see 1.2.1)    (see 1.2.2)  designator  (see 1.2.4) (see 1.2.5)
                                              (see 1.2.3)
_____/
                   \/
             Drawing number
```
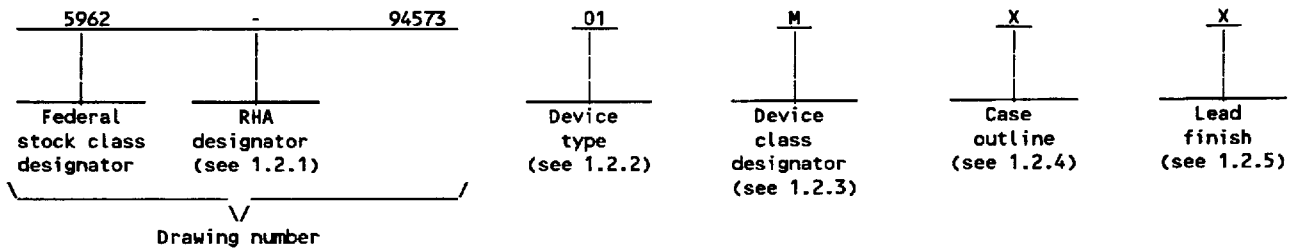
1.2.1 **RHA designator**. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 **Device type(s)**. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	48410-25	Histogrammer/accumulating buffer
02	48410-33	Histogrammer/accumulating buffer

1.2.3 **Device class designator**. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 **Case outline(s)**. The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P84	84	Pin-grid array

1.2.5 **Lead finish**. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3 <u>Absolute maximum ratings</u>. 1/

  Supply voltage . . . . .8.0 V
  Input, output, or I/O voltage applied range . . . . .GND - 0.5 V to V_{CC} + 0.5 V
  Storage temperature range (T_S) . . . .-65°C to 150°C
  Lead temperature (soldering, 10 seconds) . . . . .300°C
  Junction temperature (T_J) . . . . .175°C
  Thermal resistance:
    Junction-to-ambient (Θ_{JA}) . . . . .34.3°C/W
    Junction-to-case (Θ_{JC}) . . . . .See MIL-STD-1835
  Power dissipation at 125°C . . . . .1.46 W

1.4 <u>Recommended operating conditions</u>.

  Operating voltage range . . . . .4.5 V to 5.5 V
  Ambient operating temperature range (T_A) . . . .-55°C to 125°C

1.5 <u>Digital logic testing for device classes Q and V</u>.

  Fault coverage measurement of manufacturing
    logic tests (MIL-STD-883, test method 5012) . . . . . . XX percent 2/

2. APPLICABLE DOCUMENTS

  2.1 <u>Government specification, standards, bulletin, and handbook</u>. Unless otherwise specified, the following
specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index
of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified
herein.

  SPECIFICATION

    MILITARY

      MIL-I-38535   - Integrated Circuits, Manufacturing, General Specification for.

  STANDARDS

    MILITARY

      MIL-STD-883 - Test Methods and Procedures for Microelectronics.
      MIL-STD-973 - Configuration Management.
      MIL-STD-1835 - Microcircuit Case Outlines.

  BULLETIN

    MILITARY

      MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

  HANDBOOK

    MILITARY

      MIL-HDBK-780 - Standardized Military Drawings.

  (Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with
specific acquisition functions should be obtained from the contracting activity or as directed by the contracting
activity.)

1/ Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit
    may be impaired. Functional operability under any of these conditions is not necessarily implied.
2/ Values will be added when they become available.

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2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 <u>Case outline(s)</u>. The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.

3.2.3 <u>Block diagram</u>. The block diagram shall be as specified on figure 2.

3.2.4 <u>Timing waveforms</u>. The timing waveforms shall be as specified on figure 3.

3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 <u>Certification/compliance mark</u>. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 <u>Certificate of compliance</u>. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change for device class M</u>. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 <u>Verification and review for device class M</u>. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 <u>Microcircuit group assignment for device class M</u>. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Logical 1 input voltage	V_{IH}	V_{CC} = 5.5 V	1,2,3	All	2.2		V
Logical 0 input voltage	V_{IL}	V_{CC} = 4.5 V	1,2,3	All		0.8	V
Clock input high voltage	V_{IHC}	V_{CC} = 5.5 V	1,2,3	All	3.0		V
Clock input low voltage	V_{ILC}	V_{CC} = 4.5 V	1,2,3	All		0.8	V
Output high voltage	V_{OH}	I_{OH} = -400 mA, V_{CC} = 4.5 V 2/	1,2,3	All	2.6		V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA, V_{CC} = 4.5 V 2/	1,2,3	All		0.4	V
Input leakage current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V	1,2,3	All	-10	10	µA
Output or I/O leakage current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5 V	1,2,3	All	-10	10	µA
Standby power supply current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V Outputs open	1,2,3	All		500	µA
Operating power supply current	I_{CCOP}	f = 25.6 MHz, V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND 3/	1,2,3	All		308	mA
Clock period	t_{CP}	See figure 3	9,10,11	01 02	39 30		ns
Clock pulse width high	t_{CH}	See figure 3	9,10,11	01 02	15 12		ns
Clock pulse width low	t_{CL}	See figure 3	9,10,11	01 02	15 12		ns
Data input setup time	t_{DS}	See figure 3	9,10,11	01 02	16 15		ns

See footnotes at the end of table.

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TABLE I. _Electrical performance characteristics_ - Continued.

Test	Symbol	Conditions 1/ −55°C ≤ T_A ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Data input 0-23 hold time	t_{DH}	See figure 3	9,10,11	01 02	1 1		ns
Clock to data I/O 0-23 Valid	t_{DO}	See figure 3	9,10,11	01 02		24 19	ns
FC Pulse Width	t_{FL}	See figure 3	9,10,11	01 02	35 35		ns
FCT 0-2 setup to LD#	t_{FS}	See figure 3	9,10,11	01 02	15 12		ns
FCT 0-2 hold from LD#	t_{FH}	See figure 3	9,10,11	01 02	1 1		ns
START# setup to CLK	t_{SS}	See figure 3	9,10,11	01 02	16 15		ns
START# hold from CLK	t_{SH}	See figure 3	9,10,11	01 02	0 0		ns
PIN 0-9 setup time	t_{PS}	See figure 3	9,10,11	01 02	16 15		ns
PIN 0-9 hold time	t_{PH}	See figure 3	9,10,11	01 02	1 1		ns
LD# pulse width	t_{LL}	See figure 3	9,10,11	01 02	15 12		ns
LD# setup to START#	t_{LS}	See figure 3 4/	9,10,11	All	T_{CP}		ns
WR# low	t_{WL}	See figure 3	9,10,11	01 02	20 15		ns
WR# high	t_{WH}	See figure 3	9,10,11	01 02	20 15		ns
Address setup time	t_{AS}	See figure 3	9,10,11	01 02	20 16		ns
Address hold time	t_{AH}	See figure 3	9,10,11	01 02	2 2		ns
Data I/O setup to WR#	t_{WS}	See figure 3	9,10,11	01 02	20 16		ns
Data I/O hold from WR#	t_{WH}	See figure 3	9,10,11	01 02	2 2		ns
RD# low	tRL	See figure 3	9,10,11	01 02	55 43		ns

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RD# high	t_{RH}	See figure 3	9,10,11	01 02	20 17		ns
RD# low to Data I/O Valid	t_{RD}	See figure 3	9,10,11	01 02		55 43	ns
Output enable time	t_{OE}	See figure 3 5/	9,10,11	01 02		24 19	ns
Read/Write cycle time	t_{CY}	See figure 3	9,10,11	01 02	80 65		ns
Input capacitance	C_{IN}	V_{CC} = Open, f = 1 MHz, All measurements are referenced to device GND, See 4.4.1c T = 25°C	4	All		12	pF
Output capacitance	C_O	V_{CC} = Open, f = 1 MHz, All measurements are referenced to device GND, See 4.4.1c T = 25°C	4	All		12	pF
Functional tests		See 4.4.1b 6/	7,8	All			
Data I/O Valid after RD# high	t_{OH}	See figure 3 7/ 8/	9,10,11	All	0		ns
Output disable time	t_{OD}	See figure 3 7/ 8/	9,10,11	All		27	ns
Output rise time	t_R	See figure 3 7/ 8/ From 0.8 V to 2.0 V	9,10,11	All		9	ns
Output fall time	t_F	See figure 3 7/ 8/ From 2.0 V to 0.8 V	9,10,11	All		9	ns

1/ All testing to be performed using worst-case test conditions unless otherwise specified. A.C. testing (except subgroup 7,8 functional testing) shall be performed as follows: Input levels (clk input) 4.0 V and 0 V, Input levels (all other inputs) 0 V and 3.0 V. Timing reference levels (clk) = 2.0 V, (others) = 1.5 V. Output load per test load circuit with CL = 40 pF. Output transition is measured at V_{OH} ≥ 1.5 V and V_{OL} ≤ 1.5 V. The # indicates active low.

2/ Interchanging of force and sense conditions is permitted.

3/ Operating supply current is proportional to frequency, typical rating is 12.0 mA/MHz. Maximum junction temperature must be considered when operating part at high clock frequencies.

4/ There must be at least one rising edge of DLK between the rising edge of LD# and the falling edge of START#.

5/ Transisiton is measured at ±200 mV from steady state voltage with loading as specified in test load circuit with C_L = 40 pF.

6/ Tested as follows: f = 1MHz, V_{IH} = 2.6 V, V_{IL} = 0.4 V, V_{OH} ≥ 1.5 V, V_{OL} ≤ 1.5 V, V_{IHC} = 3.4 V and V_{ILC} = 0.4 V.

7/ Parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process design changes.

8/ Loading is specified in the test load circuit with C_L = 40 pF.

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FIGURE 1. Terminal connections.

	A	B	C	D	E	F	G	H	J	K	L
11	DIN6	DIN10	DIN11	DIN13	DIN16	DIN17	DIN19	DIN22	DIO23	DIO22	DIO19
10	DIN5	DIN7	DIN9	DIN12	DIN15	DIN21	DIN20	DIN23	DIO21	DIO20	DIO17
9	DIN4	DIN8			DIN14	GND	DIN18			DIO18	DIO16
8	DIN2	DIN3								DIO15	DIO14
7	PIN9	DIN0	GND						DIO10	DIO12	DIO11
6	VCC	DIN1	CLK			TOP VIEW			DIO9	DIO8	DIO13
5	PIN6	PIN7	PIN8						DIO6	DIO7	GND
4	PIN5	PIN4								DIO4	DIO5
3	PIN3	PIN1			FCT0	IOADD9	IOADD8			DIO1	DIO3
2	PIN2	FC=	RD=	FCT2	WR=	UWS	IOADD6	IOADD3	IOADD0	DIO0	DIO2
1	PIN0	START=	LD=	FCT1	GND	IOADD5	IOADD7	IOADD4	IOADD2	IOADD1	VCC

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FIGURE 2. Block diagram.

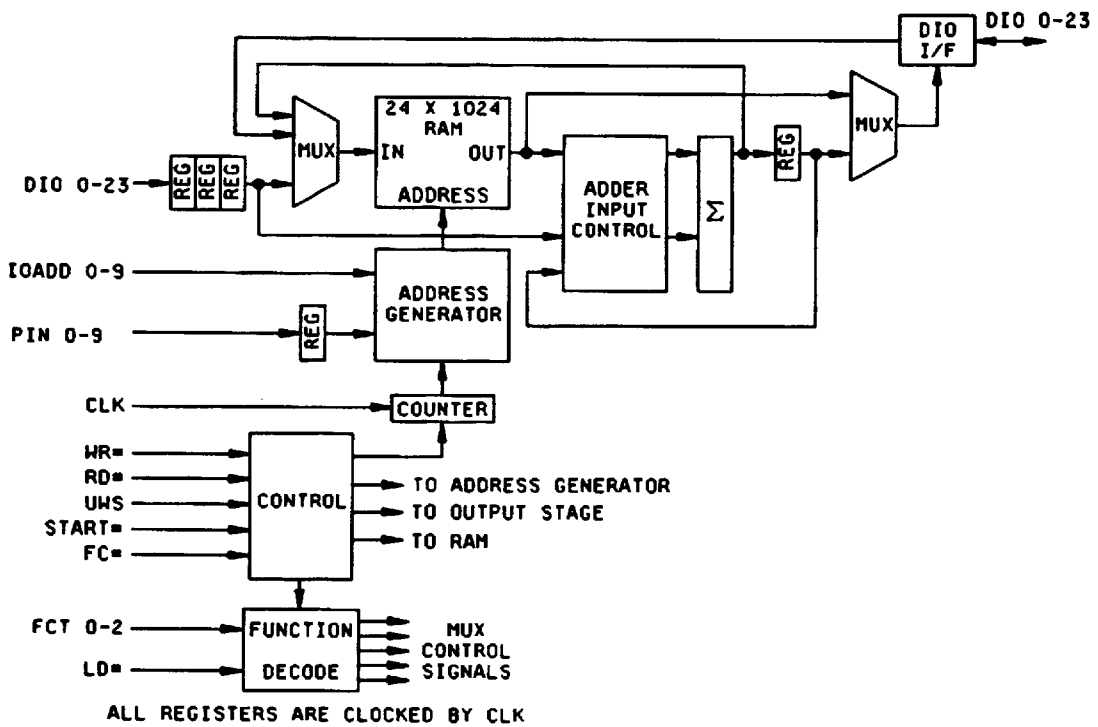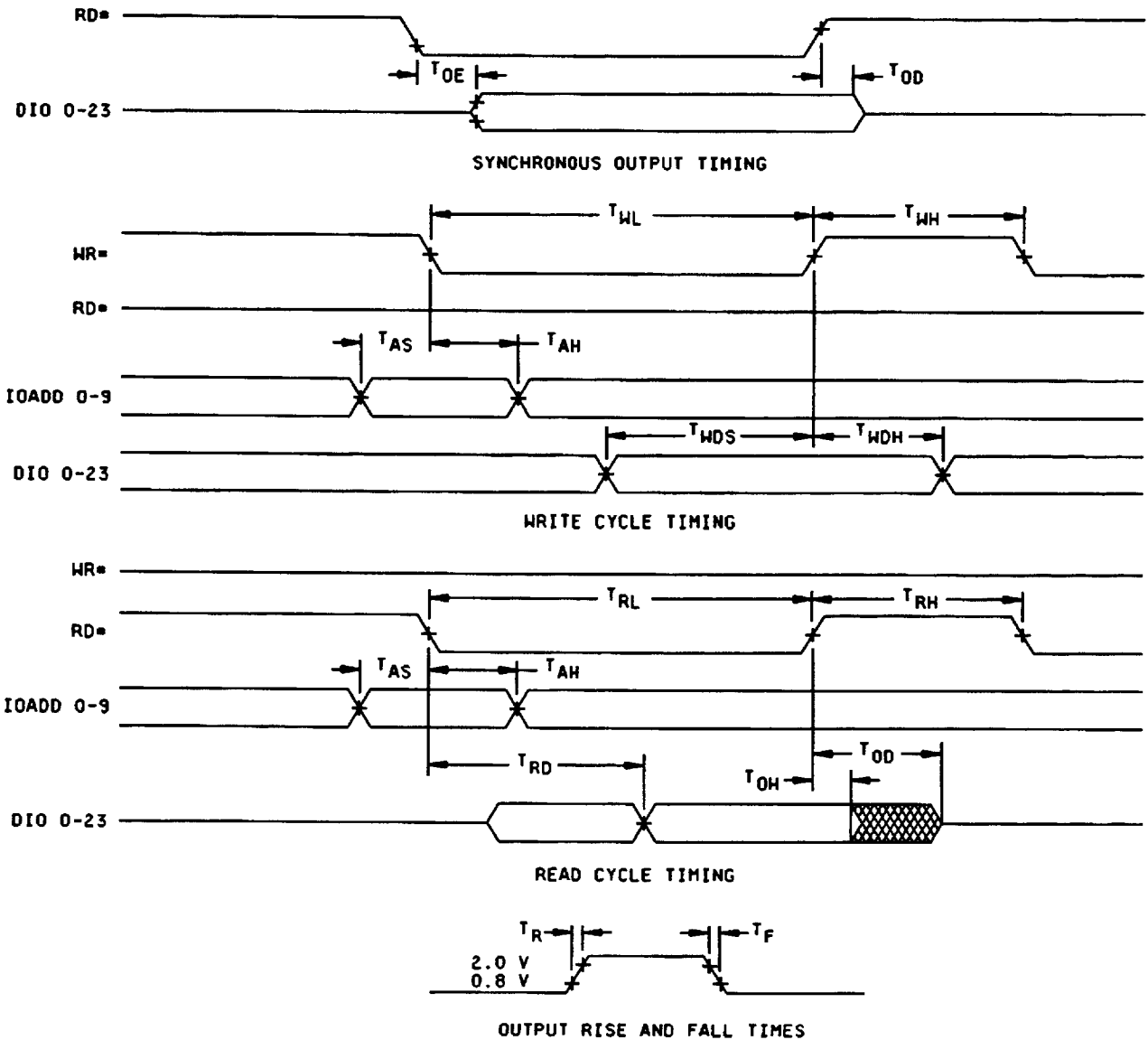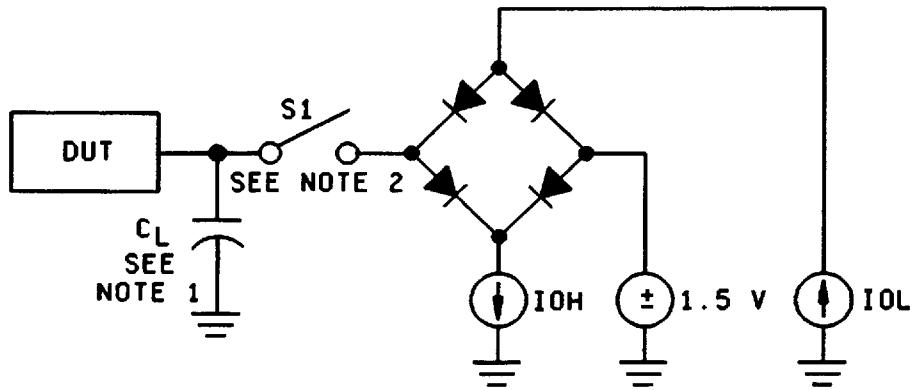| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-94573
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SYNCHRONOUS DATA AND CONTROL TIMING

FUNCTION LOAD TIMING

FIGURE 3. Timing waveforms

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SYNCHRONOUS OUTPUT TIMING

WRITE CYCLE TIMING

READ CYCLE TIMING

OUTPUT RISE AND FALL TIMES

FIGURE 3. Timing waveforms - Continued.

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Notes:
1. Includes stray and jig capacitance. C_L = 40 pF.
2. Switch S1 open for I_{CCSB} and I_{CCOP} test.

FIGURE 3. Timing waveforms - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 <u>Screening</u>. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 <u>Additional criteria for device class M</u>.

    a. Burn-in test, method 1015 of MIL-STD-883.

       (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

       (2) T_A = +125°C, minimum.

    b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 <u>Additional criteria for device classes Q and V</u>.

    a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

    b. Interim and final electrical test parameters shall be as specified in table II herein.

    c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 <u>Conformance inspection</u>. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 <u>Group A inspection</u>.

    a. Tests shall be as specified in table II herein.

    b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

    c. Subgroup 4 (C_{IN} and C_O measurement) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Test all applicable pins on five devices with zero failures.

4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.2.1 <u>Additional criteria for device class M</u>. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. <u>Electrical test requirements</u>.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 1/ 10, 11	1, 2, 3, 7, 1/ 8, 10, 11	1, 2, 3, 7 2/ 8, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)			

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

   a. End-point electrical parameters shall be as specified in table II herein.

   b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

   c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 <u>Substitutability</u>. Device class Q devices will replace device class M devices.

6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 <u>Comments</u>. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

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6.5 <u>Abbreviations, symbols, and definitions.</u> The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows.

SYMBOL	DESCRIPTION
CLK	Clock input. This input has no effect on the chips functionality when the chip is programmed to an asynchronous mode. All signals denoted as synchronous have their timing specified with reference to this signal
PIN 0-9	Pixel input. This input bus is sampled by the rising edge of clock. It provides the on chip RAM with address values in histogram, bin accumulate and LUT (write) mode. During asynchronous modes it is unused.
LD#	The load pin is used to load the FCT0-2 bits into the FCT registers.
FCT 0-2	These three pins are decodes to determine the mode of operation for the chip. The signals are sampled by the rising edge of LD# and take effect after the rising edge of LD#. Since the loading of this function is asynchronous to CLK, it is necessary to disable the START# pin during loading and enable START# at least 1 CLK cycle following the LD# pulse.
START#	This pin informs the on chip circuitry which clock cycle will start and/or stop the current mode of operation. Thus, the modes are asynchronously selected (via LD#) but are synchronously started and stopped. This input is sampled by the rising edge of CLK. The actual function of this input depends on the mode that is selected. START# must always be held high (disabled) when changing modes. This will provide a smooth transition from one mode to the next by allowing the part to reconfigure itself before new mode begins. When START# is high, LUT (read) mode is enabled except for Delay and Delay and Subtract modes.
FC#	Flash clear. This input provides a fully asynchronous signal which effectively resets all bits in the RAM array and the input and output data paths to zero.
DIN0-23	Data input bus. Provides data to the histogrammer during Bin Accumulate, LUT, Delay and Delay and Subtract modes. Synchronous to CLK.
DIO0-23	Asynchronous data bus. Provides RAM access for a microprocessor in preconditioning the memory array and reading the results of the previous operation. Configurable as either a 24 bit or 16 bit bus.
IOADD0-9	RAM address in asynchronous modes. Sampled on the falling edge of WR# or RD#.
UWS	Upper Word Select. IN 16 bit asynchronous mode, a one on this pin denotes the contents of DIO0-7 as being the upper eight bits of the data in or out of the Histogrammer. A zero means that DIO0-15 are the lower 16 bits. In all other modes this pin has no effect.
WR#	Write enable to the RAM for the data on DIO0-23 when the device is configured in one of the asynchronous modes. Asynchronous to CLK.
RD#	Read control for the data on DIO0-23 in asynchronous modes. Output enable for DIO0-23 in other modes. Asynchronous to CLK.
VCC	+5 V
GND	Ground

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6.6 <u>One part - one part number system</u>. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 <u>Sources of supply</u>.

6.7.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 <u>Approved sources of supply for device class M</u>. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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