OC-48/STM-16 Framer with VC-POSIC2GVC

Features

- OC-48/STS-48/STM-16, OC-12/STS-12/STM-4, OC-3/STS3/STM-1 rates, concatenated and non-concatenated
- Complies with ITU-Standards G.707/Y.1322 and G.783 $^{\![1,2]}$
- Complies with Bellcore GR253 rev.1, 1997^[3]
- Channelized operation: supports 16xOC-3 and 4xOC-12 within OC-48 stream
- Supports TUG3 mapping in SDH mode
- Virtual concatenation enables secure and dedicated bandwidth provisioning^[4]
- Up to 16 channels
- From 50-Mbps to 1.2-Gbps bandwidth per channel
- STS-1 and STS-3c granularity
- Full duplex mapping of ATM cells over SONET/SDH
- Complies with ITU-Standards I 432.2^[5,6,7]
- Full duplex mapping of packet-over-SONET/SDH: IETF RFC 1619/1662/2615 (HDLC/PPP)^[8,9,10]
- · Generic Protocol Encapsulator/Decapsulator delineates packets/frames with length-CRC frame construct
- Generic Framing Procedure (GFP) per ANSI T1X1.5^[11,12,13]
- GFP 268r1
- Simple Data Link (SDL)—IETF RFC2823^[14]
- Cypress Hybrid Data Transport (HDT)^[15]
- User-programmable encapsulation
- User-programmable clear channel transport
- User-programmable SONET/SDH bypass
- · Programmable frame tagging engine for packet preclassification enables such features as
- MPLS label lookup and tagging

- PPP: LCP and NCP tagging
- · PPP control packets optionally sent to host CPU interface
- · MAC/layer 3 address look up and tagging.
- Programmable A1A2 processing bypass in Rx direction with frame sync input
- Complete section overhead (SOH), line overhead (LOH), and path overhead (POH) processing
- APS extraction, CPU interrupt generation, and programmable insertion of APS byte
- Line side APS port interface
- Provision for protection switching on SONET/SDH port
- Programmable PRBS generator and receiver
- · Serial port to access line/section data communication channel (DCC) and voice communication channel (VCC)
- Full duplex UTOPIA/OIF-SPI (POS-PHY) level 3 interface^[16,17]
- 16-bit/32-bit host CPU interface bus
- JTAG and boundary scan
- Glue-less interface with Cypress CYS25G0101DX **OC-48 PHY**
- 0.18-um CMOS, 504-pin BGA package
- +1.8V for core, +3.3V for LVTTL I/O, +1.5V/+3.3V for HSTL/LVPECL I/O supply, and +0.75V/2.0V reference

Applications

- · Multi-service nodes
- · ATM switches and routers
- Packet routers and multiservice routers
- SONET/SDH/add-drop mux for packet/data applications
- · SONET/SDH/ATM/POS test equipment

Notes:

- TIU-T Recommendation G.707. "Network Node Interface for the Synchronous Digital Hierarchy." 1996.

 ITU-T Recommendation G.783. "Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks." 2000.

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 ITU-T Recommendation I.432.3. "B-ISDN User-Network Interface—Physical Layer Specification: 1544 kbit/s and 2048 kbit/s Operation." 1999.

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