POSIC2GVC™/POSIC2G™ Evaluation Board

Purpose

This board is intended for two purposes. The first is as a demonstration of the capabilities of the (Packet-Over-SONET Integrated Circuit) POSIC2GVC™ device. The second is as a development platform for the system designer who wants to evaluate the POSIC2GVC device, to create custom logic to interface with POSIC2GVC, and to implement their own functionality.

Features

The features of this board include:

- Cypress POSIC2GVC device
- Cypress high-performance No Bus Latency™ (NoBL™) RAM, 12 MBytes
- Cypress CYS25G0101DX OC-48 SONET/SDH PHY
- Cypress Delta39K™ CPLD CY39100V388-200MGC
- Motorola MPC860 processor, operating at 66 MHz
- Two 300K gate FPGAs, each scalable to 600K gates
- OCP optical modules, 1310-nm wavelength
- Four independent clock sources on the board
- 16 MBytes of SDRAM
- 1 MByte of FLASH memory
- Codec and handset for communication over orderwire bytes.

Standard MICTOR connectors are used on all buses for external driving and observing signals.This permits the user to directly control all aspects of the board's operation.

The evaluation board is powered by an external 3.3V power supply. The board also has a 5V power supply connector, to supply 5V to the 266-pin MICTOR connector on the board.

External Interfaces

The following signals are brought out through connectors:

- RS 232 debug port
- UTOPIA/SPI-3 Level 3 signals
- TOH serial data interface
- Processor data, address and control signals
- JTAG signals
- BDM signals
- POSIC2GVC-SONET transmit and receive parallel data bus
- NoBL SRAM interface signals
- Telephone Handset 4-wire interface
- POSIC2GVC Debug Port interface.

The evaluation board is a free-standing, 12-layer PCB with mounting holes for support.

See *Figure 5* for an example using the MICTOR connectors to replace the Motorola CPU with another device.

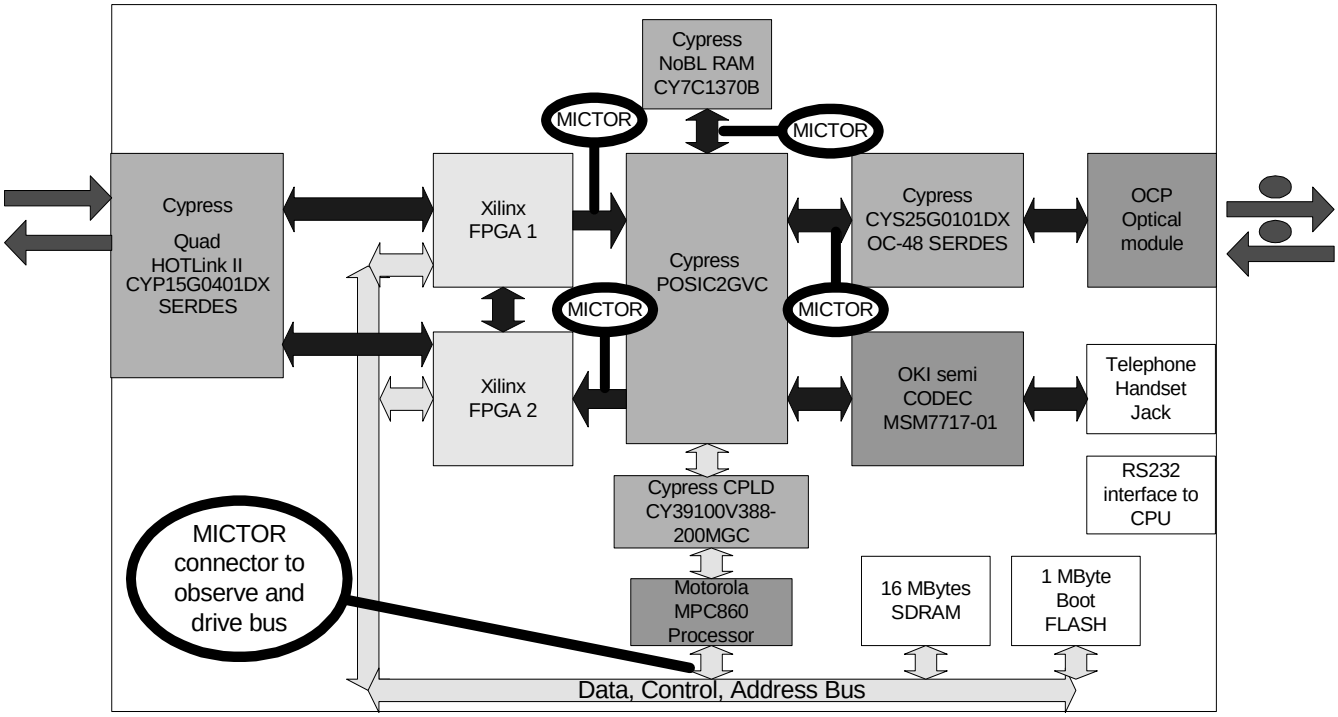

Figure 1. POSIC2GVC Evaluation Board Block Diagram