

T-52-13-05


HV04
HV06

64-Channel Serial To Parallel Converter With High Voltage CMOS Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options					
		84-Pad Ceramic Leadless Chip Carrier	84-J Lead Plastic Chip Carrier	80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die
HV04	60V	HV0406LC	HV0406PJ	HV0406DG	HV0406PG	HV0406T	HV0406X
	80V	HV0408LC	HV0408PJ	HV0408DG	HV0408PG	HV0408T	HV0408X
HV06	60V	HV0606LC	HV0606PJ	HV0606DG	HV0606PG	HV0606T	HV0606X
	80V	HV0608LC	HV0608PJ	HV0608DG	HV0608PG	HV0608T	HV0608X

Features

- ☐ HVCMOS® Technology
- ☐ Output voltages up to 90V using a ramped supply
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20 mA
- ☐ Shift register speed 8 MHz
- ☐ Latched data outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings¹

Supply voltage, V_{DD}	-0.5V to +15V
Supply voltage, V_{PP} ²	-0.5V to +90V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current ³	3.0A
High voltage supply current ³	2.6A
Continuous total power dissipation ⁴	1900mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS} .

2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.

3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.

4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV04 and HV06 are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the low to high transition of the clock. The HV04 shifts in the counterclockwise direction when viewed from the top of the package and the HV06 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout64). Operation of the shift register is not affected by the LE (latch enable), BL (blanking), or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored when LE is low.

The HV04 and HV06 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or limit the current through each output.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

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Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current			25	mA	$f_{CLK} = 8\text{MHz}$, $f_{DATA} = 4\text{MHz}$ $\overline{LE} = \text{LOW}$
I_{DDQ}	Quiescent V_{DD} Supply Current			0.25	mA	All $V_{IN} = 0\text{V}$
I_{PP}	High Voltage Supply Current			0.50	mA	$V_{PP} = 80\text{V}$ All outputs high
				0.50	mA	$V_{PP} = 80\text{V}$ All outputs low
I_{IH}	High-Level Logic Input Current			10	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current	-10			μA	$V_I = 0\text{V}$
V_{OH}	High-Level Output	HV_{OUT}	74		V	$V_{PP} = 80\text{V}$, $I_{HV_{OUT}} = -20\text{mA}$
		Data Out	$V_{DD} - 1\text{V}$		V	$I_{D_{OUT}} = -100\mu\text{A}$
V_{OL}	Low-Level Output	HV_{OUT}		6	V	$V_{PP} = 80\text{V}$, $I_{HV_{OUT}} = +20\text{mA}$
		Data Out		1	V	$I_{D_{OUT}} = +100\mu\text{A}$
V_{OC}	HV_{OUT} Clamp Voltage			$V_{PP} + 1.5$	V	$I_{OL} = +20\text{mA}$
				-1.5	V	$I_{OL} = -20\text{mA}$

AC Characteristics

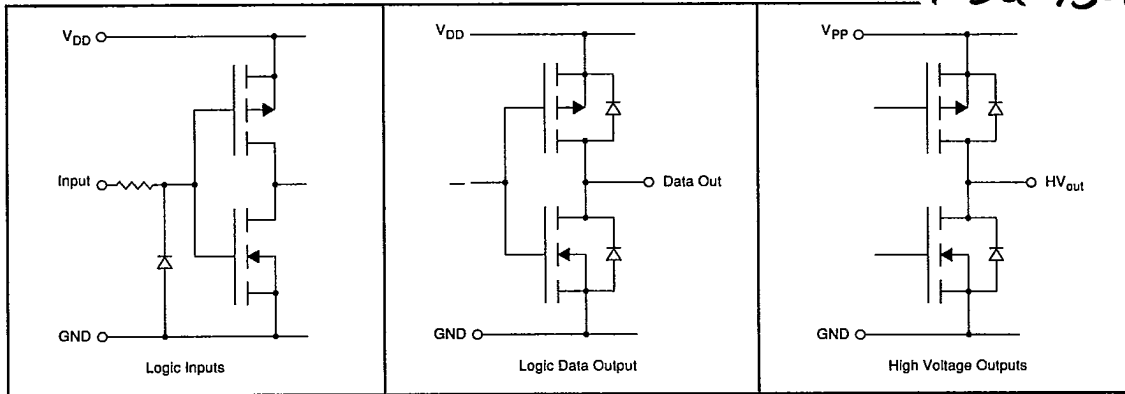
Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Rises	25			ns	
t_H	Data Hold Time After Clock Rises	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	$\overline{LE}$ Delay Time Rising Edge of Clock	25			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock	30			ns	
t_D	Delay Time from V_{PP} Low Until Change in $\overline{LE}$, $\overline{POL}$, $\overline{BL}$ Is Allowed	100			ns	
t_{SL}	Setup Time from $\overline{LE}$ Rise to V_{PP} Rise	200			ns	
t_{SB}	Setup Time from $\overline{BL}$ Selected to V_{PP} Rise	150			ns	
t_{SP}	Setup Time from $\overline{POL}$ Selected to V_{PP} Rise	100			ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLH}	Delay Time Clock to Data Low to High			100	ns	

Recommended Operating Conditions

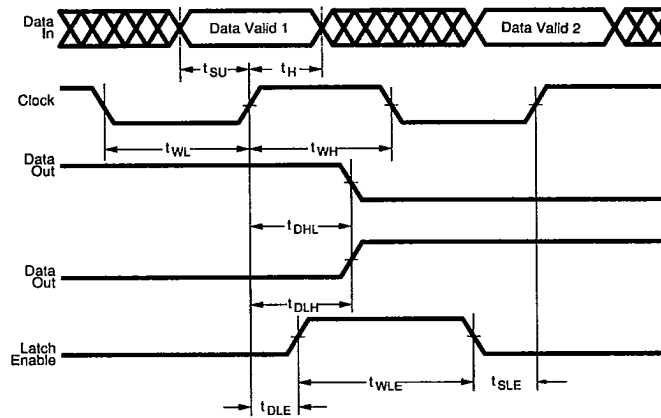
Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	10.8	12	13.2	V
V_{PP}	High voltage supply	-0.3		80	V
V_{IH}	High-level input voltage	$V_{DD} - 2\text{V}$		V_{DD}	V
V_{IL}	Low-level input voltage	0		2.0	V
dV/dt	V_{PP} ramp rate			80	V/ μs
T_A	Operating free-air temperature	-40		+85	$^{\circ}\text{C}$

Input and Output Equivalent Circuits

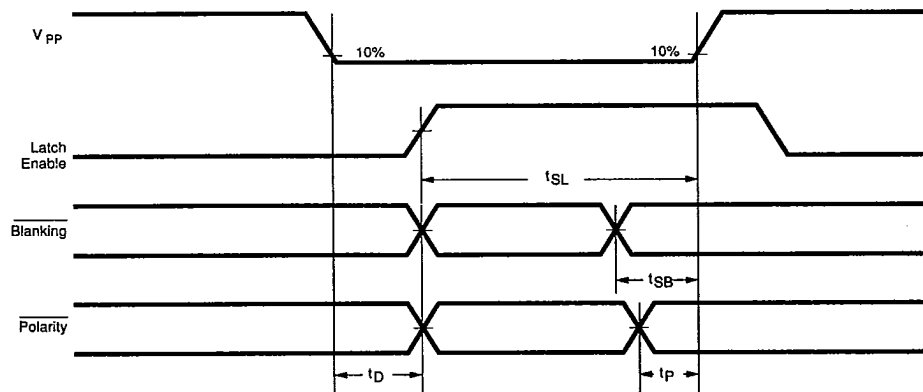
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Switching Waveforms

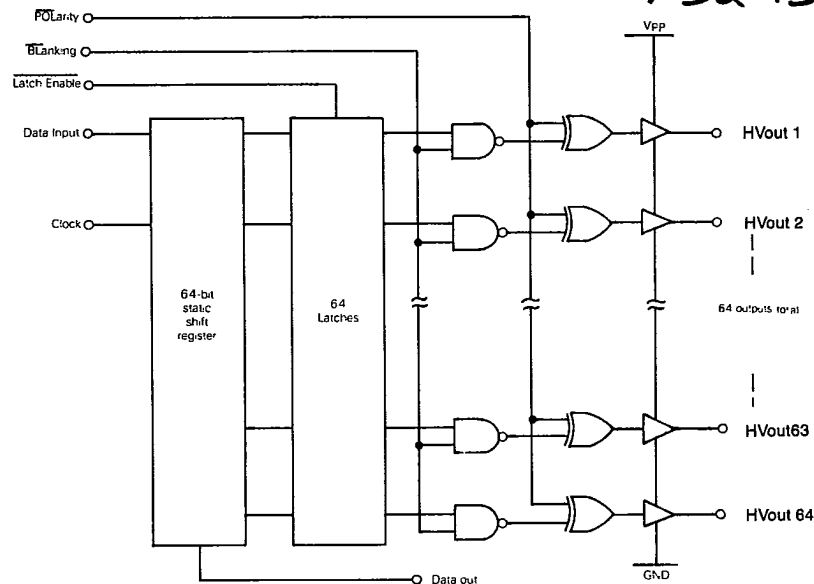


Output Control Waveforms



Functional Block Diagram

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Function Table

Function	Inputs					Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1 2...64	HV Outputs 1' 2...64	Data Out *
All on	X	X	X	L	L	* *	H H...H	*
All off	X	X	X	L	H	* *	L L...L	*
Invert mode	X	X	L	H	L	* *	* *	*
Load S/R	H or L	↑	L	H	H	H or L *	* *	*
Load Latches	X	H or L	↑	H	H	* *	* *	*
	X	H or L	↑	H	L	* *	* *	*
Transparent Latch mode	L	↑	H	H	H	L *	L *	*
	H	↑	H	H	H	H *	H *	*

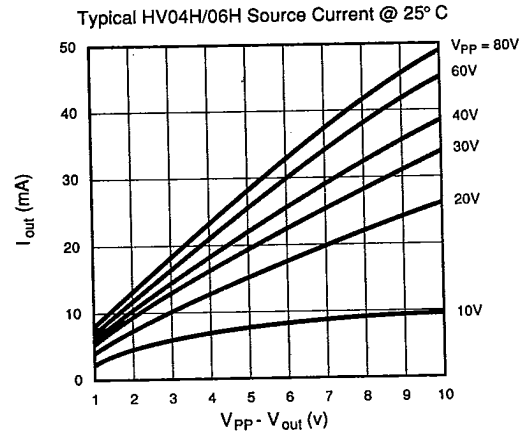
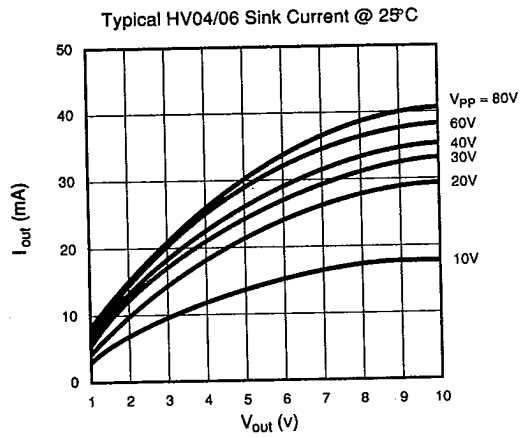
Notes:

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.

* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

Typical Performance Curves

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Pin Configurations

PJ and LC Packages

HV04

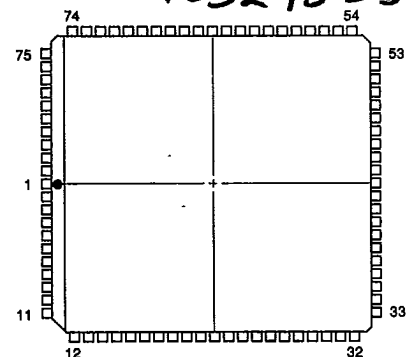
Pin	Function	Pin	Function
1	V _{DD}	43	HVout 33
2	LE	44	HVout 34
3	Data in	45	HVout 35
4	BL	46	HVout 36
5	HVout 1	47	HVout 37
6	HVout 2	48	HVout 38
7	HVout 3	49	HVout 39
8	HVout 4	50	HVout 40
9	HVout 5	51	HVout 41
10	HVout 6	52	HVout 42
11	N/C	53	N/C
12	V _{PP}	54	V _{PP}
13	GND	55	GND
14	HVout 7	56	HVout 43
15	HVout 8	57	HVout 44
16	HVout 9	58	HVout 45
17	HVout 10	59	HVout 46
18	HVout 11	60	HVout 47
19	HVout 12	61	HVout 48
20	HVout 13	62	HVout 49
21	HVout 14	63	HVout 50
22	HVout 15	64	HVout 51
23	HVout 16	65	HVout 52
24	HVout 17	66	HVout 53
25	HVout 18	67	HVout 54
26	HVout 19	68	HVout 55
27	HVout 20	69	HVout 56
28	HVout 21	70	HVout 57
29	HVout 22	71	HVout 58
30	GND	72	GND
31	V _{PP}	73	V _{PP}
32	N/C	74	N/C
33	HVout 23	75	HVout 59
34	HVout 24	76	HVout 60
35	HVout 25	77	HVout 61
36	HVout 26	78	HVout 62
37	HVout 27	79	HVout 63
38	HVout 28	80	HVout 64
39	HVout 29	81	POL
40	HVout 30	82	Data Out
41	HVout 31	83	CLK
42	HVout 32	84	GND

HV06

Pin	Function	Pin	Function
1	V _{DD}	43	HVout 32
2	LE	44	HVout 31
3	Data in	45	HVout 30
4	BL	46	HVout 29
5	HVout 64	47	HVout 28
6	HVout 63	48	HVout 27
7	HVout 62	49	HVout 26
8	HVout 61	50	HVout 25
9	HVout 60	51	HVout 24
10	HVout 59	52	HVout 23
11	N/C	53	N/C
12	V _{PP}	54	V _{PP}
13	GND	55	GND
14	HVout 58	56	HVout 22
15	HVout 57	57	HVout 21
16	HVout 56	58	HVout 20
17	HVout 55	59	HVout 19
18	HVout 54	60	HVout 18
19	HVout 53	61	HVout 17
20	HVout 52	62	HVout 16
21	HVout 51	63	HVout 15
22	HVout 50	64	HVout 14
23	HVout 49	65	HVout 13
24	HVout 48	66	HVout 12
25	HVout 47	67	HVout 11
26	HVout 46	68	HVout 10
27	HVout 45	69	HVout 9
28	HVout 44	70	HVout 8
29	HVout 43	71	HVout 7
30	GND	72	GND
31	V _{PP}	73	V _{PP}
32	N/C	74	N/C
33	HVout 42	75	HVout 6
34	HVout 41	76	HVout 5
35	HVout 40	77	HVout 4
36	HVout 39	78	HVout 3
37	HVout 38	79	HVout 2
38	HVout 37	80	HVout 1
39	HVout 36	81	POL
40	HVout 35	82	Data Out
41	HVout 34	83	CLK
42	HVout 33	84	GND

Package Outline

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top view

84-pin J-lead Package

Pin Configurations

PG and DG Packages

HV04

Pin	Function	Pin	Function
1	GND	41	GND
2	V _{PP}	42	V _{PP}
3	HVout 59	43	HVout 23
4	HVout 60	44	HVout 24
5	HVout 61	45	HVout 25
6	HVout 62	46	HVout 26
7	HVout 63	47	HVout 27
8	HVout 64	48	HVout 28
9	POL	49	HVout 29
10	Data Out	50	HVout 30
11	CLK	51	HVout 31
12	GND	52	HVout 32
13	V _{DD}	53	HVout 33
14	LE	54	HVout 34
15	Data In	55	HVout 35
16	BL	56	HVout 36
17	HVout 1	57	HVout 37
18	HVout 2	58	HVout 38
19	HVout 3	59	HVout 39
20	HVout 4	60	HVout 40
21	HVout 5	61	HVout 41
22	HVout 6	62	HVout 42
23	V _{PP}	63	V _{PP}
24	GND	64	GND
25	HVout 7	65	HVout 43
26	HVout 8	66	HVout 44
27	HVout 9	67	HVout 45
28	HVout 10	68	HVout 46
29	HVout 11	69	HVout 47
30	HVout 12	70	HVout 48
31	HVout 13	71	HVout 49
32	HVout 14	72	HVout 50
33	HVout 15	73	HVout 51
34	HVout 16	74	HVout 52
35	HVout 17	75	HVout 53
36	HVout 18	76	HVout 54
37	HVout 19	77	HVout 55
38	HVout 20	78	HVout 56
39	HVout 21	79	HVout 57
40	HVout 22	80	HVout 58

HV06

Pin	Function	Pin	Function
1	GND	41	GND
2	V _{PP}	42	V _{PP}
3	HVout 6	43	HVout 42
4	HVout 5	44	HVout 41
5	HVout 4	45	HVout 40
6	HVout 3	46	HVout 39
7	HVout 2	47	HVout 38
8	HVout 1	48	HVout 37
9	POL	49	HVout 36
10	Data Out	50	HVout 35
11	CLK	51	HVout 34
12	GND	52	HVout 33
13	V _{DD}	53	HVout 32
14	LE	54	HVout 31
15	Data In	55	HVout 30
16	BL	56	HVout 29
17	HVout 64	57	HVout 28
18	HVout 63	58	HVout 27
19	HVout 62	59	HVout 26
20	HVout 61	60	HVout 25
21	HVout 60	61	HVout 24
22	HVout 59	62	HVout 23
23	V _{PP}	63	V _{PP}
24	GND	64	GND
25	HVout 58	65	HVout 22
26	HVout 57	66	HVout 21
27	HVout 56	67	HVout 20
28	HVout 55	68	HVout 19
29	HVout 54	69	HVout 18
30	HVout 53	70	HVout 17
31	HVout 52	71	HVout 16
32	HVout 51	72	HVout 15
33	HVout 50	73	HVout 14
34	HVout 49	74	HVout 13
35	HVout 48	75	HVout 12
36	HVout 47	76	HVout 11
37	HVout 46	77	HVout 10
38	HVout 45	78	HVout 9
39	HVout 44	79	HVout 8
40	HVout 43	80	HVout 7

