MPEG-2 Digital Audio/Video Decoder

Affordable high-quality playback

Highlights

This digital audio/video decoder is designed with enhanced features to meet rapidly emerging demand of broadcast, small office/home office (SOHO), desktop publishing, video post-processing, and professional editing user applications.

MPEGCS22

This audio/video (A/V) decoder is part of a family of MPEG-2 products from IBM Microelectronics. This (A/V) integrated single chip decodes MPEG-2 standard MP@ML video and MPEG-2 stereo Layer I & II (CD quality) audio. This decoder can sustain, at minimum, MPEG-2 (IPB frames) data rates up to 15Mbp/s (MP@ML).

Designed for Emerging A/V Applications

The decoder's extended features provide access to user data in the video stream. The design allows for recognition of sequence error codes embedded in the video stream. Horizontal and vertical filters deliver high quality video for data formats that require picture size expansion. The chip has a built in phase-locked-loop to keep the audio and video synchronized. A flexible host interface is supported with four modes of operation to provide for high-bandwidth or cost-sensitive applications. Memory bus flexibility is provided to support 2 MB or 4 MB applications.

Teletext and Vertical Blanking Interval Data Output

The MPEGCS22 decoder chip supports data transmission on the pixel bus and teletext data output on the TTX Data pin during the Vertical Blanking Interval (VBI). The application controls the number of lines of VBI data to be output. For VBI data outputs, all the VBI lines can be used to deliver data. A double buffer is provided so the host can write VBI or teletext data to one buffer while the data in the other buffer is being displayed.

MPEGCS22 Features:

- *Standard Main Profile at Main Level (MP@ML) decoder for 4:2:0 chroma applications, along with MPEG audio decoding*
- *Video Decoder - MPEG-2, ISO/IEC 13818-2 MP@ML*
- *Audio Decoder - MPEG-2, ISO/IEC 13818-3 Layers I & II*
- *Supports European DVB standard*
- *Supports on-chip Packetized Elementary Stream (PES) layer decoding for both audio and video to extract the Presentation Time Stamp (PTS)*
- *User data automatically stored in SDRAM accessible to host*
- *Letterbox mode supported for 16:9 Aspect Ratio*
- *Horizontal and vertical filters deliver high quality video. Pan and scan are supported in 1/16 pel accuracy*
- *Up to 11 bits DC precision for enhanced picture quality*
- *Sophisticated error concealment on all video layers*
- *Picture-in-picture support*
- *Supports Teletext or Vertical Blanking Interval data output*

Flexible Interface to Industry-Standard SDRAM:

- *2 MB SDRAM 16-bit interface for MPEG-2 NTSC/PAL up to 15 Mbp/s*
- *4 MB SDRAM addressing capability for extended application*

Audio Features:

- *Supports MPEG-2 Layer I & II stereo*
- *Capable of playing PCM audio data*
- *Sampling rates of 16, 22.05, 24, 32, 44.1 and 48 KHz supported*
- *Generation of 128 different tones for up to 31 different durations*
- *Audio attenuation in 63 increments per channel*
- *Built-in phase-locked-loop to provide the audio clocks for audio and video synchronization*
- *Common 16-bit serial audio output interfaces to support most DAC interfaces*
- *De-emphasis indication*
- *Single clock (27 MHz) input*
- *Error concealment support*

Enhanced On-Screen Display (OSD):

- *Link list operation with multiregions and block copy capability*
- *Animation assist*
- *Programmable OSD size*
- *OSD-controlled video shading or blending*
- *Programmable bitmap resolution up to 8 bits per color mapped pixel*
- *16-bit direct color mode*

Input Interface Flexibility:

- *8-bit or 16-bit audio/video compression data and host data interface*
- *8-bits with acknowledge for easy connection to transport chips*
- *Serial audio compressed data for transport chip connection*
- *Serial video compressed data input with simultaneous host data interface*

Output Interface Flexibility (Programmable Controls):

- *Composite blanking and Field ID signals*
- *V-sync and H-sync signals*
- *V-ref and H-ref signals*
- *Programmable signal polarity*

Specifications

Technology	0.4 micron CMOS process, 4 levels of metal
Ambient temperature range	0-70°C
Nominal supply voltage	3.3 Volts ±5%
Nominal power dissipation	1.4 watts
Packaging	28 mm plastic quad flat pack (160 pins)

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY
12533-6531

The IBM home page can be found at:
http://www.ibm.com

The IBM Microelectronics Division home page can be found at:
http://www.chips.ibm.com

07G520329

G522-0329-00