OTI-043 Single Chip Flat Panel VGA Controller

Features

■ Highly integrated, single chip design	*Saves space and minimizes implementation cost*
■ Fully Hardware IBM VGA compatible	*Supports all IBM VGA modes*
■ Supports CRT monitors and flat panel displays simultaneously	*Allows system to function as a desktop as well as a laptop*
■ 800 x 600 resolution with 64 shades of gray for flat panels and 256 colors for CRTs	*High resolution display*
■ Supports 256K x 4 and 64K x 16 DRAMs	*Increases design flexibility and increases performance*
■ Operating system independent power management scheme	*Power management function can be used with all operating systems (DOS, OS/2, UNIX)*
■ Internal data cache	*Increases performance*
■ Maximum pixel clock frequency up to 50 MHz	*Increases display quality*
■ Intelligent color summing and contrast adjusting logic	*Improves display quality*
■ Automatic video compensation logic adapts to different panel resolutions	*Increases usable display area*
■ Integrated palette and separate LCD video timing circuit	*Speeds switching between LCD and VGA modes and reduces software overhead*
■ Local bus option with OTI-040 Core Logic Subsystem	*Increases performance*
■ 160-pin PQFP	*Easy to handle, saves space*

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General Description

The OTI-043 is a highly integrated flat panel controller which provides a cost-effective, high performance graphics solution for notebook/laptop PCs. It supports a variety of flat panels including gas plasma, electro-luminescent (EL), and liquid crystal (LCD) displays. By integrating the key system elements on a single chip, this controller simplifies the design and reduces the implementation cost of a VGA graphics subsystem.

LCD panel displays are supported in up to 800 x 600 mode with 64 gray levels. Output signals for an external CRT support up to VESA-compatible 800 x 600 resolution with 256 colors. A flexible DRAM configuration supports both 256K x 4 and 64K x 16 DRAMs. This allows the system designer to optimize board layout to specific requirements. Utilizing 64K x 16 DRAMs can double system video performance.

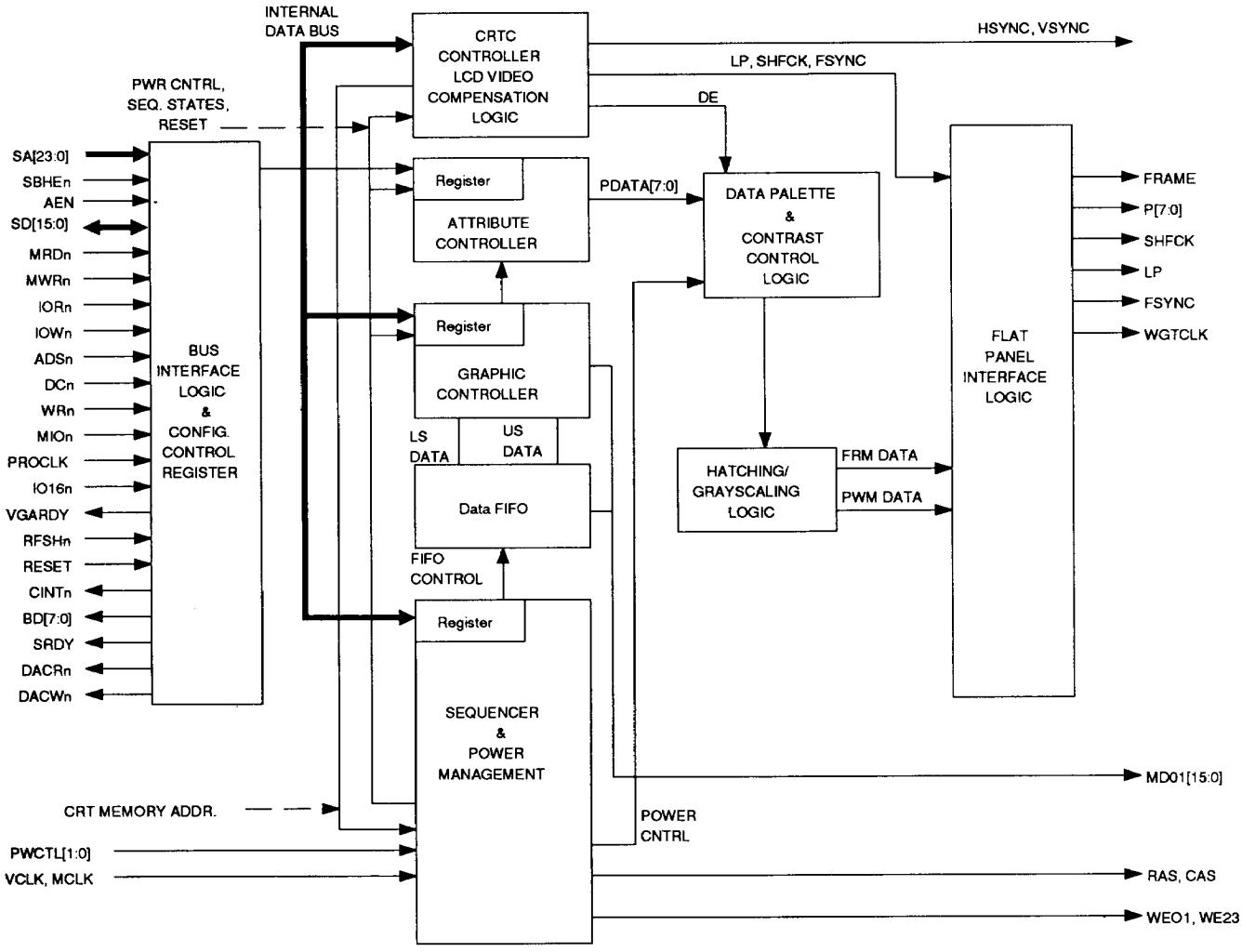
Because power management is critical in notebook and laptop PCs, the OTI-043 can be directly accessed by hardware to optimize system power management control. Specific sections of the controller can be disabled through various power management modes to extend battery life. Produced using 1.0µ CMOS process technology, the chip itself consumes very little power.

The OTI-043 provides full hardware support for context switching. All of the internal registers can be accessed for both reading and writing. There are also separate registers for flat panel control, providing fast switching between LCD and CRT displays.

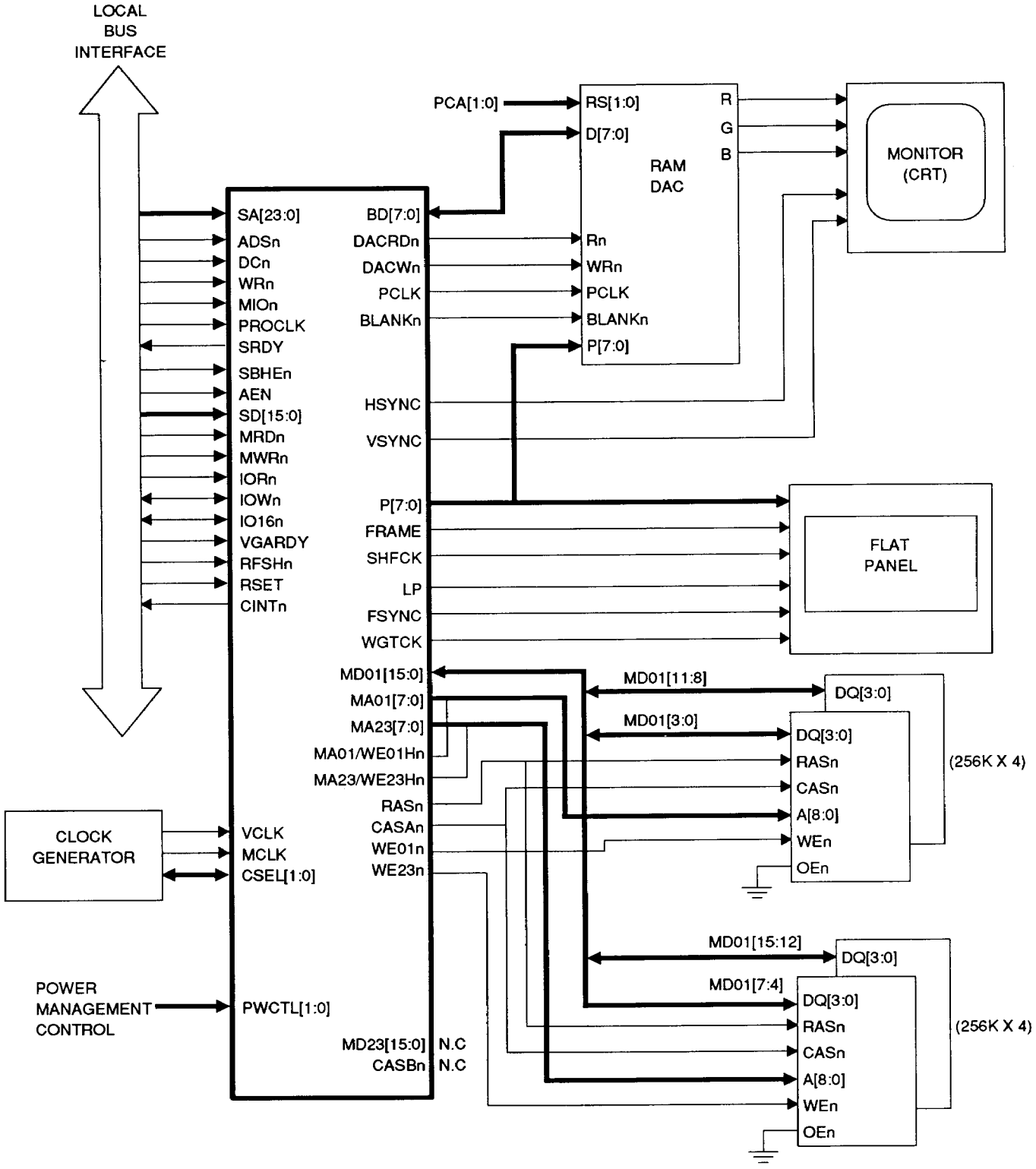
An automatic video compensation feature enables the OTI-043 to be used for different VGA display resolutions on a fixed size panel. Internal data caching speeds CPU access time for faster screen refreshes.

A proprietary local bus scheme enables the OTI-043 to reside on the CPU bus instead of the conventional PC bus. This tightly-coupled video system increases video performance by more than 70%.

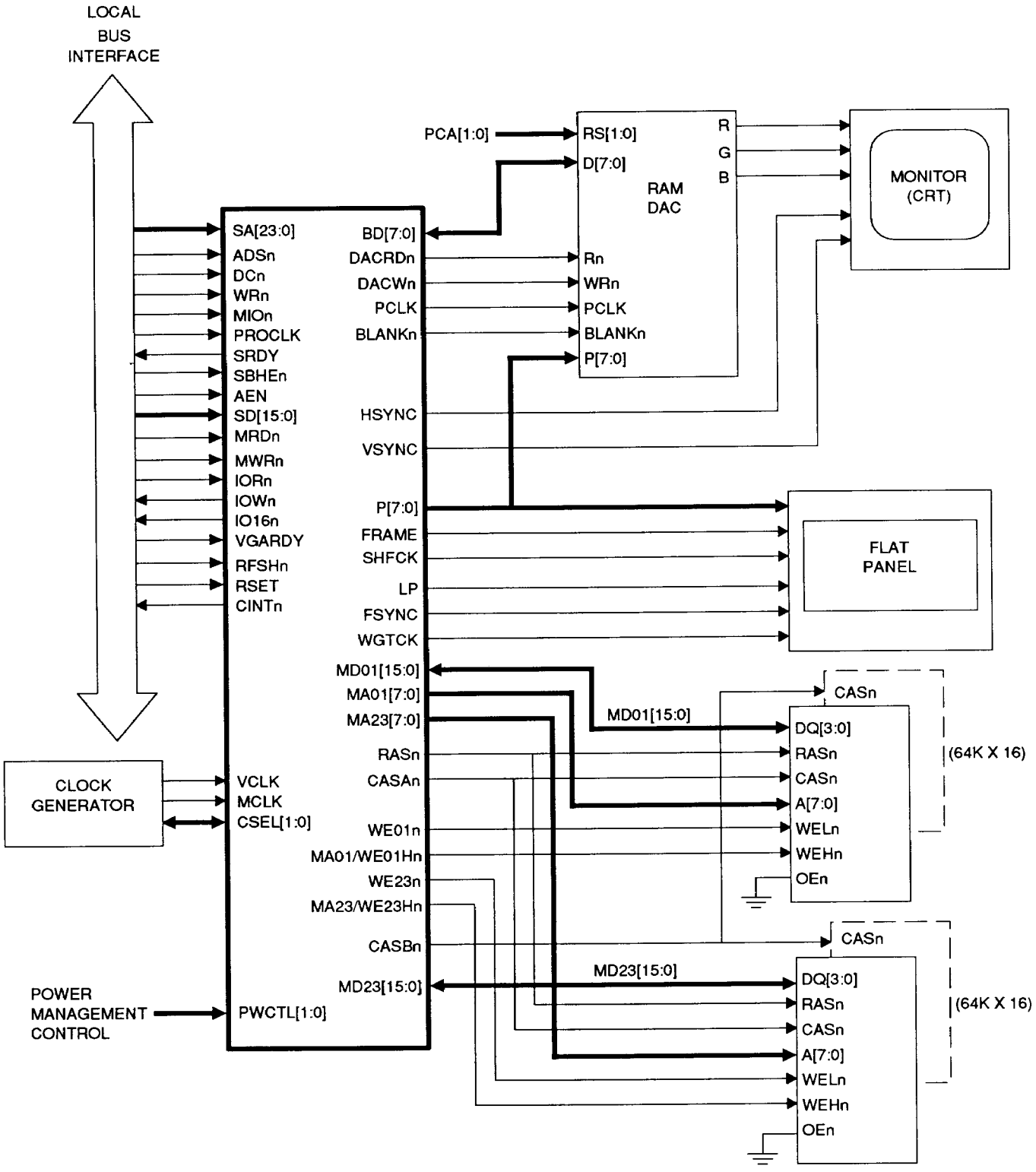
Chip Block Diagram



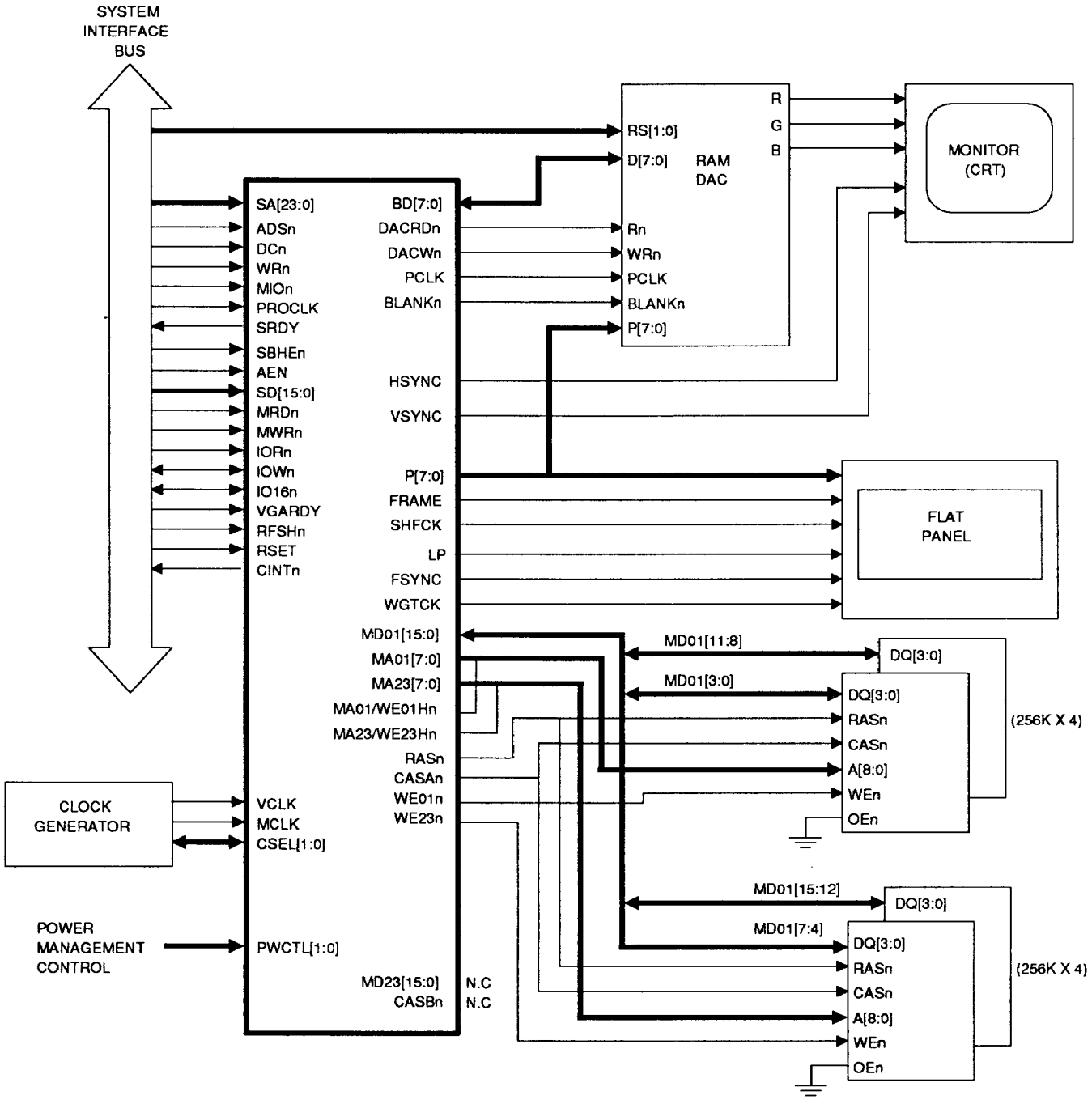
Local Bus Video System Block Diagram 256K x 4



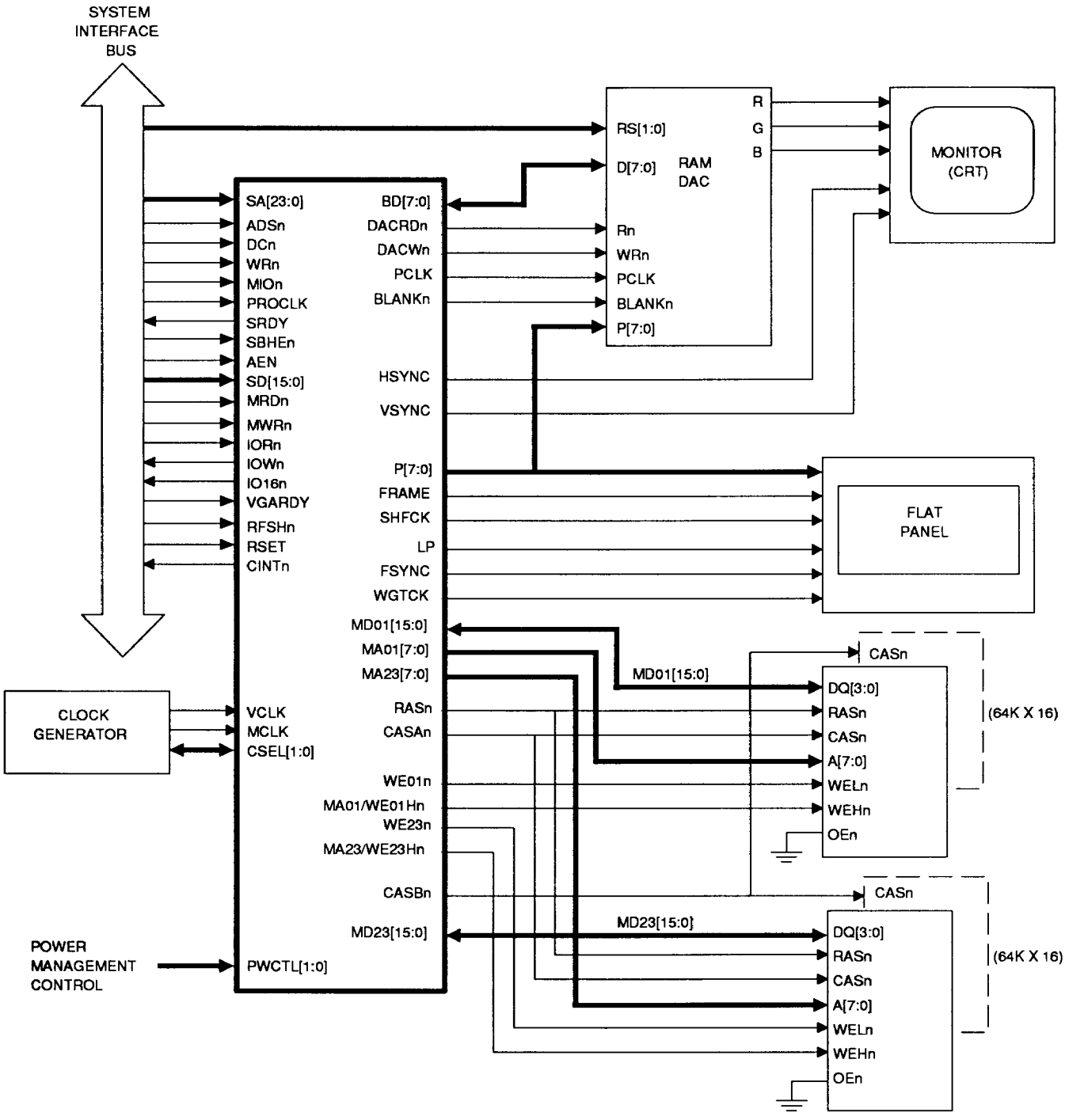
Local Bus Video System Block Diagram 64K x 16



On-Board Video System Block Diagram 256K x 4



On-Board Video System Block Diagram 64K x 16



Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
CPU Bus Interface			
AEN	TBA	I	ADDRESS ENABLE. An active-high signal used to qualify the video memory I/O access from CPU. When it is high, the DMA controller has control of the address bus, data bus and command bus.
RFSHn	TBA	I	REFRESH. An active-low signal used to qualify the video memory access from CPU. When it is low, it indicates a memory refresh cycle.
IORn	TBA	I	I/O READ. An active-low I/O read strobe, asserted in 8/16-bit I/O cycles.
IOWn	TBA	I	I/O WRITE. An active-low I/O write strobe, asserted in 8/16-bit I/O write cycles.
MRDn	TBA	I	MEMORY READ. An active-low memory read strobe, asserted in 8/16-bit memory read cycles.
MWRn	TBA	I	MEMORY WRITE. An active-low memory write strobe, asserted in 8/16-bit memory write cycles.
RSET	TBA	I	RESET. An active high system reset signal. This input signal will reset the flat panel controller and initialize the configuration register based on the logic level on BD[7:0] pins at power-up reset time. In on-board mode, this pin is connected to CPU Reset and it is used to determine the phase of the processor clock.
VGARDY	TBA	O	VGA READY. An open collector, active high output to signal the processor that it is ready for memory access. This signal is used to add wait states to the bus cycle during video memory access. It is pulled low by the flat panel controller right after the video memory access request by the CPU to allow additional time to finish the memory cycle.
CINTn	TBA	O	CRT INTERRUPT REQUEST. An interrupt request is generated when a vertical retrace occurs if it is enabled by Bit 5 in the Vertical Retrace End register. It is an active-low, open-collector output.
M16n (SRDY)	TBA	O	16-BIT MEMORY. An active-low, open-drain output signal used to indicate to the system that the present data transfer is a 16-bit memory cycle. It is derived from the decode of LA17 through LA23. In local bus mode, this pin functions as an open-drain, active-low output used to indicate the termination of a CPU bus cycle.
IO16n	TBA	O	16-BIT I/O. An active-low, open-collector output signal used to indicate to the system that the current data transfer is a 16-bit I/O cycle. It is derived from an address decode.

Pin Name	Pin Number	Pin Type	Description
CPU Bus Interface (Continued)			
BHENn	TBA	I	BYTE HIGH ENABLE. When the flat panel is in the 16-bit mode, this active-low signal indicates a transfer of data on the high byte of the data bus (SD[15:8]).
SD[15:8]	TBA	I/O	DATA LINES 15-8. CPU data bus bits 15-8.
SD[7:0]	TBA	I/O	DATA LINES 7-0. CPU data bus bits 7-0.
SA[23:0]	TBA	I	ADDRESS LINES 23-0. In non-local bus mode, SA[19:0] are connected to the CPU address bus bits 19-0 and SA[23:20] are connected to LA[23:20]. In local bus mode, SA[23:0] are connected to the CPU address bus.
ADS (ALE)	TBA	I	ADDRESS STATUS. This input signal indicates a valid bus cycle in local bus mode. In non-local bus mode, this signal is used to latch valid address and decode from the microprocessor.
PROCLK	TBA	I	PROCESSOR CLOCK. In local bus mode, this pin is used to sample CPU status and address.
MIOn (ASEL)	TBA	I	MEMORY I/O SELECT. An active-low input used to distinguish between memory cycles and I/O cycles. In non-local bus mode, this input acts as the address select for the controller.
WRn	TBA	I	WRITE/READ. This input is used to distinguish between Read (active high) and Write (active-low) cycles.
DCn	TBA	I	DATA/CONTROL. This input is used to distinguish between Data cycles (active high) and Control cycles (active-low).
BIOS ROM Control ROMENLn (HLDA)	TBA	I/O	ROM LOW BYTE ENABLE. An active-low signal to enable/control the low byte of BIOS to the low byte of the CPU data bus in 16-bit BIOS mode. This bit is not used in 8-bit mode. In local bus mode, this signal functions as hold acknowledge signal from the CPU to indicate a DMA cycle or master cycle..
BD[7:0]	TBA	I/O	DATA LINE 7-0. Data bits 7-0 of BIOS high-byte data in 16-bit BIOS mode, or single-byte data in 8-bit BIOS mode. Also, data bits of DAC and dipswitch.
Clock Interface			
VCLK	TBA	I	VIDEO CLOCK. This is the master input dot clock for the flat panel controller chip.
MCLK	TBA	I	MEMORY CLOCK. This is a direct input clock used for DRAM access timing.
CSEL0-1 (CLK0-1)	TBA	I/O	CLOCK SELECT 0-1. Clock select lines 0-1. These two pins reflect the value of the miscellaneous output register 3C3 bits 2 and 3. This pin can be redefined through the status register as input clocks.

Pin Name	Pin Number	Pin Type	Description
CRT, Flat Panel and RAMDAC Interface			
HSYNC	TBA	I/O	HORIZONTAL SYNC. Horizontal synchronization pulse to display monitor. The polarity of the pulse is determined by Bit 6 of the Miscellaneous Output Register (Bit 6 of 3DFh, index 12h).
VSYNC	TBA	I/O	VERTICAL SYNC. Vertical synchronization pulse to display monitor. The polarity of the pulse is determined by Bit 7 of the Miscellaneous Output Register (Bit 7 of 3DFh, index 12h).
BLANKn	TBA	O	BLANK. Active-low output signal to RAMDAC to blank the pixel data for the display monitor.
P[7:0]	TBA	O	PIXEL DATA. Pixel data bits 7-0, output to external color palette for color mapping during CRT display . It is also output to the flat panel as the is display data.
FRAME	TBA	O	FRAME. Active high output signal to the flat panel. It is used as the back bias signal for the LCD panel.
SHFCK	TBA	O	SHIFT CLOCK. Clock output to the flat panel to latch the pixel data, P0-7. It is derived from the internal character clock.
LP	TBA	O	LOAD PULSE. An active high output signal to the flat panel to latch the data into the internal shift register of the flat panel.
FSYNC	TBA	O	FRAME SYNC. Frame synchronization pulse to the flat panel.
WGTCK/DE	TBA	O	WEIGHT CLOCK or DISPLAY ENABLE. An active high output signal. Reference clock for the pulse width modulation to achieve different grayshades. It can also be redefined as display enable and will go active during display time.
DACRn	TBA	O	RAMDAC READ. An active-low I/O read signal generated for reading external color palette registers.
DACWn	TBA	O	RAMDAC WRITE. An active-low I/O write signal generated for writing external color palette registers.
PCLK	TBA	O	PIXEL CLOCK. Pixel clock output to AC to latch the pixel data P7-0.
Video Memory Interface			
MA0[7:0]	TBA	O	MEMORY ADDRESS. Memory address lines 7-0 for memory maps 0 and 1.
MA23[7:0]	TBA	O	MEMORY ADDRESS. Memory address lines 7-0 for memory maps 2 and 3.
MD01[15:0]	TBA	I/O	MEMORY DATA. Memory data lines 15-0 for maps 0 and 1. In the 64K x 16 configuration, these bits are used as the memory data bits 15-0 for maps 0 and 1. With two 256K x 4 DRAMs, bits 3-0 are for maps 0, 1 and bits 7-4 are for maps 2 and 3. With four 256K x 4 DRAMs, bits 3-0 and 11-8 are for maps 0 and 1, and bits 7-4 and 15-12 are for maps 2 and 3.

Pin Name	Pin Number	Pin Type	Description
Video Memory Interface (Continued)			
MD23[15:0]	TBA	I/O	MEMORY DATA. Memory data lines 15-0 for maps 2 and 3. In the 64K x 16 configuration, these bits are used as the memory data bits 15-0 for maps 0 and 1. With 256K x 4 DRAMS, these lines are not used.
RASn	TBA	O	ROW ADDRESS STROBE. Active-low output signal to all video memory maps.
CASAn	TBA	O	COLUMN ADDRESS STROBE. Active-low output signal to all video memory maps.
CASBn	TBA	O	COLUMN ADDRESS STROBE. Active-low output signal to Bank B in the 64K x 16 configuration.
WE01n	TBA	O	WRITE ENABLE. Active-low write enable pulse to memory maps 0 and 1 in the 256K x 4 configuration. Active-low, write enable pulse to map 0 in the 64K x 16 configuration.
WE023n	TBA	O	WRITE ENABLE. Active-low write enable pulse to memory maps 1 and 3 in the 256K x 4 configuration. Active-low, write enable pulse to map 2 in the 64K x 16 configuration.
MA/WE01Hn	TBA	O	MEMORY ADDRESS BIT 8. For maps 0 and 1 in the 256K x 4 configuration. Low-active WRITE ENABLE for map 1 in the 64K x 16 configuration.
MA/WE23Hn	TBA	O	MEMORY ADDRESS BIT 8. For maps 2 and 3 in the 256K x 4 configuration. Low-active WRITE ENABLE for map 3 in the 64K x 16 configuration
Miscellaneous			
SWSENSE	TBA	I	SWITCH SENSE. An input signal used to auto detect the monitor type.
PWCTL[1:0]	TBA	I	POWER CONTROL. These two bits are used to indicate various modes of power saving.