SGS-THOMSON MICROELECTRONICS

STV0300

FAST SINGLE CHIP OF 8192 COMPLEX POINT FAST FOURIER TRANSFORM

PRELIMINARY DATA

- PROGRAMMABLE FFT SIZE FROM 2 TO 8192 COMPLEX WORDS
- 16K WORDS OF ON-CHIP MEMORY (NO EXTERNAL MEMORY NEEDED). HALF OF THE MEMORY ACTS AS AN INPUT BUFFER TO ALLOW SERIAL PROCESSING OF ADJACENT DATA BLOCKS.
- INPUT SAMPLING FREQUENCY AT 20MHz :
  - 8192 FFT PERFORMED EVERY 410µs
  - 4096 FFT PERFORMED EVERY 205µs
  - 2048 FFT PERFORMED EVERY 103µs
  - 1024 FFT PERFORMED EVERY 52µs
  - 512 FFT PERFORMED EVERY 26µs
  - 256 FFT PERFORMED EVERY 13µs
  - 128 FFT PERFORMED EVERY 7µs
  - 64 FFT PERFORMED EVERY 4µs
  - 32 FFT PERFORMED EVERY 2µs
- 2 x 10 BIT COMPLEX INPUT IN NATURAL ORDER FOR 8192-POINTS AND 4092-POINTS FFT
- 2 x 12 BIT COMPLEX INPUT IN NATURAL ORDER FOR FFT OF UP TO 2048 COMPLEX POINTS
- 10-BIT ACCURACY FOR SINE AND COSINE VALUES
- 2 x 12 BIT INTERNAL ACCURACY
- 2 x 12 BIT COMPLEX OUTPUT IN BIT REVERSE ORDER
- DIRECT OR INVERSE FFT
- PROCESSING OF $\{x_n\}$ or $\{-1^n x_n\}$

APPLICATIONS

- ORTHOGONAL FREQUENCY DIVISION MULTIPLEX (DIGITAL AUDIO BROADCASTING, DIGITAL TERRESTRIAL TV BROADCASTING)
- SINGLE FREQUENCY NETWORKS FOR DIGITAL TV
- SPECTRAL ANALYSIS (MEASUREMENT SYSTEMS, RADARS, ...)
- FIR FILTERING

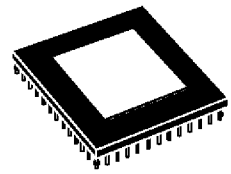
TECHNICAL FEATURES

- INPUT SAMPLING FREQUENCY :
  - MINIMAL : 1kHz
  - MAXIMAL : 30MHZ
- LATENCY (BETWEEN FIRST DATA OF INPUT BLOCK AND FIRST DATA OF OUTPUT BLOCK) :
  - 8192 POINTS : 8918 CYCLES
  - 4096 POINTS :6870 CYCLES
  - 2048 POINTS : 2768 CYCLES
  - 1024 POINTS : 1744 CYCLES
  - 512 POINTS : 714 CYCLES
  - 256 POINTS : 458 CYCLES
  - 128 POINTS : 196 CYCLES
  - 64 POINTS : 132 CYCLES
  - 32 POINTS : 62 CYCLES
  - 16 POINTS : 46 CYCLES
  - 8 POINTS : 24 CYCLES
  - 4 POINTS : 20 CYCLES
  - 2 POINTS : 12 CYCLES
  - 1 POINT(TEST MODE) : 12 CYCLES
- INPUT LEVEL :
  TTL COMPATIBLE, 0 -3.3V ± 10% (3V-3.6V)
- DISSIPATED POWER : 0.6W at 20MHz

DESCRIPTION

This chip is dedicated to the computation of Fast Fourier Transforms of up to 8192 complex points. It includes all necessary data and coefficient storage elements (350 kbits of internal memory) for single chip operation.
This component has been specified with the CCETT and developed by the CNET of Grenoble for the validation of the single frequency network concept in an OFDM digital terrestrial television system. SGS-THOMSON is licensed by France Telecom CNET.

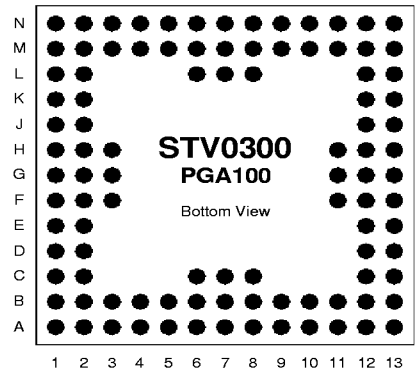
PRODUCT STATUS :
Non Recurring Engineering Samples available.



PGA100
(Ceramic Grid Array Package)

ORDER CODE : STV0300S

PIN CONNECTIONS



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PIN DESCRIPTION

Pad Name	Pin	Type	Levels	Description
CK	N5	I	0 - 3.3V	Clock
SYNC_IN	N11	I	0 - 3.3V	Each block of data must begin on a rising edge of SYNC_IN synchronous to the rising edge of CK.
IN_R[11] IN_R[10] IN_R[9] IN_R[8] IN_R[7] IN_R[6] IN_R[5] IN_R[4] IN_R[3] IN_R[2] IN_R[1] IN_R[0]	E1 F3 F2 F1 H1 H2 H3 J1 J2 K1 K2 L1	I	0 - 3.3V	Input data real part two complement's notation for 8192-points and 4096-points FFT, IN_R[1:0] is not used and can be left unconnected (internally tied to ground level) synchronous to the rising edge of CK.
IN_I[11] IN_I[10] IN_I[9] IN_I[8] IN_I[7] IN_I[6] IN_I[5] IN_I[4] IN_I[3] IN_I[2] IN_I[1] IN_I[0]	B5 A4 A3 A2 B3 A1 B1 C2 C1 D2 D1 E2	I	0 - 3.3V	Input data imaginary part two complement's notation for 8192-points and 4096-points FFT, IN_I[1:0] is not used and can be left unconnected (internally tied to ground level) synchronous to the rising edge of CK.
MINUS	N10	I	0 - 3.3V	When MINUS is high, the corresponding data is multiplied by -1 synchronous to the rising edge of CK.
LEN[3] LEN[2] LEN[1] LEN[0]	M1 L2 N1 M3	I	0 - 3.3V	FFT length : - 8192 points FFT when 1101 - 4096 points FFT when 1100 - 2048 points FFT when 1011 - 1024 points FFT when 1010 - 512 points FFT when 1001 - 256 points FFT when 1000 - 128 points FFT when 0111 - 64 points FFT when 0110 - 32 points FFT when 0101 - 16 points FFT when 0100 - 8 points FFT when 0011 - 4 points FFT when 0010 - 2 points FFT when 0001 - 1 point FFT when 0000 Values 1110 and 1111 should not be selected. Synchronous to the rising edge of CK.

0300-01.TBL

PIN DESCRIPTION (continued)

Pad Name	Pin	Type	Levels	Description
GAIN_IN	N12	I	0 - 3.3V	In order to improve SNR for 8192 points FFT only (recommended value : 1, 0 for high dynamic input).
GAIN_OUT[3] GAIN_OUT[2] GAIN_OUT[1] GAIN_OUT[0]	N3 M4 N4 M5	I	0 - 3.3V	In order to compute circuit gain (see §2 for limit values).
FFTINV	M10	I	0 - 3.3V	Direct FFT when low, inverse FFT when High.
TEST_IN[7] TEST_IN[6] TEST_IN[5] TEST_IN[4] TEST_IN[3] TEST_IN[2] TEST_IN[1] TEST_IN[0]	L6 N6 M7 L7 N8 M8 L8 M9	I	0 - 3.3V	To be set to low for normal operation mode.
NRST	N13	I	0 - 3.3V	Chip reset, synchronous to the rising edge of CK.
SYNC_OUT	M13	O	0 - V_{DD}_P	A high level occurs on the first data of a block synchronous to the rising edge of CK.
OUT_R[11] OUT_R[10] OUT_R[9] OUT_R[8] OUT_R[7] OUT_R[6] OUT_R[5] OUT_R[4] OUT_R[3] OUT_R[2] OUT_R[1] OUT_R[0]	A13 B13 C13 D13 E12 E13 F12 F13 H12 H11 J13 J12	O	0 - V_{DD}_P	Output data real part two complement's notation bit reverse order synchronous to the rising edge of CK.
OUT_I[11] OUT_I[10] OUT_I[9] OUT_I[8] OUT_I[7] OUT_I[6] OUT_I[5] OUT_I[4] OUT_I[3] OUT_I[2] OUT_I[1] OUT_I[0]	A5 C6 B6 A6 A7 A8 B8 C8 A9 A11 B11 B12	O	0 - V_{DD}_P	Output data imaginary part two complement's notation bit reverse order synchronous to the rising edge of CK.
TEST_OUT[3] TEST_OUT[2] TEST_OUT[1] TEST_OUT[0]	K13 K12 L13 L12	O	0 - V_{DD}_P	Output test pins can be left unconnected.
V_{SS}	B2, G3, G1, M2, M12, G12, G11, G13, A12, B10, A10, B9	G	0V	Ground
V_{DD}_P	G2, N7, H13, C7	P	3.3V	Power for pad
V_{CC}_C	N2, M6, N9, M11, F11, D12, C12, B7, B4	P	3.3V	Power

0300-01.TBL

FUNCTIONAL DESCRIPTION

The FFT8K chip uses a pipelined architecture to compute the FFT (see Figure 1). Such an architecture allows high speed processing without the need of a fast clock. All computations are synchronous to the input data sampling clock (up to 30MHz).

The chip contains :

- an input interface that latches inputs,
- an output interface which controls the circuit gain and latches outputs,
- a control block which enables or not the radix-2 stage or the radix-4 stages depending on the FFT length and defines the circuit gain,
- a radix-2 stage,
- 6 radix-4 stages.

The FFT8K chip works on data organized into blocks whose size is equal to the FFT length. Each block must start on a rising edge of SYNC_IN which must remain high at least one cycle. Similarly, the chip generates a high level on the SYNC_OUT pad during the first data of an output block. Input data are in natural order ; output data are in bit reverse order. Figure 2 shows an example for an 8-point FFT.

Due to its pipelined architecture, the FFT8K chip is able to process a continuous data flow : it can read a new block while processing the previous one (see Figure 3).

Between two consecutive symbols, non valid data can be inserted (see Figure 4).

Figure 1 : Architecture

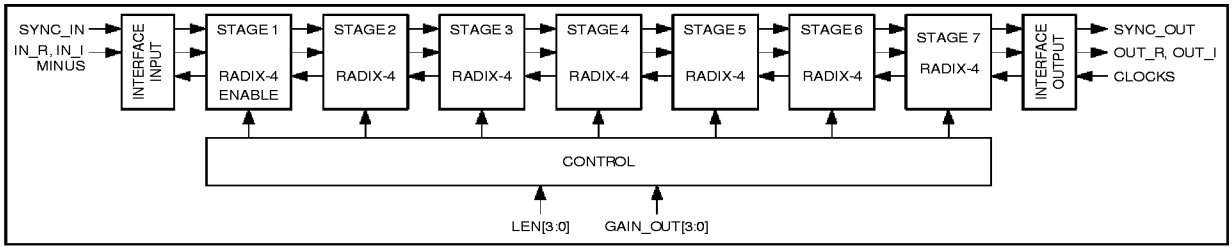


Figure 2 : 8-points FFT Example

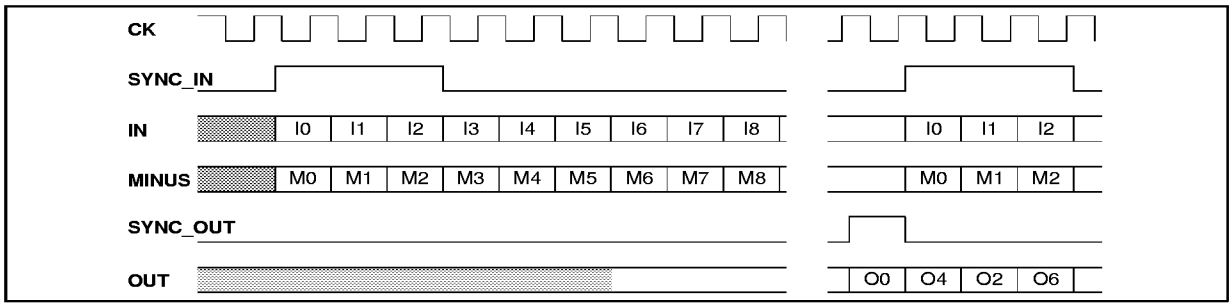
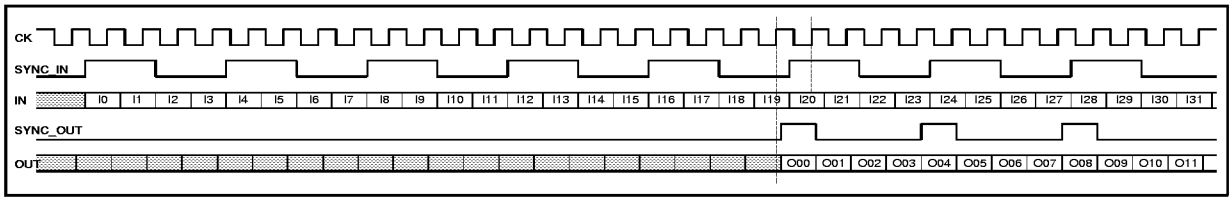
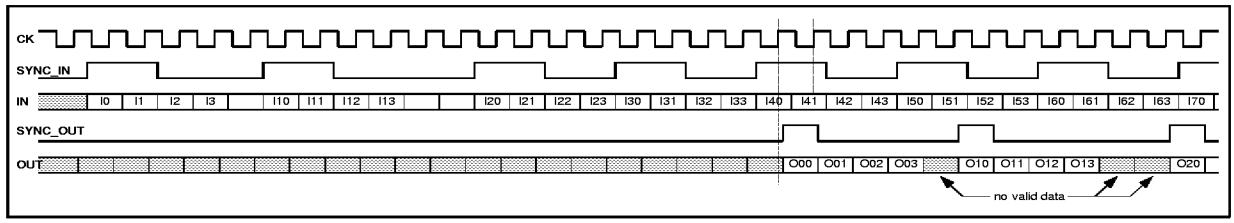


Figure 3 : 4-points FFT Example



FUNCTIONAL DESCRIPTION (continued)

Figure 4 : 4-points FFT Example (with guard interval)



If the input of the current block is still going on (there has been no rising edge on the SYNC_IN to indicate the beginning of new block), the data available at the output pins after the complete result of this block are not valid (see Figure 5).

If symbol (between 2 sync pulses) is shorter than the FFT length, the output is non valid and no SYNC_OUT high level is generated (see Figure 6).

The circuit computes the following equation :

$$OUT(k) = G \times \Sigma\ (-1)^{MINUS(i)} \times IN(i)\ W^{ik}N$$

where $w^{ik}N = \exp((-1)^{(FFTINV)+1}\ 2ikP/N)$,

FFTINV must be set to 0 for a direct FFT and to 1 for an inverse FFT, MINUS is an input of the Circuit (used to select x_n or $(-1)^n x_n$, IN is the input data and is defined by its imaginary part IN_I and real part IN_R, OUT is the output data and is defined by its imaginary part OUT_I and its real part OUT_R. It is provided in the bit reverse order.

Circuit gain is given by the following equation :

- log2G = GAIN_OUT - |log4N| - 9 if N ≤ 8192
- log2G = GAIN_OUT - |log4N| - 10 if N = 8192 and GAIN_IN = 0
- log2G = GAIN_OUT - |log4N| - 8 if N = 8192 and GAIN_IN = 1

where N is the FFT length, |log4N| is the highest integer lower or equal to log4N, and GAIN_OUT a user selectable parameter to adjust the output dynamic.

8192 points	$-16 \le log2G \le 1$
4096 points	$-15 \le log2G \le 0$
2048 points	$-14 \le log2G \le 1$
1024 points	$-14 \le log2G \le 1$
512 points	$-13 \le log2G \le 2$
256 points	$-13 \le log2G \le 2$
128 points	$-12 \le log2G \le 3$
64 points	$-12 \le log2G \le 3$
32 points	$-11 \le log2G \le 4$
16 points	$-11 \le log2G \le 4$
8 points	$-10 \le log2G \le 5$
4 points	$-10 \le log2G \le 5$
2 points	$-9 \le log2G \le 6$
1 point	$-9 \le log2G \le 6$

Figure 5 : 4-points FFT Example (with SYNC_IN rising edge)

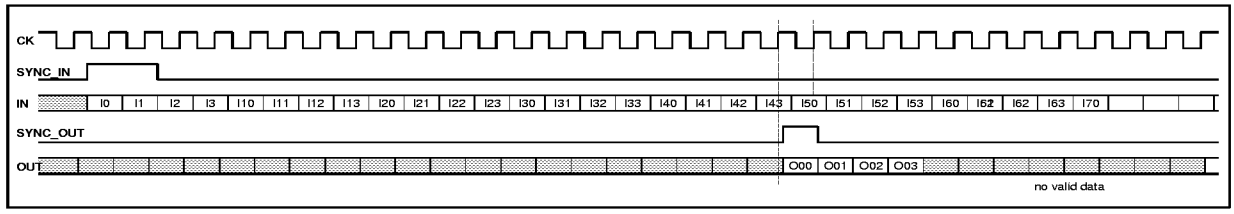
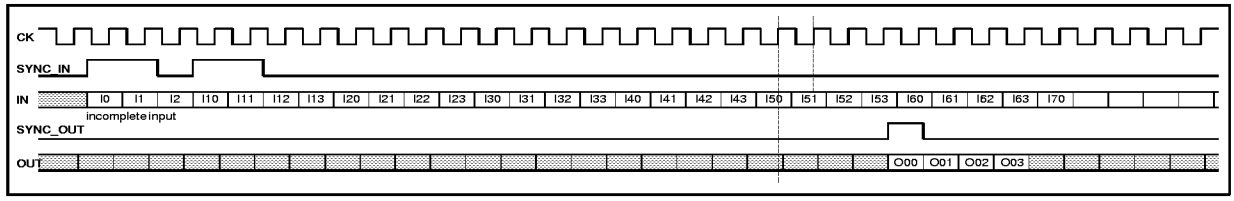


Figure 6 : 4-points FFT Example (with incomplete symbol)



RECOMMENDED OPERATING CONDITIONS

TT Levels : low = 0.4V, high = 2.4V - CMOS Output : low = 0V, high = V_{DD}_P - Maximum Output Load : 25pF

Symbol	Parameter	Value	Unit
V_{DD}_P, V_{DD}_C	Supply Voltage	3, 3.6	V
V_{SS}	Ground Voltage	0	V
T_{oper}	Operating Temperature	0, +85	°C

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Note : The inputs can not be directly connected to the outputs of TTL devices supplied with 5V and must be converted to 3.3V before connecting them on the chip. The outputs of the chip are able to supply TTL devices with 5V power supply.

TIMING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_C	Cycle Time	33			ns
t_{CL}	Low Level Hold Time for Clock	10			ns
t_{CH}	High Level Hold Time for Clock	10			ns
t_{SD}	Dat Set-up Time	-20			ns
t_{HD}	Data Hold Time	30			ns
t_{SR}	Sync_in Set-up Time	-20			ns
t_{HR}	Sync_in Hold Time	30			ns
t_{PO}	Output Propagation Time			15	ns
t_{PR}	Sync_out Propagation Time			15	ns

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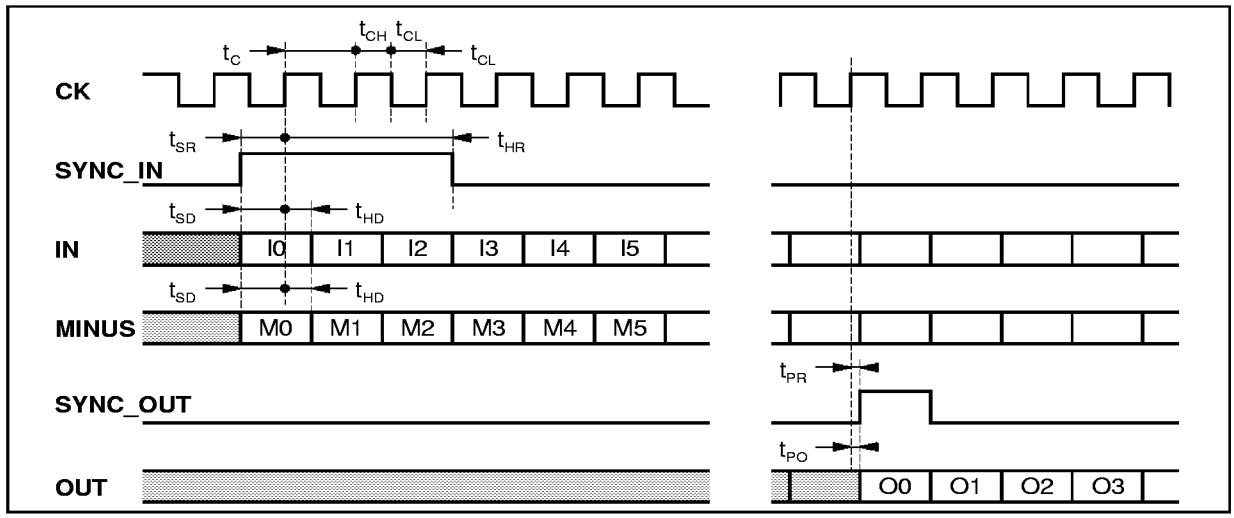
Figure 7 : Waveforms



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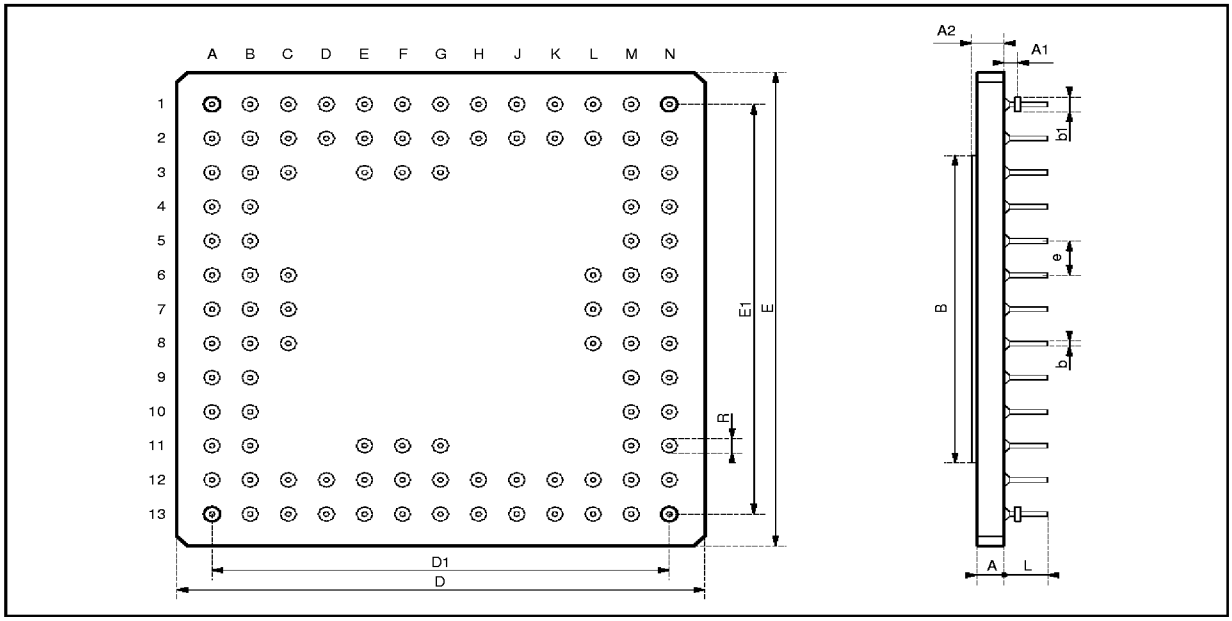
Note : The output is provided in the bit reverse order : for a 8-points FFT, X0, X4, X6, X1, X5, X3, X7.

PACKAGE MECHANICAL DATA

100 PINS - CERAMIC GRID ARRAY (PGA)



PMPG100B.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.24			0.088
A1			1.40			0.055
A2			2.54			0.100
B			17.78			0.700
b			0.50			0.020
b1			1.68			0.065
D			33.58			1.332
D1			30.78			1.212
E			33.58			1.332
E1			30.78			1.212
e		2.54			0.100	
L			4.70			0.185
R			1.78			0.070

PGA100B.TBL