

CRA90000

Reduced Pad Pitch CMOS Gate Arrays

DS4964-1.0

INTRODUCTION

CRA90000 is an extension to the Mitel CLA90000 family of gate arrays that offers reduced pad pitch, achieving excellent area savings for pad limited devices. CRA90000 offers a cost effective solution to FPGA conversion and inherits all of the CLA90000 design libraries and system level support for fast time to market.

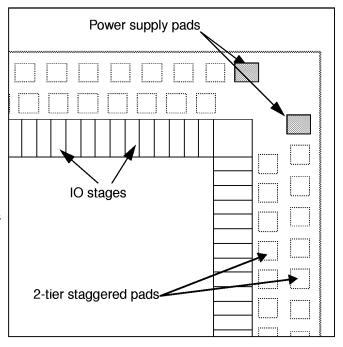
FEATURES

- Low power, 0.5µW/MHz/gate at 3V supply (NAND driving 2 input loads)
- 150ps gate delay for 2-input NAND driving two input loads (5V)
- Double or triple layer metal on a 0.6µm (drawn) process
- 208-pin,160-pin or 144-pin packages
- Low cost for pad limited designs
- All CLA90000 core cells, memories and complex cores available
- Embedded, mixed signal cells that connect directly to pads can be used in approved packages
- Simplified power supply options
- Power supply to sensitive input cells can be isolated
- 3.3V or 5V operation
- Up to 6mA drive from a single I/O cell

ARRAY SIZES

Array	No. of Gates	Typical Utilization of Gates		Number of
		2-layer metal	3-layer metal	Pads
CRA 905	49928	20000	30000	≤ 168
CRA 907	84872	34000	51000	≤ 216

BASE ARCHITECTURE



I/O

- Fast and slow slew rate variants for low noise or high speed
- Pullup/pulldown options on input cells
- 2kV ESD protection
- Open source, open drain and tristate outputs
- CMOS and TTL compatible variants

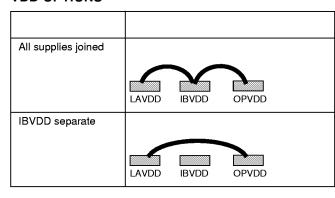
CRA90000 I/O offers most of the features of CLA90000 I/O on single voltage, reduced pad pitch arrays. Output drive strengths are 2, 4 and 6mA giving very low noise. If required, I/O cells that connect in parallel could be designed to drive loads of up to 12mA.

CRA90000

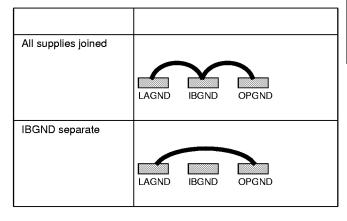
SUPPLY OPTIONS

CRA90000 has three VDD rails and three GND rails, which supply the core, intermediate buffer and output areas. Devices must be single voltage, but the intermediate buffer supply rails can be separated for noise isolation. The following power supply configurations are available:

VDD OPTIONS



GND OPTIONS



CAE SUPPORT

CLA90000 and CRA90000 have identical design tool support, including the following features:

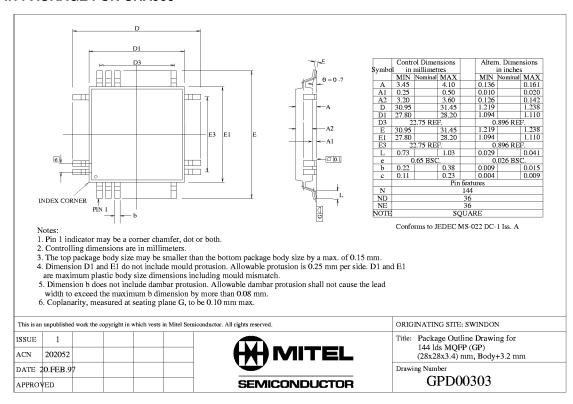
- Synthesis with Synopsys, Mentor or Cadence
- Sign-off simulation with Mentor, Cadence or Synopsys VCS simulators
- VITAL compliant library
- Full top-down design flow support
- Point tools supported, including Zycad and Powermill
- Direct route to layout and test
- Advanced delay modelling and netlist checking

The Mitel Universal Delay Compiler (UDC) is supplied with all design kits for advanced delay modelling and comprehensive netlist checking. The UDC matches Synopsys and Mentor native delay calculation.

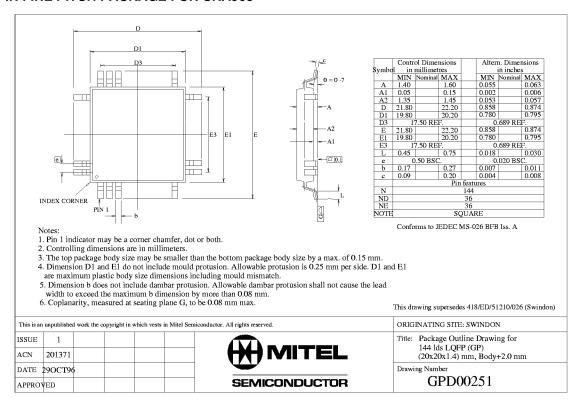
PACKAGING

Array	Number of Pads	Packages
CRA 905	≤ 168	144 MQFP, 144 LQFP (Fine Pitch)
CRA 907	≤216	160 MQFP, 208 MQFP

144-PIN PACKAGE FOR CRA905

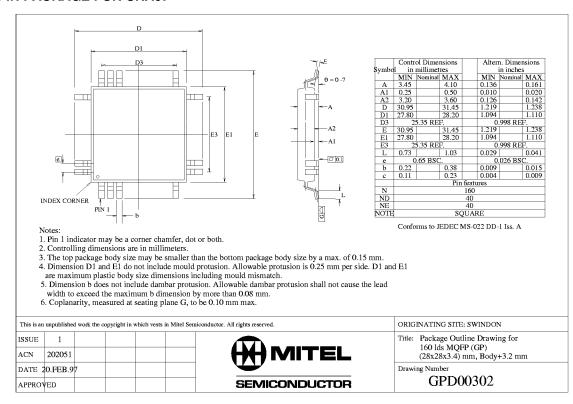


144-PIN FINE PITCH PACKAGE FOR CRA905



CRA90000

160-PIN PACKAGE FOR CRA07



208-PIN PACKAGE FOR CRA907

