

HM674256UH Series Under development

262144-words × 4-bits High Speed Static Random Access Memory

Features

- 262144-words × 4-bits organization
- Directly TTL compatible input and output
- Choice of 5.0 V or 3.3 V power supplies for output buffers
- Completely static memory
- No clock or timing strobe required
- Super fast access time: 10/12 ns (max)
- Revolutionary pin arrangement

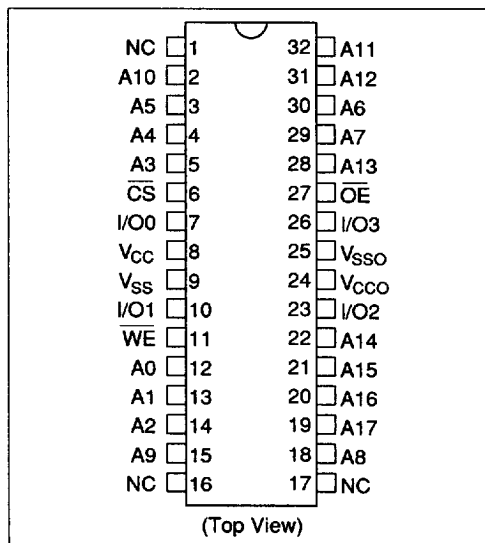
Ordering Information

Type No.	Access time	Package
HM674256UHJ-10	10 ns	400 mil 32pin Plastic SOJ
HM674256UHJ-12	12 ns	(CP-32DB)

Pin Description

Pin name	Function
A0 – A17	Address input
I/O0 – I/O3	Data input/output
WE	Write enable
CS	Chip select
OE	Output enable
V _{CC}	+5 V power supply
V _{CCO}	Output buffer power supply
V _{SSO}	Output buffer ground
V _{SS}	Ground
NC	No connection

Pin Arrangement



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Note: This document contains information on a product under development.
Hitachi reserves the right to change or discontinue the product without notice.

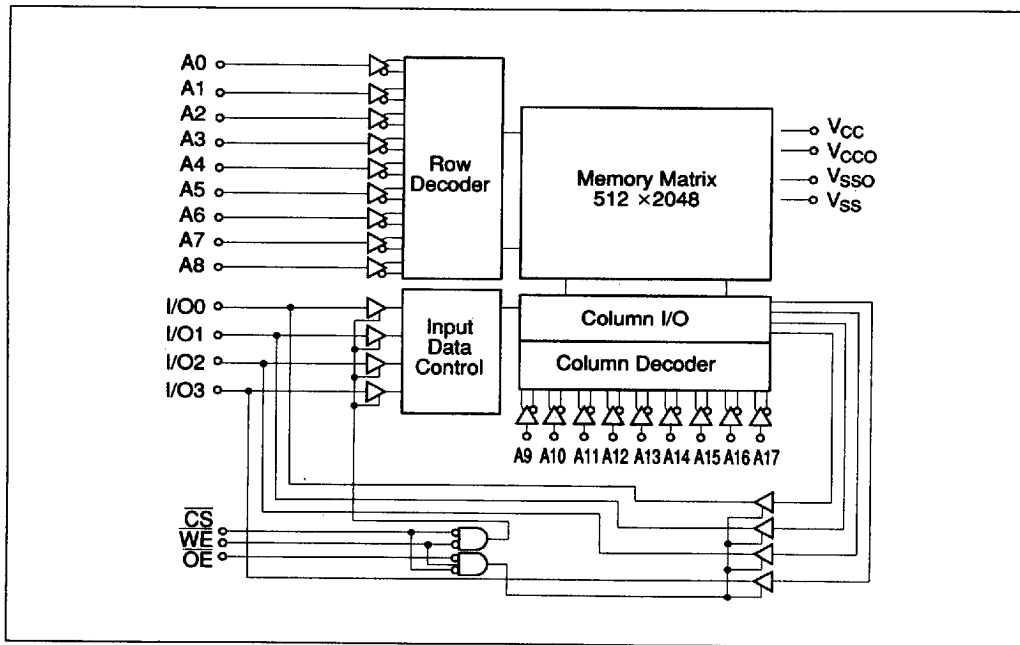
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Block Diagram



Function Table

Input

CS	WE	OE	Output	Mode	V _{CC} current	Reference cycle
H	X	X	High-Z	Not selected	I _{SB} , I _{SB1}	—
L	H	H	High-Z	Output disable	I _{CC} , I _{CC1}	—
L	H	L	Data out	Read	I _{CC} , I _{CC1}	Read cycle 1, 2, 3
L	L	H	Data in	Write	I _{CC} , I _{CC1}	Write cycle 1, 2, 3, 4
L	L	L	Data in	Write	I _{CC} , I _{CC1}	Write cycle 5, 6

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS} *1	V_T	-0.5 to $V_{CC} + 0.5$	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range (with bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage temperature range	T_{stg}	-55 to +125	°C

Note: 1. With respect to $V_{SS} = V_{SSO}$

For the DC and AC specifications shown in these tables, this device was tested under a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (0°C ≤ Ta ≤ 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
5 V TTL compatible	V_{CCO}	4.5	5.0	5.5	V
3.3 V TTL compatible		3.0	3.3	3.6	V
	V_{SS}, V_{SSO}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.5$	V
Input low voltage	V_{IL}	-0.5	—	0.8	V

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DC Characteristics ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{CCO} = 5.0 \text{ V} \pm 10\%$ or $3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = V_{SSO} = 0 \text{ V}$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

		HM674256UH					
		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	2	—	2	μA	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 0\text{ V to } V_{CC}$
Output leakage current	$ I_{LO} $	—	10	—	10	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IL}$, $V_{I/O} = 0\text{ V to } V_{CCO}$
Operating power supply current	I_{CC}	—	120	—	120	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0\text{ mA}$
Average operating current	I_{CC1}	—	170	—	160	mA	Min. cycle, $I_{I/O} = 0\text{ mA}$
Standby power supply current	I_{SB}	—	40	—	40	mA	$\overline{CS} = V_{IH}$
	I_{SB1}	—	30	—	30	mA	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$
Output low voltage	V_{OL}	—	0.4	—	0.4	V	$I_{OL} = 8\text{ mA}$
Output high voltage	V_{OH}	2.4	—	2.4	—	V	$I_{OH} = -4\text{ mA}$

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Max	Unit	Test condition
Input capacitance	C_{IN}^{*1}	6	pF	$V_{IN} = 0 \text{ V}$
Input/output capacitance	$C_{I/O}^{*1}$	10	pF	$V_{I/O} = 0 \text{ V}$

Note: 1. This parameter is sampled and has not been 100% tested.

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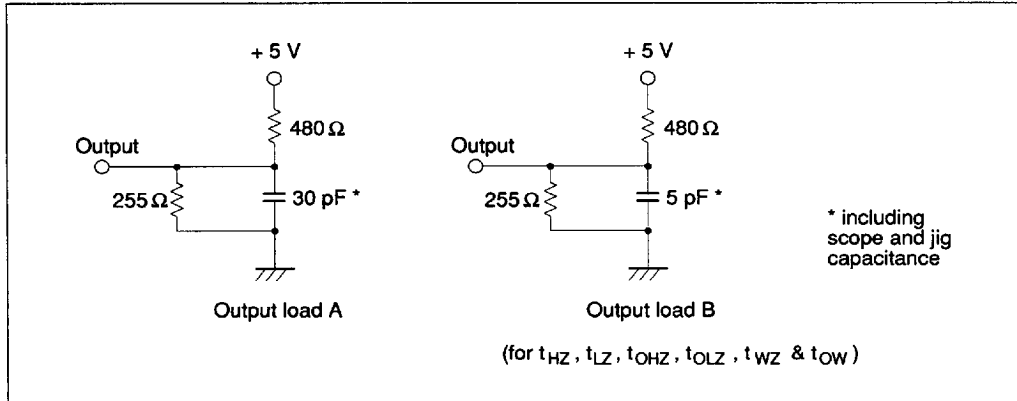
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AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{CCO} = 5.0\text{ V} \pm 10\%$ or $3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = V_{SSO} = 0\text{ V}$, $T_a = 0\text{ to } +70^\circ\text{C}$, unless otherwise noted)

Test conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure
- Input rise and fall time: 4 ns
- Output reference level: 1.5 V



Read Cycle

		HM674256UH				
		-10		-12		
Parameter	Symbol	Min	Max	Min	Max	Unit
Read cycle time	t _{RC}	10	—	12	—	ns
Address access time	t _{AA}	—	10	—	12	ns
Chip select access time	t _{ACS}	—	10	—	12	ns
Chip selection to output in low-Z	t _{LZ} ^{*1, *2}	3	—	4	—	ns
Output enable to output valid	t _{OE}	—	5	—	6	ns
Output enable to output in low-Z	t _{OLZ} ^{*1, *2}	0	—	0	—	ns
Chip deselection to output in high-Z	t _{HZ} ^{*1, *2}	0	5	0	6	ns
Output hold from address change	t _{OH}	3	—	4	—	ns

Notes: 1. This parameter is sampled and has not been 100% tested.
 2. Transition is measured $\pm 200\text{ mV}$ from steady state voltage with specified loading in Load (B).

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Write Cycle

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		-10		-12		
Parameter	Symbol	Min	Max	Min	Max	Unit
Write cycle time	t _{WC} ^{*1}	10	—	12	—	ns
Chip selection to end of write	t _{CW}	8	—	10	—	ns
Address valid to end of write	t _{AW}	8	—	10	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write pulse width	t _{WP}	8	—	10	—	ns
Write recovery time	t _{WR}	0	—	0	—	ns
Data valid to end of write	t _{DW}	5	—	6	—	ns
Data hold time	t _{DH}	0	—	0	—	ns
Write enable to output in high-Z	t _{WZ} ^{*2, *3}	0	5	0	6	ns
Output disable to output in high-Z	t _{OHZ} ^{*2, *3}	0	5	0	6	ns
Output active from end of write	t _{OW} ^{*2, *3}	0	—	0	—	ns

- Notes:
1. All write cycle timings are referred from the last valid address to the first transitioning address.
 2. This parameter is sampled and has not been 100% tested.
 3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

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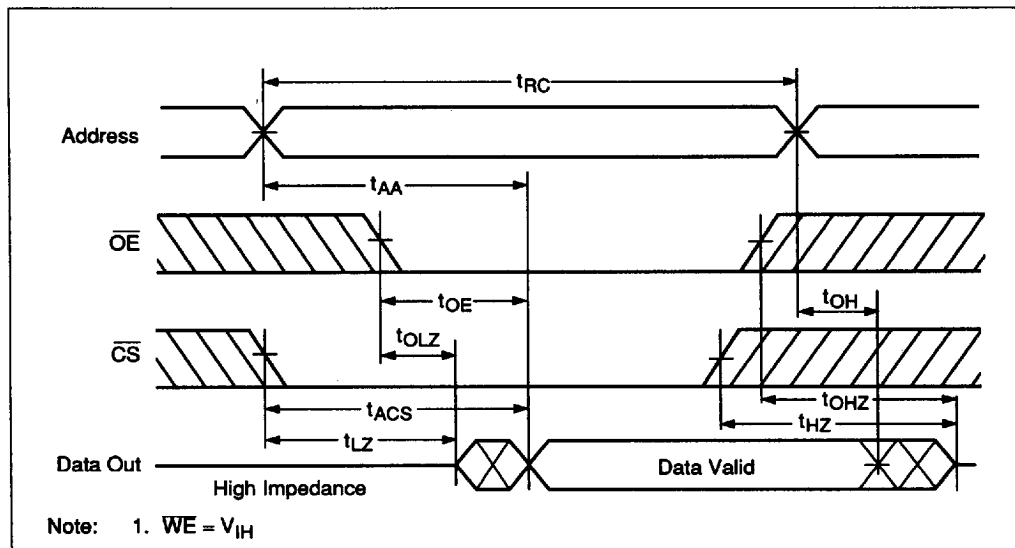
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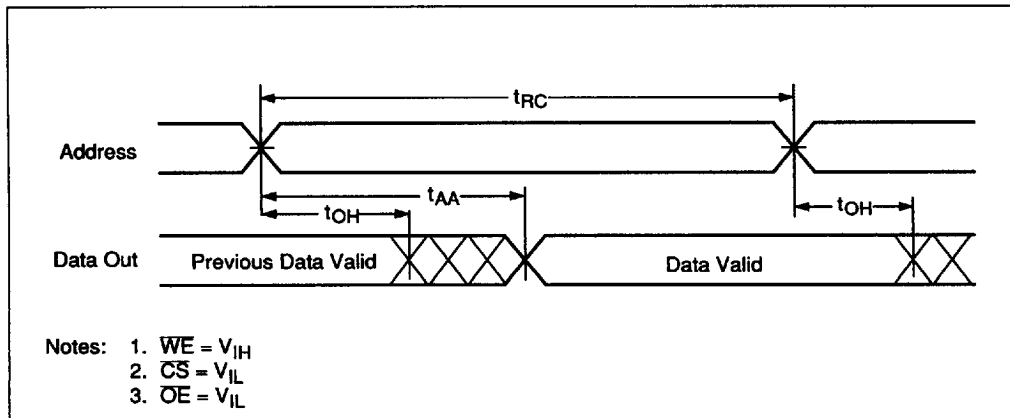
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Timing Waveforms

Read Cycle 1

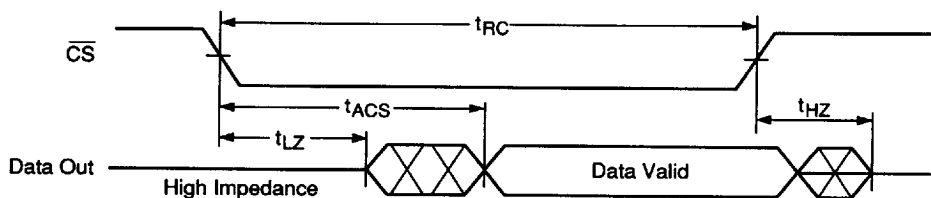


Read Cycle 2



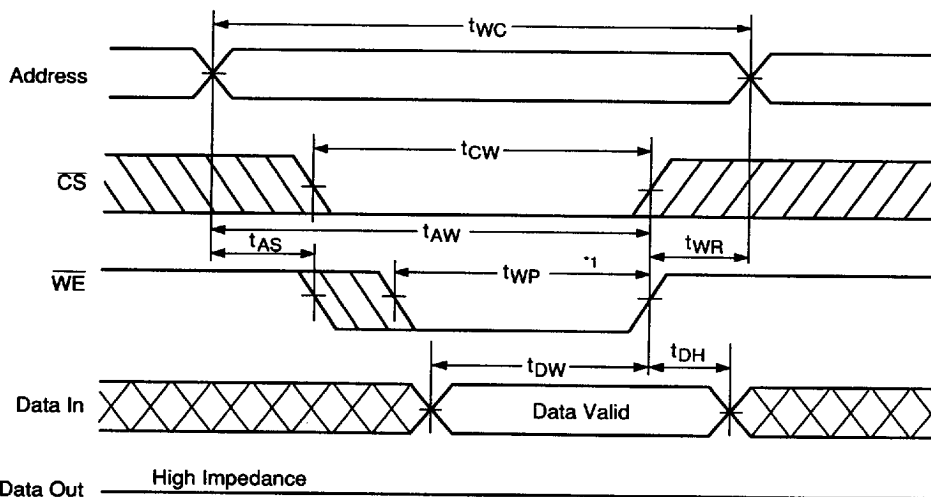
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Read Cycle 3



- Notes:
1. $WE = V_{IH}$
 2. $\overline{OE} = V_{IL}$
 3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE} = H$, $\overline{WE}$ Controlled)



- Note:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

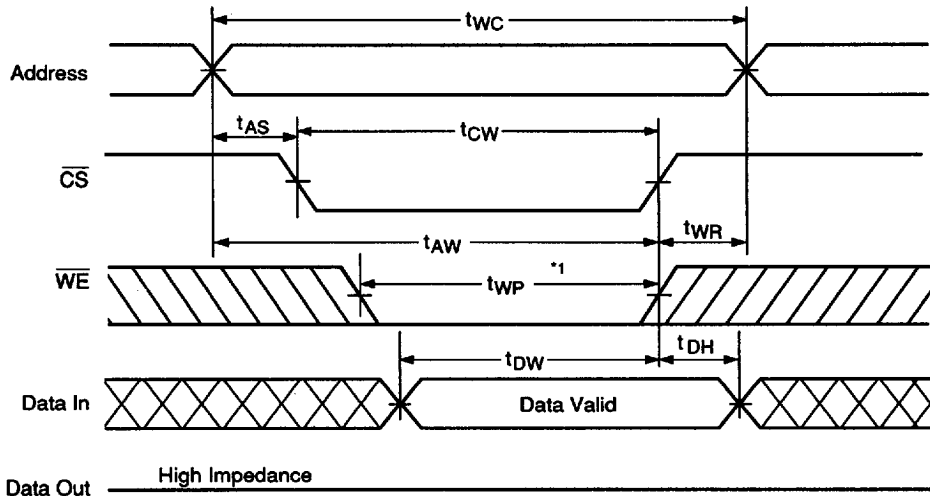
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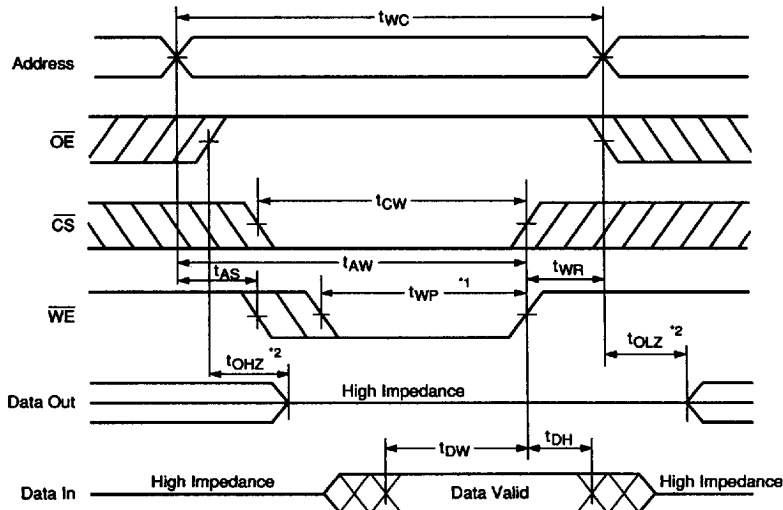
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Write Cycle 2 ($\overline{OE} = H$, $\overline{CS}$ Controlled)



Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

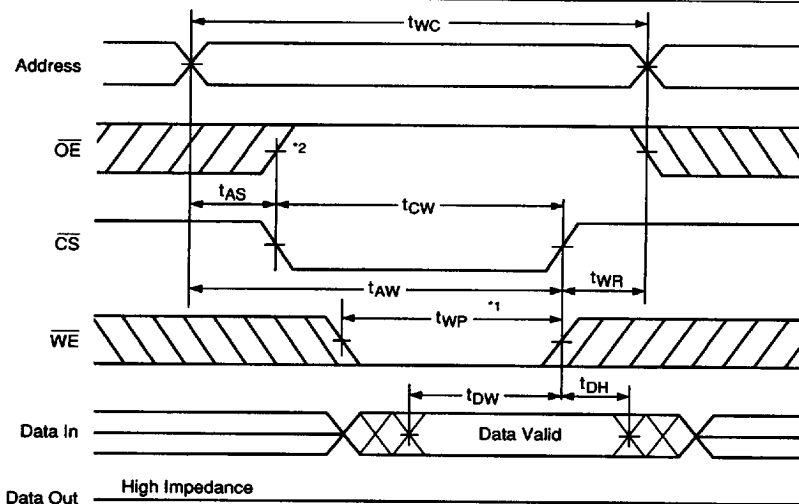
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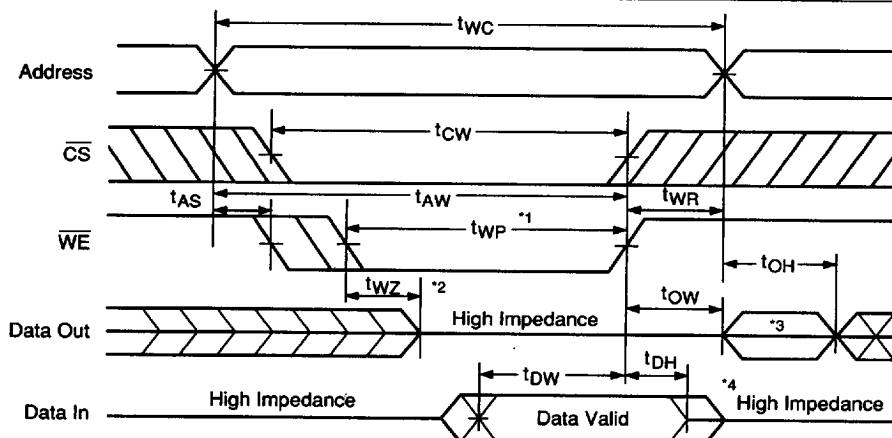
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Write Cycle 4 ($\overline{OE}$ = clocked, $\overline{CS}$ controlled)



- Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
 2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)

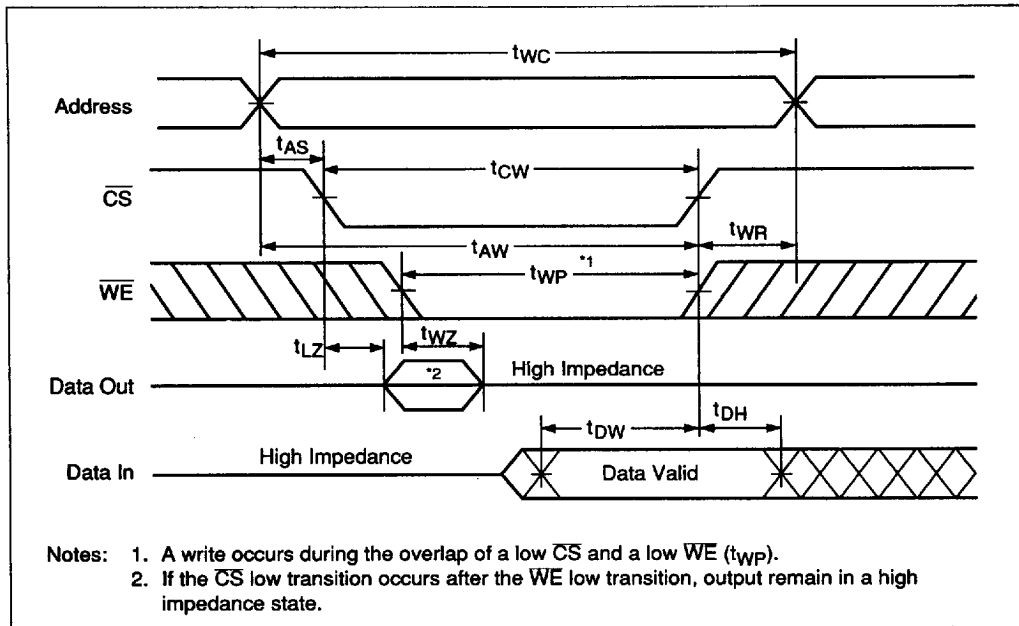


- Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
 2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
 3. Output data is the same phase of write data of this write cycle.
 4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

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Write Cycle 6 ($\overline{OE} = L$, $\overline{CS}$ controlled)



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