

## 184pin Unbuffered DDR SDRAM DIMMs based on 512Mb B ver.

This Hynix unbuffered Dual In-Line Memory Module (DIMM) series consists of 512Mb B ver. DDR SDRAMs in 400mil TSOP II packages on a 184pin glass-epoxy substrate. This Hynix 512Mb B ver. based unbuffered DIMM series provide a high performance 8 byte interface in 5.25" width form factor of industry standard. It is suitable for easy interchange and addition.

### FEATURES

- JEDEC Standard 184-pin dual in-line memory module (DIMM)
- Two ranks 128M x 72, 128M x 64 and One rank 64M x 72, 64M x 64, 32M x 64 organization
- 2.6V ± 0.1V VDD and VDDQ Power supply for DDR400, 2.5V ± 0.2V for DDR333 and below
- All inputs and outputs are compatible with SSTL\_2 interface
- Fully differential clock operations (CK & /CK) with 133/166/200MHz
- DLL aligns DQ and DQS transition with CK transition
- Programmable CAS Latency: DDR266(2, 2.5 clock), DDR333(2.5 clock), DDR400(3 clock)
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Edge-aligned DQS with data outs and Center-aligned DQS with data inputs
- Auto refresh and self refresh supported
- 8192 refresh cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- Built with 512Mb DDR SDRAMs in 400 mil TSOP II packages
- Lead-free product listed for each configuration (RoHS compliant)

### ADDRESS TABLE

	Organization	Ranks	SDRAMs	# of DRAMs	# of row/bank/column Address	Refresh Method
<b>256MB</b>	32M x 64	1	32Mb x 16	4	13(A0~A12)/2(BA0,BA1)/10(A0~A9)	8K / 64ms
<b>512MB</b>	64M x 64	1	64Mb x 8	8	13(A0~A12)/2(BA0,BA1)/11(A0~A9,A11)	8K / 64ms
<b>512MB</b>	64M x 72	1	64Mb x 8	9	13(A0~A12)/2(BA0,BA1)/11(A0~A9,A11)	8K / 64ms
<b>1GB</b>	128M x 64	2	128Mb x 8	16	13(A0~A12)/2(BA0,BA1)/11(A0~A9,A11)	8K / 64ms
<b>1GB</b>	128M x 72	2	128Mb x 8	18	13(A0~A12)/2(BA0,BA1)/11(A0~A9,A11)	8K / 64ms

### PERFORMANCE RANGE

Part-Number Suffix	-D43 <sup>1</sup>	-J	-H	Unit
<b>Speed Bin</b>	DDR400B	DDR333	DDR266B	-
<b>CL - tRCD - tRP</b>	3-3-3	2.5-3-3	2.5-3-3	CK
<b>Max Clock Frequency</b>	<b>CL=3</b>	200	-	MHz
	<b>CL=2.5</b>	166	166	MHz
	<b>CL=2</b>	133	133	MHz

**Note:**

1. 2.6V ± 0.1V VDD and VDDQ Power supply for DDR400 and 2.5V ± 0.2V for DDR333 and below

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**ORDERING INFORMATION**

Part Number	Density	Organization	# of DRAMs	Material	DIMM Dimension	ECC Support
HYMD532646B6-H	256MB	32Mb x 16	4	Normal	133.35 x 31.75 x 3.18 [mm <sup>3</sup> ]	None
HYMD532646BP6-H	256MB	32Mb x 16	4	Lead-free <sup>1</sup>	↑	None
HYMD532646B6J-D43/J	256MB	32Mb x 16	4	Normal	↑	None
HYMD532646BP6J-D43/J	256MB	32Mb x 16	4	Lead-free <sup>1</sup>	↑	None
HYMD564646B8-H	512MB	64Mb x 8	8	Normal	↑	None
HYMD564646BP8-H	512MB	64Mb x 8	8	Lead-free <sup>1</sup>	↑	None
HYMD564646B8J-D43/J	512MB	64Mb x 8	8	Normal	↑	None
HYMD564646BP8J-D43/J	512MB	64Mb x 8	8	Lead-free <sup>1</sup>	↑	None
HYMD564726B8-H	512MB	64Mb x 8	9	Normal	↑	ECC
HYMD564726BP8-H	512MB	64Mb x 8	9	Lead-free <sup>1</sup>	↑	ECC
HYMD564726B8J-D43/J	512MB	64Mb x 8	9	Normal	↑	ECC
HYMD564726BP8J-D43/J	512MB	64Mb x 8	9	Lead-free <sup>1</sup>	↑	ECC
HYMD512646B8-H	1GB	128Mb x 8	16	Normal	133.35 x 31.75 x 4 [mm <sup>3</sup> ]	None
HYMD512646BP8-H	1GB	128Mb x 8	16	Lead-free <sup>1</sup>	↑	None
HYMD512646B8J-D43/J	1GB	128Mb x 8	16	Normal	↑	None
HYMD512646BP8J-D43/J	1GB	128Mb x 8	16	Lead-free <sup>1</sup>	↑	None
HYMD512726B8-H	1GB	128Mb x 8	18	Normal	↑	ECC
HYMD512726BP8-H	1GB	128Mb x 8	18	Lead-free <sup>1</sup>	↑	ECC
HYMD512726B8J-D43/J	1GB	128Mb x 8	18	Normal	↑	ECC
HYMD512726BP8J-D43/J	1GB	128Mb x 8	18	Lead-free <sup>1</sup>	↑	ECC

**Note:**

1. The "Lead-free" products contain Lead less than 0.1% by weight and satisfy RoHS - please contact Hynix for product availability.

\* These products are built with HY5DU124(8,16)22BT[P], the Hynix DDR SDRAM component.

**PIN DESCRIPTION**

Pin	Pin Description	Pin	Pin Description
CK0~2, /CK0~2	Differential Clock Inputs	VDD	Power Supply for Core and I/O
/CS0, /CS1	Chip Select Inputs	VDDQ	Power Supply for DQs
CKE0, CKE1	Clock Enable Inputs	VSS	Ground
/RAS, /CAS, /WE	Command Sets Inputs	VREF	Input/Output Reference
A0 ~ A13	Address Inputs	VDDSPD	Power Supply for SPD
A10/AP	Address Input/Autoprecharge	VDDID	VDD, VDDQ Level Detection
BA0, BA1	Bank Address	SA0~SA2	SPD Address Inputs
DQ0~DQ63	Data Inputs/Outputs	SCL	SPD Clock Input
CB0~CB7	Data Check bits	SDA	SPD Data Input/Output
DQS0~DQS8	Data Strobes	DU	Do not Use
DM0~8	Data-in Masks	NC	No Connect
		TEST	Reserved for test equipment use

**PIN ASSIGNMENT**

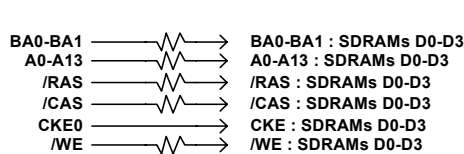
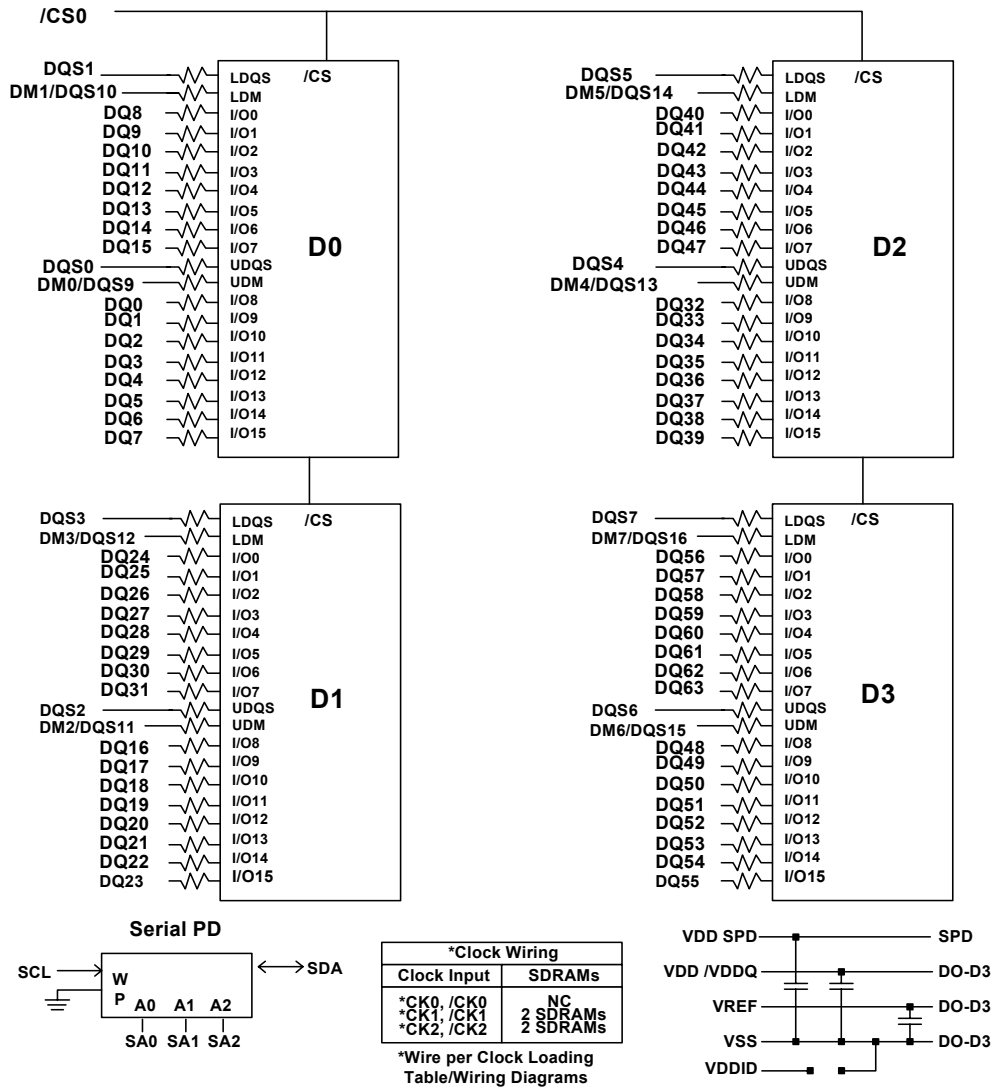
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0,DQS9	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3,DQS12	159	DM5,DQS14
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	NC,/CS2	102	NC,TEST	133	DQ31	163	NC,/CS3
11	VSS	42	VSS	72	DQ48	103	NC,FETEN	134	CB4,NC	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5,NC	165	DQ52
13	DQ9	44	CB0,NC	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1,NC	75	/CK2	106	DQ13	137	CK0	167	NC,A13
15	VDDQ	46	VDD	76	CK2	107	DM1,DQS10	138	/CK0	168	VDD
16	CK1	47	NC,DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK1	48	A0	78	DQS6	109	DQ14	140	DM8,DQS17	170	DQ54
18	VSS	49	CB2,NC	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6,NC	172	VDDQ
20	DQ11	51	CB3,NC	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2	144	CB7,NC	174	DQ60
22	VDDQ	Key		83	DQ56	114	DQ20	Key		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7,DQS16
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2,DQS11	149	DM4,DQS13	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

**note:**

1. Pins 44, 45, 47, 49, 51, 134, 135, 140, 142, 144 are reserved for x72 variants of this module and are not used on the x64 versions.
2. Pins 111, 158 are not used for single rank module.
3. Pin 167 is "NC" for 256MB, 512MB and 1GB or "A13" for 2GB module.
4. Pins 9, 10, 71, 82, 90, 101, 102, 103, 113, 163, 167, 173 are not used on this module.

## FUNCTIONAL BLOCK DIAGRAM

### 256MB, 32M x 64 Unbuffered DIMM: HYMD532646B[P]6[J]

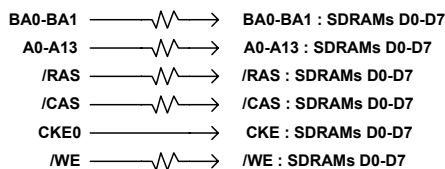
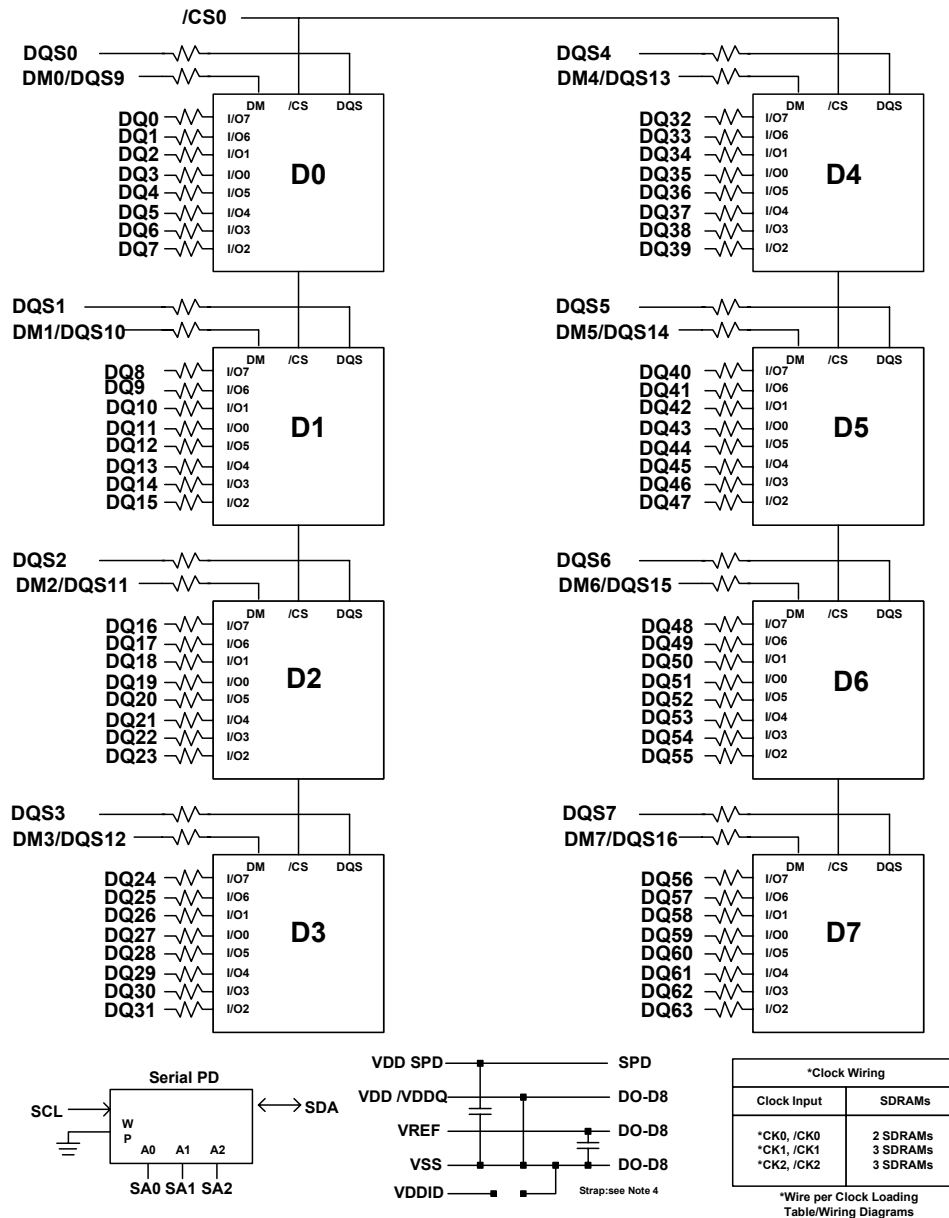


**Notes :**

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors : 22 Ohms +/- 5%.
4. VDDID strap connections  
(for memory device VDD, VDDQ):  
STRAP OUT (OPEN) : VDD = VDDQ  
STRAP IN (VSS) : VDD ≠ VDDQ
5. BAx, Ax, RAS, CAS, WE resistors : 7.5 Ohms +/- 5%

## FUNCTIONAL BLOCK DIAGRAM

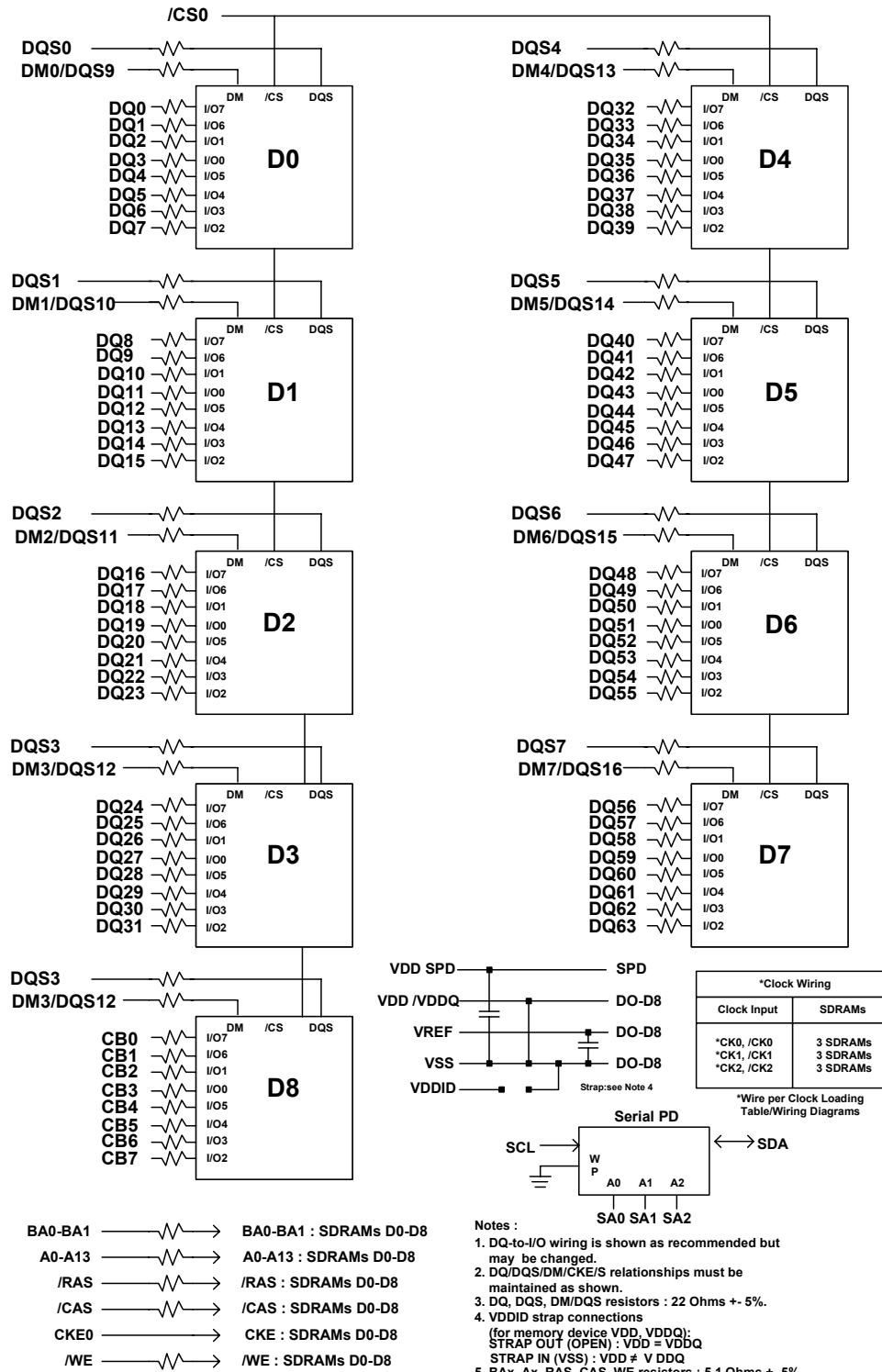
### 512MB, 64M x 64 Unbuffered DIMM: HYMD564646B[P]8[J]



- Notes :**
- DQ-to-I/O wiring is shown as recommended but may be changed.
  - DQ/DQS/DM/CKE/S relationships must be maintained as shown.
  - DQ, DQS, DM/DQS resistors : 22 Ohms +- 5%.
  - VDDID strap connections (for memory device VDD, VDDQ):  
 STRAP OUT (OPEN) : VDD = VDDQ  
 STRAP IN (VSS) : VDD ≠ VDDQ
  - BAX, Ax, RAS, CAS, WE resistors : 5.1 Ohms +- 5%

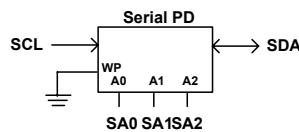
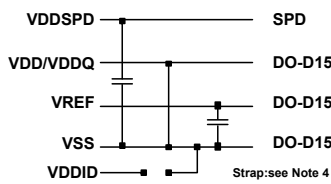
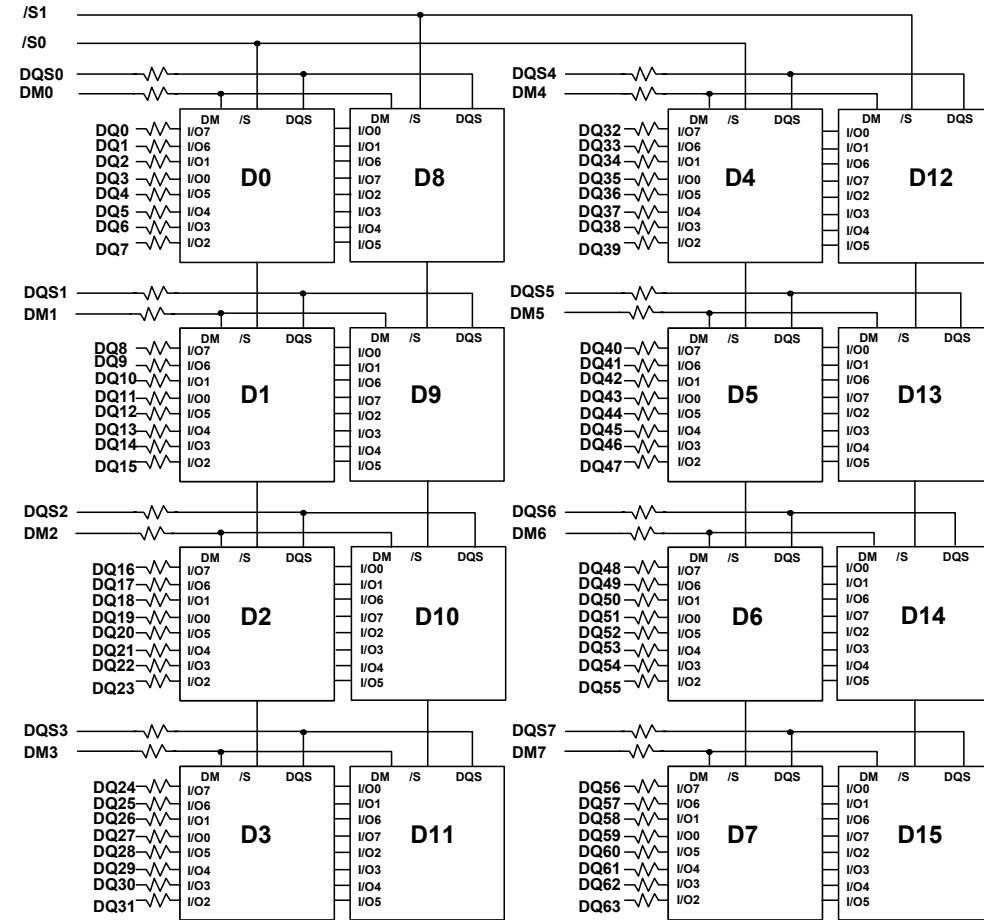
## FUNCTIONAL BLOCK DIAGRAM

### 512MB, 64M x 72 ECC Unbuffered DIMM : HYMD564726B[P]8[J]



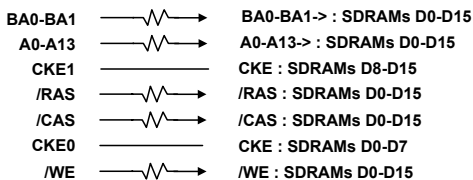
## FUNCTIONAL BLOCK DIAGRAM

1GB, 128M x 64 Unbuffered DIMM : HYMD512646B[P]8[J]



* Clock Wiring	
Clock Input	SDRAMs
*CK0./CK0	4 SDRAMs
*CK1./CK1	6 SDRAMs
*CK2./CK2	6 SDRAMs

\* Wire per Clock Loading Table/Wiring Diagrams

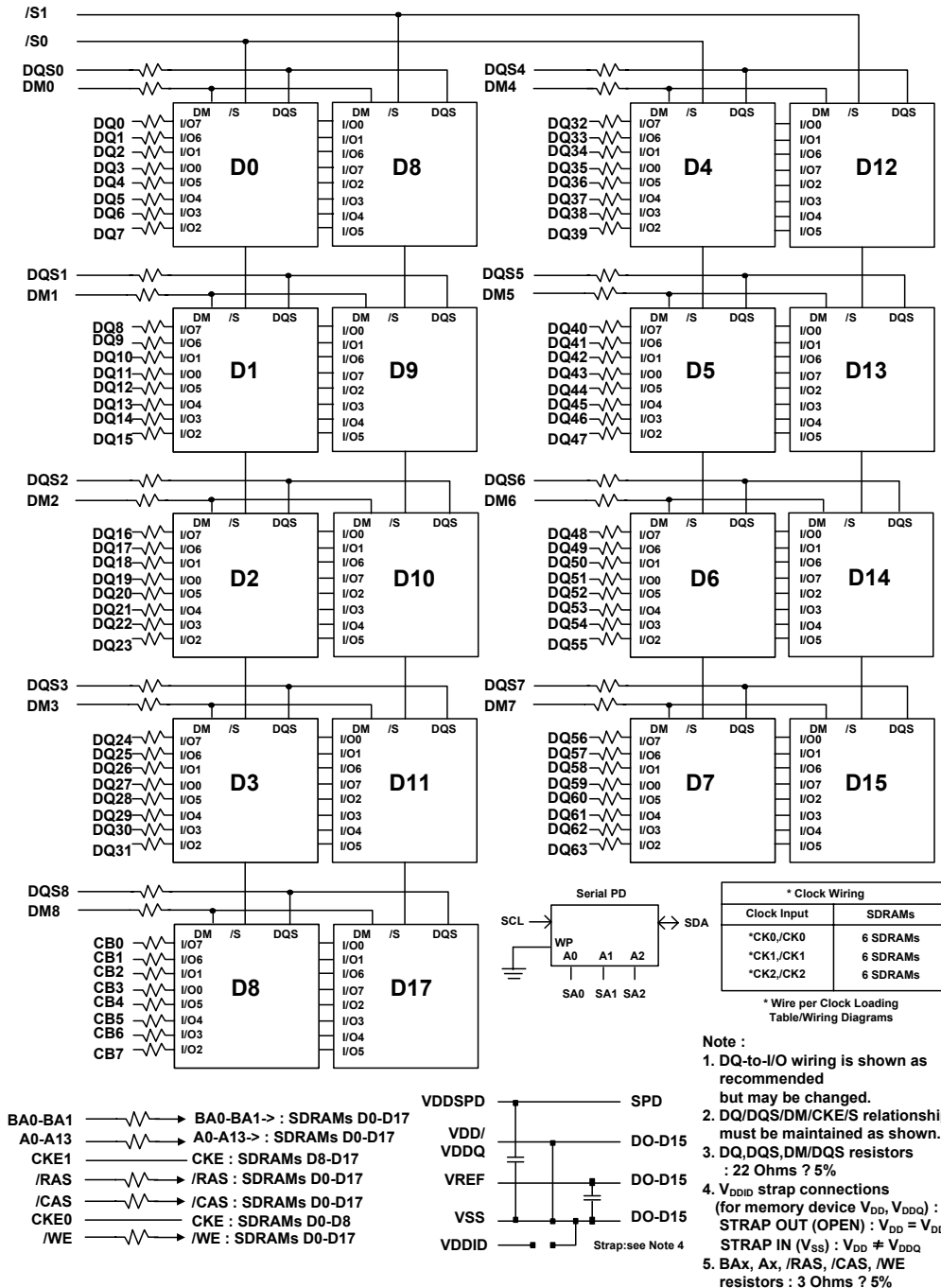


**Note :**

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ,DQS,DM/DQS resistors : 22 Ohms ? 5%
4. V<sub>DDID</sub> strap connections (for memory device V<sub>DD</sub>, V<sub>DDQ</sub>) :  
STRAP OUT (OPEN) : V<sub>DD</sub> = V<sub>DDQ</sub>  
STRAP IN (V<sub>SS</sub>) : V<sub>DD</sub> ≠ V<sub>DDQ</sub>
5. BA<sub>x</sub>, A<sub>x</sub>, /RAS, /CAS, /WE resistors : 3 Ohms ? 5%

## FUNCTIONAL BLOCK DIAGRAM

### 1GB, 128M x 72 ECC Unbuffered DIMM : HYMD512726B[P]8[J]





**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Parameter	Symbol	Rating	Unit
Operating Temperature (Ambient)	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 150	°C
Voltage on VDD relative to VSS	VDD	-1.0 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-1.0 ~ 3.6	V
Voltage on inputs relative to Vss	VINPUT	-1.0 ~ 3.6	V
Voltage on I/O pins relative to Vss	VIO	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

**Note:**

1. Operation at above absolute maximum rating can adversely affect device reliability

**DC OPERATING CONDITIONS** (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note	
Power Supply Voltage (DDR 200, 266, 333)	VDD	2.3	2.5	2.7	V		
Power Supply Voltage (DDR 400)	VDD	2.5	2.6	2.7	V	2	
Power Supply Voltage (DDR 200, 266, 333)	VDDQ	2.3	2.5	2.7	V	1	
Power Supply Voltage (DDR 400)	VDDQ	2.5	2.6	2.7	V	1,2	
Input High Voltage	VIH	VREF + 0.15	-	VDDQ + 0.3	V		
Input Low Voltage	VIL	-0.3	-	VREF - 0.15	V	3	
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V		
Reference Voltage	VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V	4	
Input Voltage Level, CK and CK inputs	VIN(DC)	-0.3	-	VDDQ+0.3	V		
Input Differential Voltage, CK and CK inputs	VID(DC)	0.36	-	VDDQ+0.6	V	5	
V-I Matching: Pullup to Pulldown Current Ratio	VI(RATIO)	0.71	-	1.4	-	6	
Input Leakage Current	ILI	-2	-	2	uA	7	
Output Leakage Current	ILO	-5	-	5	uA	8	
Normal Strength Output Driver (VOUT=VTT ± 0.84)	Output High Current (min VDDQ, min VREF, min VTT)	IOH	-16.8	-	-	mA	
	Output Low Current (min VDDQ, max VREF, max VTT)	IOL	16.8	-	-	mA	
Half Strength Output Driver (VOUT=VTT ± 0.68)	Output High Current (min VDDQ, min VREF, min VTT)	IOH	-13.6	-	-	mA	
	Output Low Current (min VDDQ, max VREF, max VTT)	IOL	13.6	-	-	mA	

**Note:**

1. VDDQ must not exceed the level of VDD.
2. For DDR400, VDD=2.6V ± 0.1V, VDDQ=2.6V ± 0.1V
3. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
4. VREF is expected to be equal to 0.5\*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak to peak noise on VREF may not exceed ± 2% of the DC value.
5. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
6. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.
7. VIN=0 to VDD, All other pins are not tested under VIN =0V.
8. DQs are disabled, VOUT=0 to VDDQ.

**IDD SPECIFICATION AND CONDITIONS** (TA=0 to 70°C, Voltage referenced to VSS = 0V)

**256MB, 32M x 64 Unbuffered DIMM: HYMD532646B[P]6[J]**

Symbol	Test Condition	Speed			Unit	Note	
		DDR400B	DDR333	DDR266B			
IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	600	560	480	mA		
IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	800	720	600	mA		
IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	40	40	40	mA		
IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	140	140	140	mA		
IDD3P	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	48	48	48	mA		
IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	200	180	160	mA		
IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOU=0mA	1120	1000	840	mA		
IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	1320	1120	1000	mA		
IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	1200	1120	1040	mA		
IDD6	CKE=<0.2V; External clock on; tCK =tCK(min)	Normal	20	20	20	mA	
		Low Power	10	10	10	mA	
IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	2160	1840	1520	mA		

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**IDD SPECIFICATION AND CONDITIONS** (TA=0 to 70°C, Voltage referenced to VSS = 0V)

**512MB, 64M x 64 Unbuffered DIMM: HYMD564646B[P]8[J]**

Symbol	Test Condition	Speed			Unit	Note	
		DDR400B	DDR333	DDR266B			
IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1200	1120	960	mA		
IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	1600	1440	1200	mA		
IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	80	80	80	mA		
IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	280	280	280	mA		
IDD3P	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	96	96	96	mA		
IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	400	360	320	mA		
IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOOUT=0mA	2240	2000	1680	mA		
IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	2240	2000	1680	mA		
IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	2400	2240	2080	mA		
IDD6	CKE=<0.2V; External clock on; tCK =tCK(min)	Normal	40	40	40	mA	
		Low Power	20	20	20	mA	
IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	4320	3680	3040	mA		

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**IDD SPECIFICATION AND CONDITIONS** (TA=0 to 70°C, Voltage referenced to VSS = 0V)

**512MB, 64M x 72 ECC Unbuffered DIMM: HYMD564726B[P]8[J]**

Symbol	Test Condition	Speed			Unit	Note	
		DDR400B	DDR333	DDR266B			
IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1350	1260	1080	mA		
IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	1800	1620	1350	mA		
IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	90	90	90	mA		
IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	315	315	315	mA		
IDD3P	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	108	108	108	mA		
IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Pre-charge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	450	105	360	mA		
IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	2520	2250	1890	mA		
IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	2520	2250	1890	mA		
IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	2700	2520	2340	mA		
IDD6	CKE=<0.2V; External clock on; tCK =tCK(min)	Normal	45	45	45	mA	
		Low Power	23	23	23	mA	
IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	4860	4140	3420	mA		

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**IDD SPECIFICATION AND CONDITIONS** (TA=0 to 70°C, Voltage referenced to VSS = 0V)

**1GB, 128M x 64 Unbuffered DIMM: HYMD512646B[P]8[J]**

Symbol	Test Condition	Speed			Unit	Note	
		DDR400B	DDR333	DDR266B			
IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1600	1480	1280	mA		
IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	2000	1800	1520	mA		
IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	160	160	160	mA		
IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	560	560	560	mA		
IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)	192	192	192	mA		
IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Pre-charge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	800	720	640	mA		
IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOOUT=0mA	2640	2360	2000	mA		
IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	2640	2360	2000	mA		
IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	2800	2600	2400	mA		
IDD6	CKE=<0.2V; External clock on; tCK =tCK(min)	Normal	80	80	80	mA	
		Low Power	40	40	40	mA	
IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	4720	4040	3360	mA		

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**IDD SPECIFICATION AND CONDITIONS** (TA=0 to 70°C, Voltage referenced to VSS = 0V)

**1GB, 128M x 72 ECC Unbuffered DIMM: HYMD512726B[P]8[J]**

Symbol	Test Condition	Speed			Unit	Note	
		DDR400B	DDR333	DDR266B			
IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1800	1665	1440	mA		
IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	2250	2025	1710	mA		
IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	180	180	180	mA		
IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	630	630	630	mA		
IDD3P	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	216	216	216	mA		
IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Pre-charge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	900	810	720	mA		
IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	2970	2655	2250	mA		
IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	2970	2655	2250	mA		
IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	3150	2925	2700	mA		
IDD6	CKE=<0.2V; External clock on; tCK =tCK(min)	Normal	90	90	90	mA	
		Low Power	45	45	45	mA	
IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	5310	4545	3780	mA		

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V <sub>IH(AC)</sub>	V <sub>REF</sub> + 0.31	-	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	V <sub>IL(AC)</sub>	-	V <sub>REF</sub> - 0.31	V	
Input Differential Voltage, CK and /CK inputs	V <sub>ID(AC)</sub>	0.7	V <sub>DDQ</sub> + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	V <sub>IX(AC)</sub>	0.5*V <sub>DDQ</sub> -0.2	0.5*V <sub>DDQ</sub> +0.2	V	2

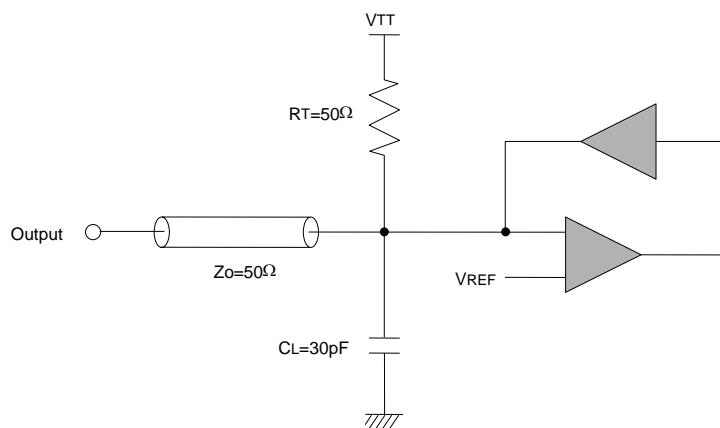
**Note:**

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5\*V DDQ of the transmitting device and must track variations in the DC level of the same.

## AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	V <sub>DDQ</sub> x 0.5	V
Termination Voltage	V <sub>DDQ</sub> x 0.5	V
AC Input High Level Voltage (V <sub>IH</sub> , min)	V <sub>REF</sub> + 0.31	V
AC Input Low Level Voltage (V <sub>IL</sub> , max)	V <sub>REF</sub> - 0.31	V
Input Timing Measurement Reference Level Voltage	V <sub>REF</sub>	V
Output Timing Measurement Reference Level Voltage	V <sub>TT</sub>	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

## OUTPUT LOAD CIRCUIT



**CAPACITANCE** (TA=25°C, f=100MHz)

**256MB: HYMD532646B[P]6[J]**

Input/Output Pins	Symbol	Min	Max	Unit
A0 ~ A12, BA0, BA1	CIN1	40	52	pF
/RAS, /CAS, /WE	CIN2	40	52	pF
CKE	CIN3	40	52	pF
/CS	CIN4	40	52	pF
CK0, /CK0, CK1, /CK1, CK2, /CK2	CIN5	22	32	pF
DM0 ~ DM7	CIN6	7	12	pF
DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	7	12	pF

**512MB: HYMD564646B[P]8[J]**

Input/Output Pins	Symbol	Min	Max	Unit
A0 ~ A12, BA0, BA1	CIN1	58	71	pF
/RAS, /CAS, /WE	CIN2	58	71	pF
CKE	CIN3	58	72	pF
/CS	CIN4	58	72	pF
CK0, /CK0, CK1, /CK1, CK2, /CK2	CIN5	25	40	pF
DM0 ~ DM7	CIN6	7	12	pF
DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	7	12	pF

**512MB (with ECC): HYMD564726B[P]8[J]**

Input/Output Pins	Symbol	Min	Max	Unit
A0 ~ A12, BA0, BA1	CIN1	60	75	pF
/RAS, /CAS, /WE	CIN2	60	75	pF
CKE	CIN3	60	75	pF
/CS	CIN4	60	75	pF
CK0, /CK0, CK1, /CK1, CK2, /CK2	CIN5	27	45	pF
DM0 ~ DM7	CIN6	7	12	pF
DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	7	12	pF
CB0 ~ CB7	CIO2	7	12	pF



**CAPACITANCE** ( $T_A=25^{\circ}\text{C}$ ,  $f=100\text{MHz}$ )

**1GB: HYMD512646B[P]8[J]**

Input/Output Pins	Symbol	Min	Max	Unit
A0 ~ A12, BA0, BA1	CIN1	90	104	pF
/RAS, /CAS, /WE	CIN2	90	104	pF
CKE0, CKE1	CIN3	58	72	pF
/CS0, /CS1	CIN4	58	72	pF
CK0, /CK0, CK1, /CK1, CK2, /CK2	CIN5	30	45	pF
DM0 ~ DM7	CIN6	12	18	pF
DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	12	18	pF

**1GB (with ECC): HYMD512726B[P]8[J]**

Input/Output Pins	Symbol	Min	Max	Unit
A0 ~ A12, BA0, BA1	CIN1	95	110	pF
/RAS, /CAS, /WE	CIN2	95	110	pF
CKE0, CKE1	CIN3	60	80	pF
/CS0, /CS1	CIN4	60	80	pF
CK0, /CK0, CK1, /CK1, CK2, /CK2	CIN5	32	45	pF
DM0 ~ DM7	CIN6	12	18	pF
DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	12	18	pF
CB0 ~ CB7	CIO2	12	18	pF

**AC CHARACTERISTICS** (note: 1 - 9 / AC operating conditions unless otherwise noted)

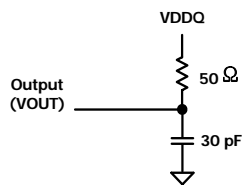
Parameter	Symbol	DDR400B		DDR333		DDR266A		DDR266B		DDR200		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Row Cycle Time	tRC	55	-	60	-	65	-	65	-	70	-	ns
Auto Refresh Row Cycle Time	tRFC	70	-	72	-	75	-	75	-	80	-	ns
Row Active Time	tRAS	40	70K	42	70K	45	120K	45	120K	50	120K	ns
Active to Read with Auto Precharge Delay	tRAP	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	ns
Row Address to Column Address Delay	tRCD	15	-	18	-	20	-	20	-	20	-	ns
Row Active to Row Active Delay	tRRD	10	-	12	-	15	-	15	-	15	-	ns
Column Address to Column Address Delay	tCCD	1	-	1	-	1	-	1	-	1	-	tCK
Row Precharge Time	tRP	15	-	18	-	20	-	20	-	20	-	ns
Write Recovery Time	tWR	15	-	15	-	15	-	15	-	15	-	ns
Internal Write to Read Command Delay	tWTR	2	-	1	-	1	-	1	-	1	-	tCK
Auto Precharge Write Recovery + Precharge Time <sup>22</sup>	tDAL	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	tCK
System Clock Cycle Time <sup>24</sup>	CL = 3	5	10	-	-	-	-	-	-	-	-	
	CL = 2.5	-	-	6	12	7.5	12	7.5	12	8.0	12	ns
	CL = 2	-	-	7.5	12	7.5	12	10	12	10	12	ns
Clock High Level Width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Clock Low Level Width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Data-Out edge to Clock edge Skew	tAC	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.75	0.75	ns
DQS-Out edge to Clock edge Skew	tDQSK	-0.55	0.55	-0.6	0.6	-0.75	0.75	-0.75	0.75	-0.75	0.75	ns
DQS-Out edge to Data-Out edge Skew <sup>21</sup>	tDQSQ	-	0.4	-	0.45	-	0.5	-	0.5	-	0.6	ns
Data-Out hold time from DQS <sup>20</sup>	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns
Clock Half Period <sup>19,20</sup>	tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	ns
Data Hold Skew Factor <sup>20</sup>	tQHS	-	0.5	-	0.55	-	0.75	-	0.75	-	0.75	ns
Valid Data Output Window	tDV	tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		ns

*- Continue*

Parameter	Symbol	DDR400B		DDR333		DDR266A		DDR266B		DDR200		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Data-out high-impedance window from CK, <sub>0</sub> /CK <sup>10</sup>	tHZ	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns
Data-out low-impedance window from CK, /CK <sup>10</sup>	tLZ	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns
Input Setup Time (fast slew rate) <sup>14,16-18</sup>	tIS	0.6	-	0.75	-	0.9	-	0.9	-	1.1	-	ns
Input Hold Time (fast slew rate) <sup>14,16-18</sup>	tIH	0.6	-	0.75	-	0.9	-	0.9	-	1.1	-	ns
Input Setup Time (slow slew rate) <sup>15-18</sup>	tIS	0.7	-	0.8	-	1.0	-	1.0	-	1.1	-	ns
Input Hold Time (slow slew rate) <sup>15-18</sup>	tIH	0.7	-	0.8	-	1.0	-	1.0	-	1.1	-	ns
Input Pulse Width <sup>17</sup>	tIPW	2.2	-	2.2	-	2.2	-	2.2	-	2.5	-	ns
Write DQS High Level Width	tDQSH	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	tCK
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	tCK
Clock to First Rising edge of DQS-In	tDQSS	0.72	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK
DQ & DM input setup time <sup>25</sup>	tDS	0.4	-	0.45	-	0.5	-	0.5	-	0.6	-	ns
DQ & DM input hold time <sup>25</sup>	tDH	0.4	-	0.45	-	0.5	-	0.5	-	0.6	-	ns
DQ & DM Input Pulse Width <sup>17</sup>	tDIPW	1.75	-	1.75	-	1.75	-	1.75	-	2	-	ns
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write DQS Preamble Setup Time <sup>12</sup>	tWPRES	0	-	0	-	0	-	0	-	0	-	ns
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	tCK
Write DQS Postamble Time <sup>11</sup>	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Mode Register Set Delay	tMRD	2	-	2	-	2	-	2	-	2	-	tCK
Exit Self Refresh to non-Read command <sup>23</sup>	tXSNR	75	-	75	-	75	-	75	-	80	-	ns
Exit Self Refresh to Read command	tXSRD	200	-	200	-	200	-	200	-	200	-	tCK
Average Periodic Refresh Interval <sup>13,25</sup>	tREFI	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us

**Note:**

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Below figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).



**Figure: Timing Reference Load**

4. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK, /CK), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL\_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE  $\leq 0.2VDDQ$  is recognized as LOW.
7. The CK, /CK input reference level (for timing referenced to CK, /CK) is the point at which CK and /CK cross; the input reference level for signals other than CK, /CK is VREF.
8. The output timing reference voltage level is VTT.
9. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
10. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
11. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
12. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
13. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
14. For command/address input slew rate  $\geq 1.0$  V/ns.
15. For command/address input slew rate  $\geq 0.5$  V/ns and  $< 1.0$  V/ns
16. For CK & /CK slew rate  $\geq 1.0$  V/ns (single-ended)
17. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
18. Slew Rate is measured between VOH(ac) and VOL(ac).
19. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).  
For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

20.  $t_{QH} = t_{HP} - t_{QHS}$ , where:

$t_{HP}$  = minimum half clock period for any given cycle and is defined by clock high or clock low ( $t_{CH}$ ,  $t_{CL}$ ).  $t_{QHS}$  accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push--out of DQS on one transition followed by the worst case pull--in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

21.  $t_{DQSQ}$ :

Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

22.  $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$

For each of the terms above, if not already an integer, round to the next highest integer.

Example: For DDR266B at CL=2.5 and  $t_{CK}=7.5$  ns

$t_{DAL} = ((15 \text{ ns} / 7.5 \text{ ns}) + (20 \text{ ns} / 7.5 \text{ ns}))$  clocks

= ((2) + (3)) clocks

= 5 clocks

23. In all circumstances,  $t_{XSNR}$  can be satisfied using

$t_{XSNR} = t_{RFCmin} + 1 * t_{CK}$

24. The only time that the clock frequency is allowed to change is during self-refresh mode.

25. If refresh timing or  $t_{DS}/t_{DH}$  is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

**SYSTEM CHARACTERISTICS CONDITIONS for DDR SDRAMS**

The following tables are described specification parameters that required in systems using DDR devices to ensure proper performance. These characteristics are for system simulation purposes and are guaranteed by design.

**Input Slew Rate for DQ/DM/DQS (Table a.)**

AC CHARACTERISTICS		DDR400		DDR333		DDR266		DDR200		UNIT	Note
PARAMETER	Symbol	min	max	min	max	min	max	min	max		
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	V/ns	1,12

**Address & Control Input Setup & Hold Time Derating (Table b.)**

Input Slew Rate	Delta tIS	Delta tIH	UNIT	Note
0.5 V/ns	0	0	ps	9
0.4 V/ns	+50	0	ps	9
0.3 V/ns	+100	0	ps	9

**DQ & DM Input Setup & Hold Time Derating (Table c.)**

Input Slew Rate	Delta tDS	Delta tDH	UNIT	Note
0.5 V/ns	0	0	ps	11
0.4 V/ns	+75	0	ps	11
0.3 V/ns	+150	0	ps	11

**DQ & DM Input Setup & Hold Time Derating for Rise/Fall Delta Slew Rate (Table d.)**

Input Slew Rate	Delta tDS	Delta tDH	UNIT	Note
± 0.0 ns/V	0	0	ps	10
± 0.25 ns/V	+50	+50	ps	10
± 0.5 ns/V	+100	+100	ps	10

**Output Slew Rate Characteristics (for x4, x8 Devices) (Table e.)**

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Note
Pullup Slew Rate	1.2 - 2.5	1.0	4.5	1,3,4,6,7,8
Pulldown Slew Rate	1.2 - 2.5	1.0	4.5	2,3,4,6,7,8

**Output Slew Rate Characteristics (for x16 Device) (Table f.)**

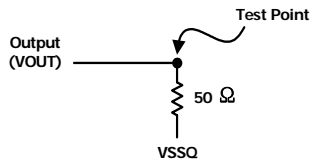
Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Note
Pullup Slew Rate	1.2 - 2.5	1.0	4.5	1,3,4,6,7,8
Pulldown Slew Rate	1.2 - 2.5	1.0	4.5	2,3,4,6,7,8

**Output Slew Rate Matching Ratio Characteristics (Table g.)**

Slew Rate Characteristic	DDR266A		DDR266B		DDR200		Note
	min	max	min	max	min	max	
Output Slew Rate Matching Ratio (Pullup to Pulldown)	-	-	-	-	0.71	1.4	5,12

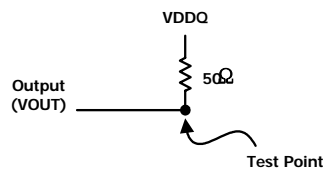
**Note:**

1. Pullup slew rate is characterized under the test conditions as shown in below Figure.



**Figure: Pullup Slew rate**

2. Pulldown slew rate is measured under the test conditions shown in below Figure.



**Figure: Pulldown Slew rate**

3. Pullup slew rate is measured between  $(VDDQ/2 - 320\text{ mV} \pm 250\text{mV})$   
 Pulldown slew rate is measured between  $(VDDQ/2 + 320\text{mV} \pm 250\text{mV})$   
 Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example: For typical slew, DQ0 is switching

For minimum slew rate, all DQ bits are switching worst case pattern

For maximum slew rate, only one DQ is switching from either high to low, or low to high.

The remaining DQ bits remain the same as for previous state.

4. Evaluation conditions

Typical: 25 °C (Ambient), VDDQ = nominal, typical process

Minimum: 70 °C (Ambient), VDDQ = minimum, slow-slow process

Maximum: 0 °C (Ambient), VDDQ = Maximum, fast-fast process

5. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.
6. Verified under typical conditions for qualification purposes.
7. TSOP-II package devices only.
8. Only intended for operation up to 256 Mbps per pin.
9. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns as shown in Table b.  
 The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
10. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables c & d. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. The delta rise/fall rate is calculated as:  
 $\{1/(\text{Slew Rate1})\} - \{1/(\text{slew Rate2})\}$   
 For example:  
 If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is -0.5 ns/V. Using the table given, this would result in the need for an increase in tDS and tDH of 100ps.
11. Table c is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC-AC slew rate and the DC-DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(AC) or VIH(DC) to VIL(DC), and similarly for rising transitions.
12. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

**SIMPLIFIED COMMAND TRUTH TABLE**

Command	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	A10/AP	BA	Note
Extended Mode Register Set	H	X	L	L	L	L	OP code			1,2
Mode Register Set	H	X	L	L	L	L	OP code			1,2
Device Deselect	H	X	H	X	X	X	X			1
No Operation			L	H	H	H				
Bank Active	H	X	L	L	H	H	RA		V	1
Read	H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge								H		1,3
Write	H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge								H		1,4
Precharge All Banks	H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank								L	V	1
Read Burst Stop	H	X	L	H	H	L	X		1	
Auto Refresh	H	H	L	L	L	H	X		1	
Self Refresh	Entry	H	L	L	L	L	H	X		1
	Exit	L	H	H	X	X	X			1
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X		1
				L	H	H	H			1
	Exit	L	H	H	X	X	X			1
				L	H	H	H			1
Active Power Down Mode	Entry	H	L	H	X	X	X	X		1
				L	V	V	V			1
	Exit	L	H	X			1			

**Note :**

1. DM is the signal in the Data Mask Command. Valid Data Input, OP Code=Operand Code, NOP=No Operation )
2. OP Code(Operand Code) consists of A0~A12 and BA0~BA1 used for Mode Registering during Extended MRS or MRS.  
Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Precharge command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tWR+tRP). Write Recovery Time(tWR) is needed to guarantee that the last data has been completely written.
5. If A10/AP is High when Row Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

**WRITE MASK TRUTH TABLE**

Function	CKEn-1	CKEn	/CS, /RAS, /CAS, /WE	DM	ADDR	A10/AP	BA	Note
Data Write	H	X	X	L		X		1
Data-In Mask	H	X	X	H		X		1

**Note:**

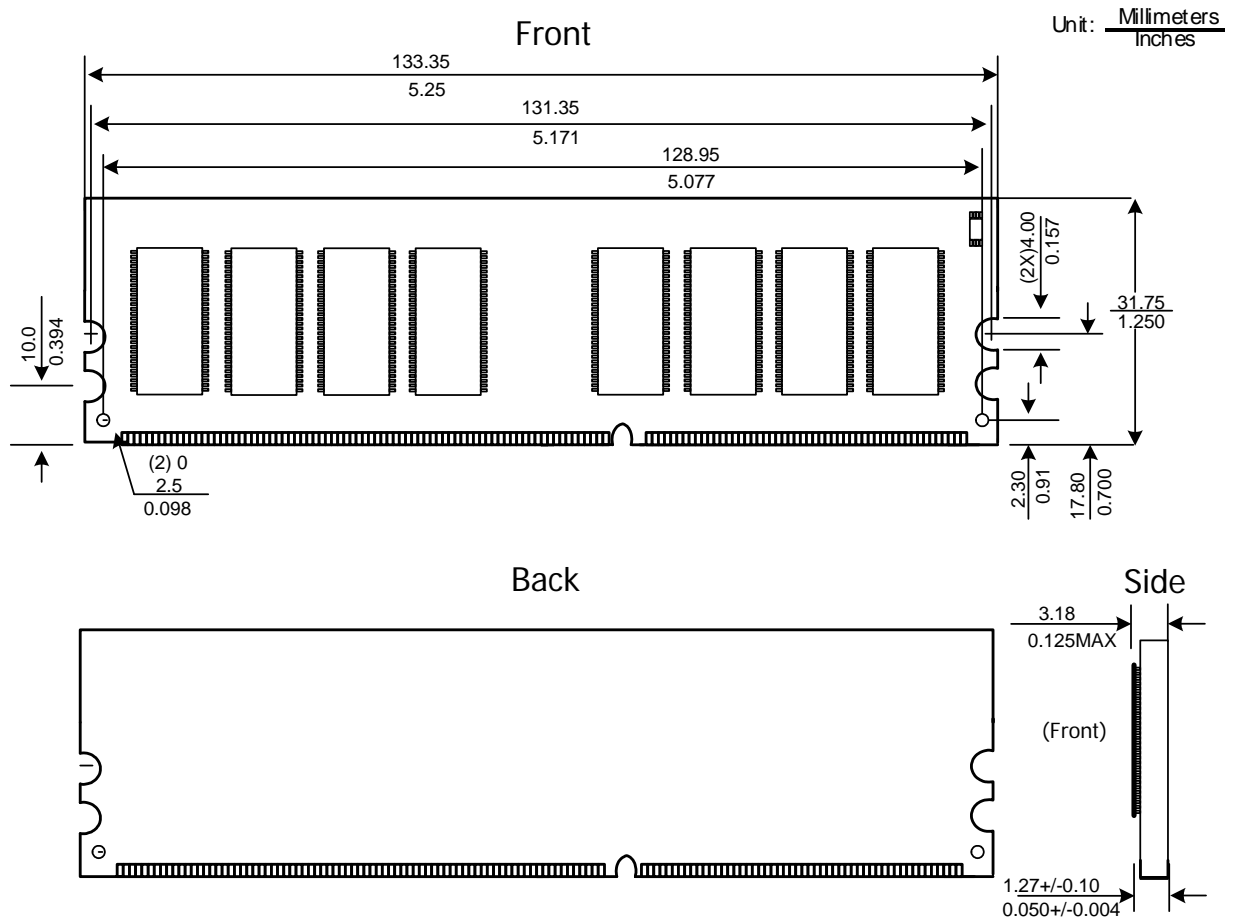
1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Stobes) and it is not related with read data.  
In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.





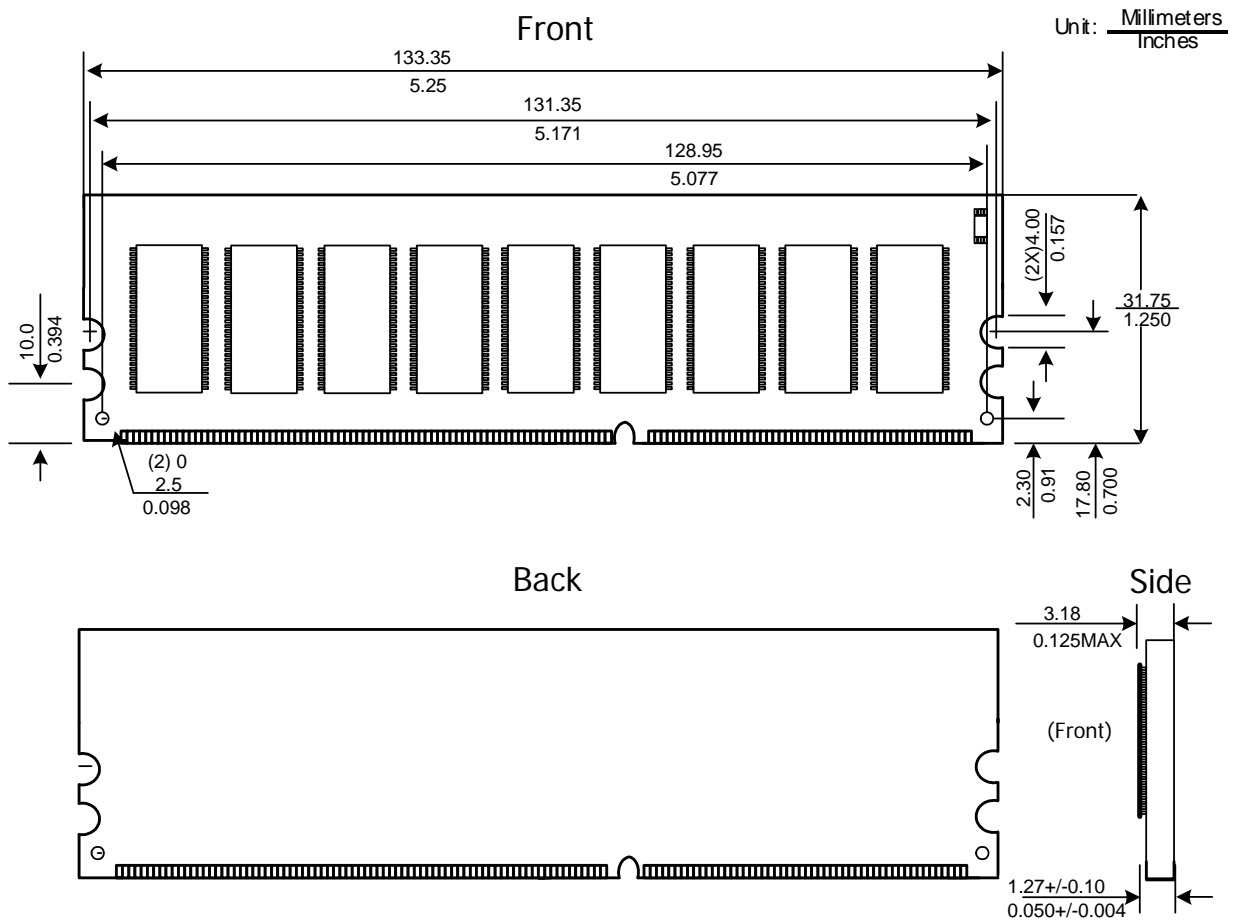
PACKAGE DIMENSIONS

512MB, 64M x 64 Unbuffered DIMM: HYMD564646B[P]8[J]



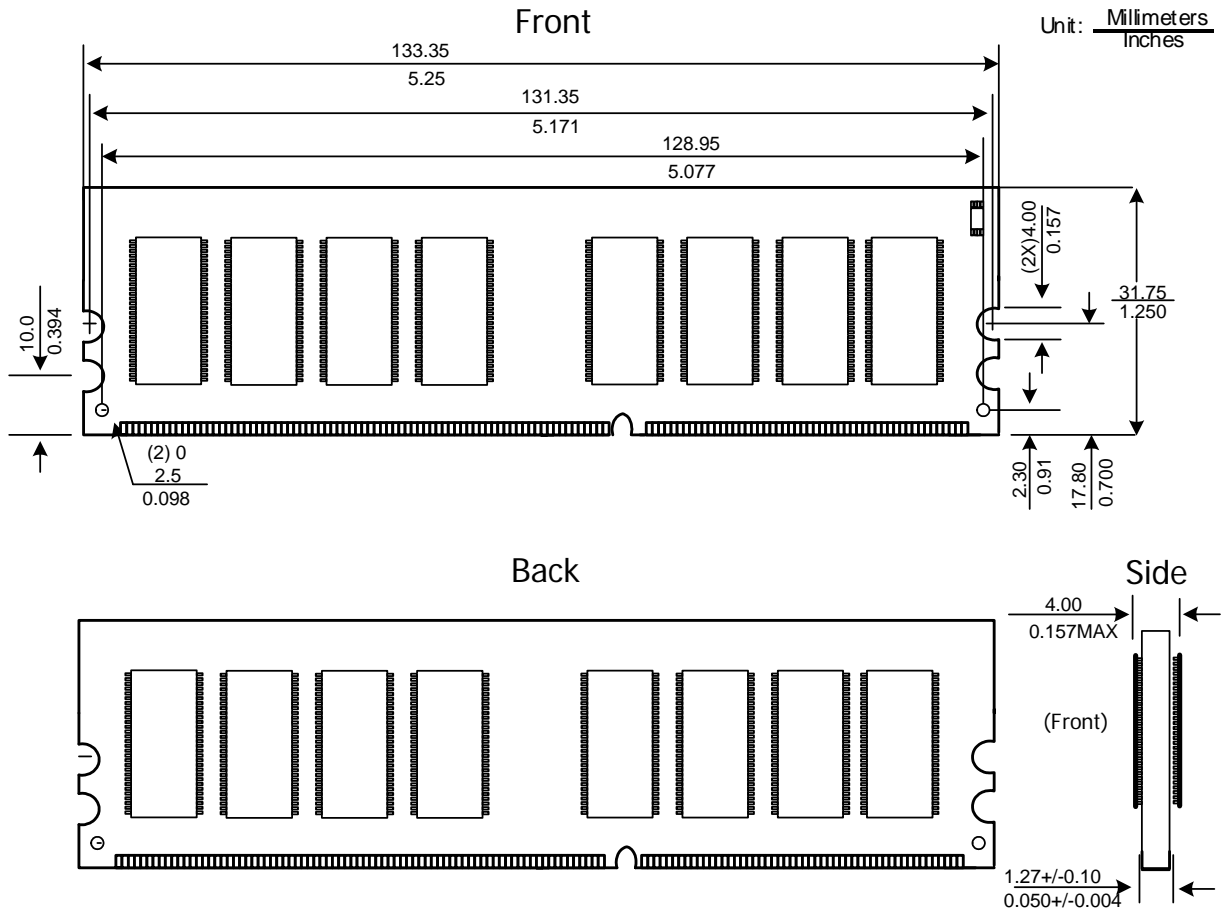
PACKAGE DIMENSIONS

512MB, 64M x 72 ECC Unbuffered DIMM: HYMD564726B[P]8[J]



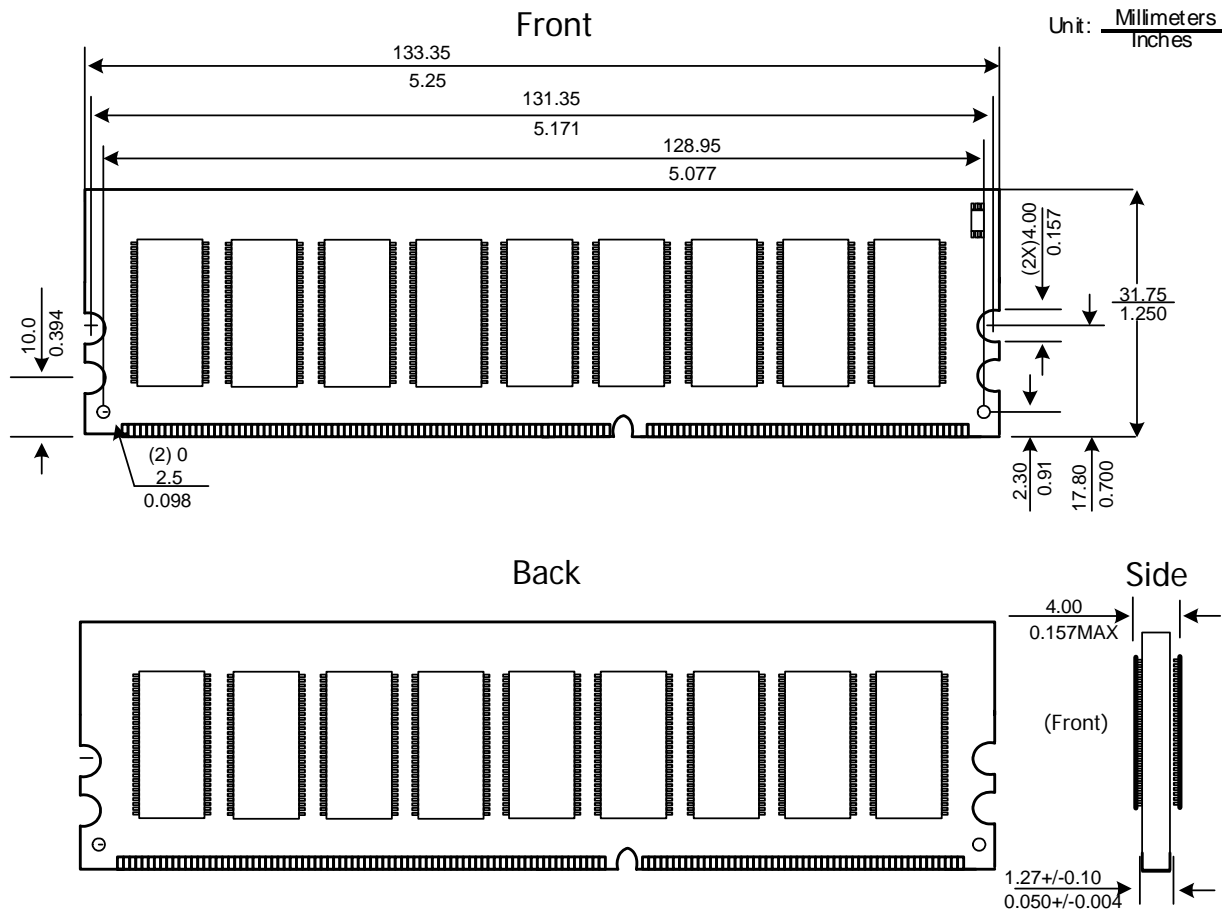
PACKAGE DIMENSIONS

1GB, 128M x 64 Unbuffered DIMM : HYMD56464B[P]8[J]



PACKAGE DIMENSIONS

1GB, 128M x 72 ECC Unbuffered DIMM: HYMD512726B[P]8[J]



**REVISION HISTORY**

Revision	History	Date	Remark
1.0	First Version Release - Datasheet coverage is changed from an individual module part to a component based module family	Feb. 2005	
1.1	Corrected PIN DESCRIPTION and PIN ASSIGNMENT Tables	May. 2005	