16 Mbit (x16/x8) Concurrent SuperFlash Memory

SST34HF1601B

Preliminary Specifications

FEATURES:

- **Organized as 1M x16 or 2M x8**
- **Dual Bank Architecture for Concurrent Read/Write Operation**
  - Bank1: 12 Mbit (768K x16/1536K x8) Flash
  - Bank2: 4 Mbit (256K x16/512K x8) Flash
- **Single 2.7-3.3V for Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 6 mA typical
  - Standby Current: 4 µA typical
- **Hardware Sector Protection/WP# Input Pin**
  - Protects 4 outermost blocks in the smaller bank (128 KWord/256 KByte)
- **Hardware Reset Pin (RST#)**
- **Sector-Erase Capability**
  - Uniform 1 KWord/2 KByte sectors
- **Block-Erase Capability**
  - Uniform 32 KWord/64 KByte blocks
- **Fast Read Access Time**
  - 80 ns
- **Latched Address and Data**
- **Fast Erase and Word-Program (typical):**
  - Sector-Erase Time: 18 ms
  - Block-Erase Time: 18 ms
  - Chip-Erase Time: 70 ms
  - Word-Program Time: 14 µs
  - Byte-Program Time: 14 µs
  - Chip Rewrite Time: 8 seconds (Word mode)
  - Chip Rewrite Time: 16 seconds (Byte mode)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
  - Ready/Busy# pin
- **CMOS I/O Compatibility**
- **JEDEC Standards**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 48-lead TSOP (12mm x 20mm)
  - 56-ball TFBGA (8mm x 10mm)

PRODUCT DESCRIPTION

The SST34HF1601B consists of two memory banks, Bank1 is 256K x16 or 512K x8 and Bank2 is 768K x16 or 1536K x8 which are CMOS concurrent Read/Write flash memories manufactured with SST's proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST34HF1601B writes (Program or Erase) with a 2.7-3.3V power supply. The SST34HF1601B device conforms to JEDEC standard pin assignments for x16/x8 memories.

Featuring high-performance Word-Program, the SST34HF1601B device provides a typical Word-Program time of 14 µsec. The devices use Toggle Bit or Data# Polling to detect the completion of the Program or Erase operation. To protect against inadvertent writes, the SST34HF1601B device has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST34HF1601B device is offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST34HF1601B is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST34HF1601B significantly improves performance and reliability, while lowering power consumption. The SST34HF1601B inherently uses less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The SST34HF1601B also improves flexibility while lowering the cost for program, data, and configuration storage applications.

Preliminary Specifications

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST34HF1601B is offered in 48-lead TSOP and 56-ball BGA packages. See Figures 2 and 3 for pin assignments.

Device Operation

All memory banks share common I/O lines, WE# and OE#. Memory bank selection is by bank select address (A_{19}, A_{18}). WE# is used with SDP to control the Erase and Program operations in each memory bank.

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Concurrent Read/Write Operation

Dual bank architecture of SST34HF1601B device allows the concurrent Read/Write operation whereby the user can read from one bank while programming or erasing in the other bank. This operation can be used when the user needs to read system code in one bank while updating data in the other bank.

CONCURRENT READ/WRITE STATE

Bank 1	Bank 2
Read	No Operation
Read	Write
Write	Read
Write	No Operation
No Operation	Read
No Operation	Write

Note: For the purposes of this table, write means to perform Block-, Sector-, or Chip-Erase or Word-Program operations as applicable to the appropriate bank.

Read Operation

The Read operation of the SST34HF1601B is controlled by CE# and OE#; both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data on the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 4).

Word-Program Operation

The SST34HF1601B is programmed on a word-by-word basis. Before programming, the sector where the word exists must be fully erased. The Program operation consists of three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed typically within 10 µs. See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 18 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored. **After detecting the completion of a Word-/Byte-Program operation (either through RY/BY# line, Data# Polling, or Toggle Bit), the host must keep CE# signal low for a minimum duration of Bus Recovery Time (T_{BR} = ~1 µs) before valid data can be read correctly. Please see Figures 5 through 8 for corresponding AC timing diagrams.**

Sector- (Block-) Erase Operation

The Sector- (Block-) Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST34HF1601B offers both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 1 KWord/2 KByte. The Block-Erase mode is based on uniform block size of 32 KWord/64 KByte. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. See Figures 10 and 11 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored.

Chip-Erase Operation

The SST34HF1601B provides a Chip-Erase operation, which allows the user to erase all unprotected sectors/blocks to the "1" state. This is useful when the device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid Read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 9 for timing diagram, and Figure 21 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Write Operation Status Detection

The SST34HF1601B provides one hardware and two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The hardware detection uses the Ready/Busy# (RY/BY#) output pin. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Ready/Busy# (RY/BY#), a Data# Polling (DQ_7) or Toggle Bit (DQ_6) read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Ready/Busy# (RY/BY#)

The SST34HF1601B includes a Ready/Busy# (RY/BY#) output signal. RY/BY# is actively pulled low while during an internal Erase or Program operation is in progress. RY/BY# is an open drain output that allows several devices to be tied in parallel to V_{DD} via an external pull up resistor. RY/BY# is high impedance whenever CE# is high or RST# is low. There is a 1 µs bus recovery time (T_{BR}) required before valid data can be read on the data bus. New commands can be entered immediately after RY/BY# goes high.

Byte/Word (CIOF)

This device includes a CIOF pin to control whether the data I/O pins operate as either x8 or x16. If the CIOF pin is at logic '1' (V_{IH}) the device is in x16 data configuration; all data I/O pins DQ_{15}-DQ_0 are active and controlled by CE# and OE#.

If the CIOF pin is at logic '0', the device is in x8 data configuration; only data I/O pins DQ_7-DQ_0 are active and controlled by CE# and OE#. The remaining data pins DQ_{14}-DQ_8 are at High Z and pin DQ_{15} is used as the Address Input (A_{-1}) for the least significant bit of the address bus.

Data# Polling (DQ_7)

When the SST34HF1601B is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling (DQ_7) timing diagram and Figure 19 for a flowchart. There is a 1 µs bus recovery time (T_{BR}) required before valid data can be read on the data bus. New commands can be entered immediately after DQ_7 becomes true data.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ_6 bit will stop toggling. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Toggle Bit timing diagram and Figure 19 for a flowchart. There is a 1 µs bus recovery time (T_{BR}) required before valid data can be read on the data bus. New commands can be entered immediately after DQ_6 no longer toggles.

Data Protection

The SST34HF1601B provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST34HF1601B provides a hardware block protection which protects the top 4 blocks of Bank 2, 128 KWord/256 KByte in the smaller bank. The block is protected when WP# is held low. See Figure 1 for Block-Protection location.

A user can disable block protection by driving WP# high thus allowing erase or program of data into the protected sectors. WP# must be held high prior to issuing the write command and remain stable until after the entire Write operation has completed.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see Figure 15). When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 14).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

The SST34HF1601B provides the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST34HF1601B is shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value during any SDP command sequence.

Product Identification

The Product Identification mode identifies the device and manufacturer. For details, see Table 4 for software operation, Figure 12 for the Software ID Entry and Read timing diagram and Figure 20 for the Software ID Entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

	Word	Data
Manufacturer's ID	0000H	00BFH
Device ID		
SST34HF1601B	0001H	2762H

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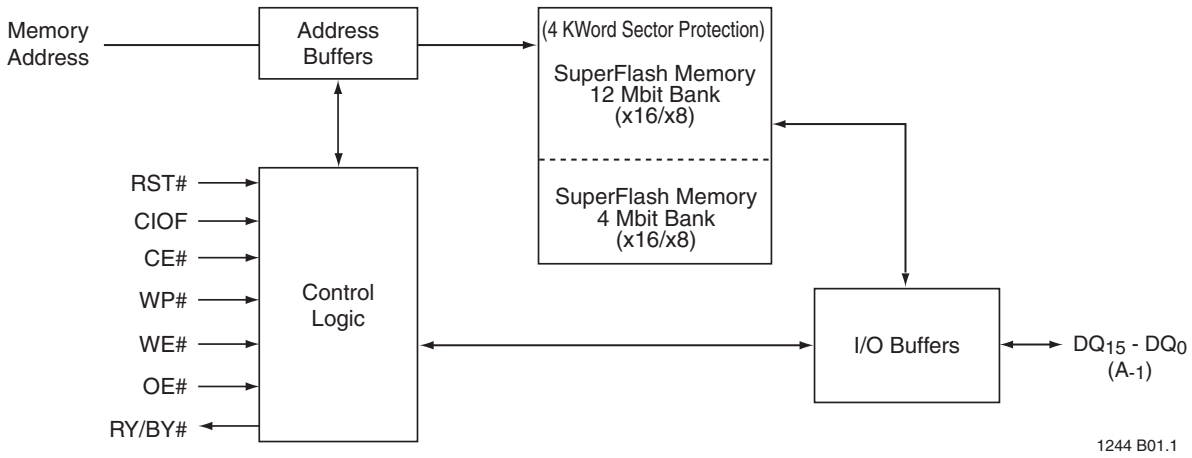
Product Identification Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 4 for the software command code, Figure 13 for timing waveform and Figure 20 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM



Top Four Blocks Protection; 32 KWord Blocks; 1 KWord Sectors

128 KWord Block Protection	FFFFFH F8000H	Block 31	Bank 2
	F7FFFH F0000H	Block 30	
	EFFFFH E8000H	Block 29	
	E7FFFH E0000H	Block 28	
	DFFFFH D8000H	Block 27	
	D7FFFH D0000H	Block 26	
	CFFFFH C8000H	Block 25	
	C7FFFH C0000H	Block 24	
	BFFFFH B8000H	Block 23	Bank 1
	B7FFFH B0000H	Block 22	
	AFFFFH A8000H	Block 21	
	A7FFFH A0000H	Block 20	
	9FFFFH 98000H	Block 19	
	97FFFH 90000H	Block 18	
	8FFFFH 88000H	Block 17	
	87FFFH 80000H	Block 16	
	7FFFFH 78000H	Block 15	
	77FFFH 70000H	Block 14	
	6FFFFH 68000H	Block 13	
	67FFFH 60000H	Block 12	
	5FFFFH 58000H	Block 11	
	57FFFH 50000H	Block 10	
	4FFFFH 48000H	Block 9	
	47FFFH 40000H	Block 8	
	3FFFFH 38000H	Block 7	
	37FFFH 30000H	Block 6	
	2FFFFH 28000H	Block 5	
	27FFFH 20000H	Block 4	
	1FFFFH 18000H	Block 3	
	17FFFH 10000H	Block 2	
	00FFFFH 008000H	Block 1	
	007FFFH 000000H	Block 0	

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FIGURE 1: SST34HF1601B, 1 MBIT X16 CONCURRENT SUPERFLASH DUAL-BANK MEMORY ORGANIZATION

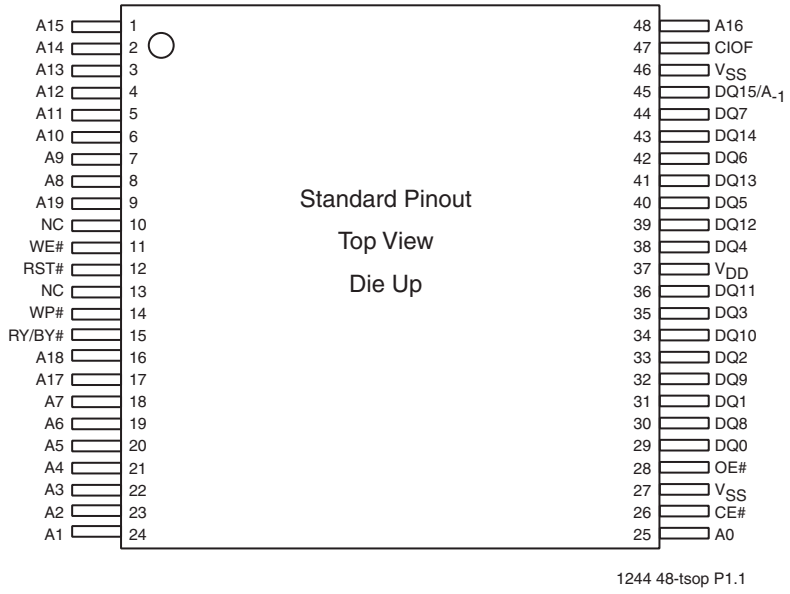
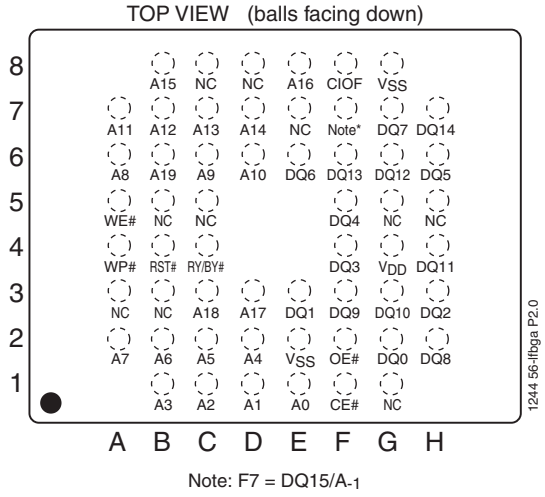


FIGURE 2: PIN ASSIGNMENTS FOR 48-LEAD TSOP (12MM X 20MM)



Note: F7 = DQ15/A-1

FIGURE 3: PIN ASSIGNMENTS FOR 56-BALL LFBGA (8MM X 10MM)

Preliminary Specifications

TABLE 2: PIN DESCRIPTION

Symbol	Name	Functions
A_{19}-A_0	Address Inputs	To provide memory addresses. During Sector-Erase and Hardware Sector Protection, A_{19}-A_{10} address lines will select the sector. During Block-Erase A_{19}-A_{15} address lines will select the block.
DQ_{14}-DQ_0	Data Input/Output (15 pins)	To output data during Read cycles and receive input data during Write cycles Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
DQ_{15}/A_{-1}	Data I/O and LSB Address	DQ_{15} is used as a data I/O pin when in x16 mode (CIOF='1') A-1 is used as the LSB address input pin when in x8 mode (CIOF='0')
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable	To control the Write operations
CIOF	Byte Selection for Flash	When low, select Byte mode. When high, select Word mode.
RST#	Hardware Reset	To reset and return the device to Read mode
RY/BY#	Ready/Busy#	To output the status of a Program or Erase Operation RY/BY# is a open drain output, so a 10KΩ - 100KΩ pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read.
WP#	Write Protect	To protect and unprotect the bottom 4 sectors from Erase or Program operation.
V_{DD}	Power Supply	To provide 2.7-3.3V power supply voltage
V_{SS}	Ground	
NC	No Connection	Unconnected pins

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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	DQ_7-DQ_0	DQ_{15}-DQ_8		Address
					CIOF = V_{IH}	CIOF = V_{IL}	
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	D_{OUT}	DQ_{14}-DQ_8 = High Z	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	D_{IN}	$DQ_{15} = A_{-1}$	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X[1]	X	High Z	Sector or Block address, XXH for Chip-Erase
Standby	V_{IH}	X	X	High Z	High Z	High Z	X
Write Inhibit	X	V_{IL}	X	High Z / D_{OUT}	High Z / D_{OUT}	High Z	X
	X	X	V_{IH}	High Z / D_{OUT}	High Z / D_{OUT}	High Z	X
Product Identification							
Software Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer's ID (BFH)	Manufacturer's ID (00H)	High Z	See Table 4
				Device ID[2]	Device ID[2]	High Z	

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1. X can be V_{IL} or V_{IH}, but no other value.
2. Device ID = 2762H

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Word-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA[3]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X[4]	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA_X[4]	50H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[5,6]	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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1. Address format A_{14}-A_0 (Hex), Addresses A_{19}- A_{15} can be V_{IL} or V_{IH}, but no other value, for the command sequence in x16 mode. For x8 mode, addresses A_{19}- A_{15}, A_{-1} (LSB), and DQ_{14}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for the command sequence.
2. DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for the command sequence.
3. WA = Program word address
4. SA_X for Sector-Erase; uses A_{19}-A_{10} address lines
   BA_X for Block-Erase; uses A_{19}-A_{15} address lines
5. The device does not remain in Software Product Identification mode if powered down.
6. With A_{19}-A_1 = 0; SST Manufacturer's ID = 00BFH, is read with A_0 = 0
   SST34HF1601B Device ID = 2762H, is read with A_0 = 1

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) for TSOP . . . . . 240°C
Output Short Circuit Current . . . . . 50 mA

OPERATING RANGE:

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 5 ns
Output Load . . . . . C_L = 30 pF
See Figures 16 and 17

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.3V

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Active V_{DD} Current				Address input=V_{ILT}/V_{IHT}, at f=1/T_{RC} Min, V_{DD}=V_{DD} Max
	Read		35	mA	CE#=OE#=V_{IL}, WE#=V_{IH}, all I/Os open
	Program and Erase		40	mA	CE#=V_{IL}, OE#=V_{IH}
	Concurrent Read/Write		75	mA	
I_{SB}	Standby V_{DD} Current		30	µA	CE#=V_{IHC}, V_{DD}=V_{DD} Max
I_{RT}	Reset V_{DD} Current		20	µA	RST# = V_{SS} ± 0.3V
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	V_{DD}=V_{DD} Max
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD}=V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	10 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10 pF

T7.0 1244

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T8.0 1244

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.3V

Symbol	Parameter	SST34HF1601B-80		Units
		Min	Max	
T_{RC}	Read Cycle Time	80		ns
T_{CE}	Chip Enable Access Time		80	ns
T_{AA}	Address Access Time		80	ns
T_{OE}	Output Enable Access Time		40	ns
T_{CLZ}[1]	CE# Low to Active Output	0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		ns
T_{CHZ}[1]	CE# High to High-Z Output		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		30	ns
T_{OH}[1]	Output Hold from Address Change	0		ns
T_{RP}[1]	RST# Pulse Width	500		ns
T_{RHR}[1]	RST# High before Read	50		ns
T_{RY}[1,2]	RST# Pin Low to Read Mode		150	µs

T9.0 1244

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase and Program operations.
   This parameter does not apply to Chip-Erase operations.

TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Word-Program Time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms
T_{BY}[1]	RY/BY# Delay Time	90		ns
T_{BR}	Bus# Recovery Time	1		µs

T10.0 1244

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

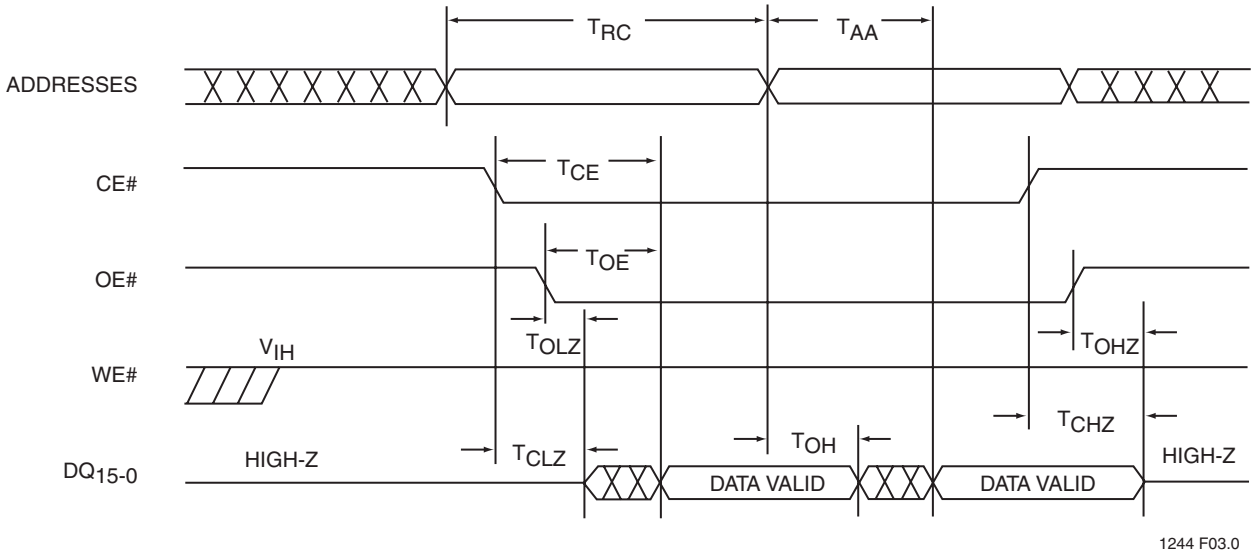
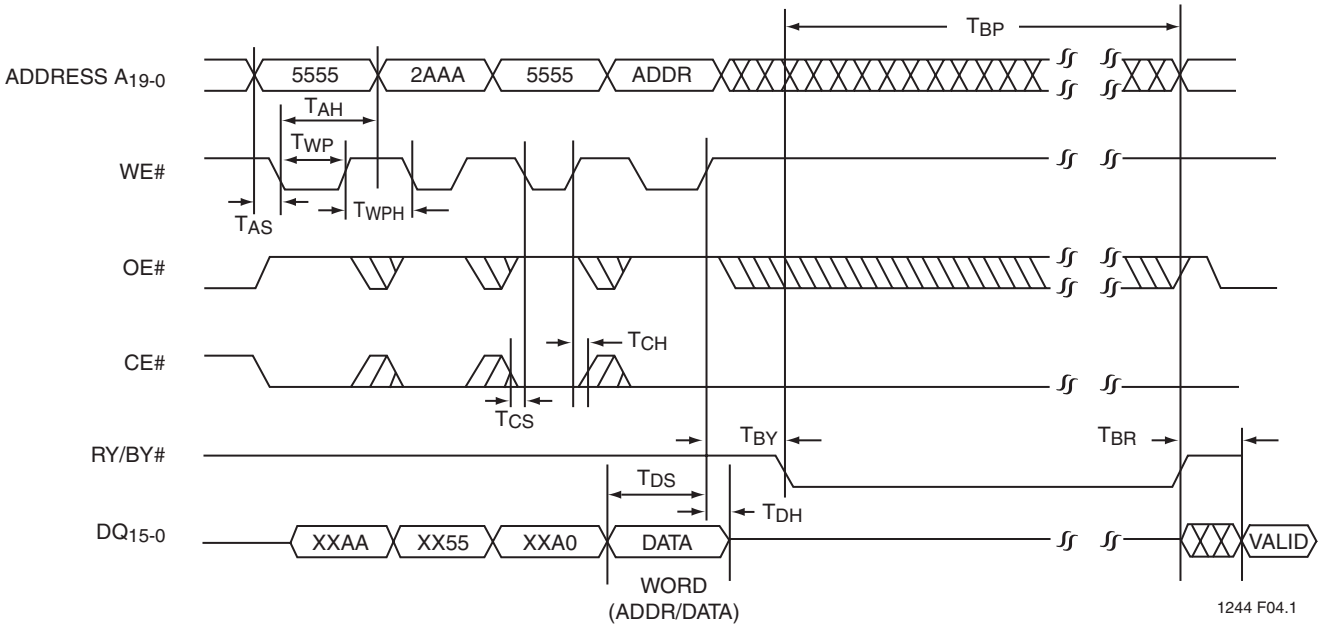
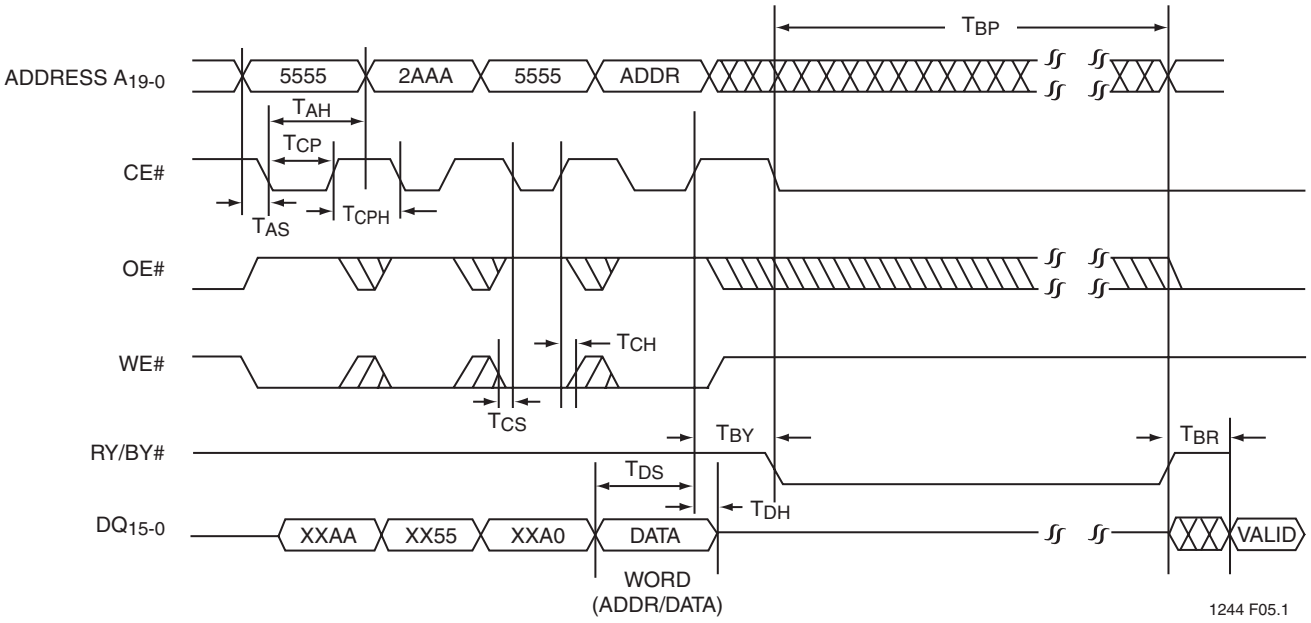


FIGURE 4: READ CYCLE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A_{-1} = ADDRESS INPUT)



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 5: WE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A_{-1} = ADDRESS INPUT)



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 6: CE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A_{-1} = ADDRESS INPUT)

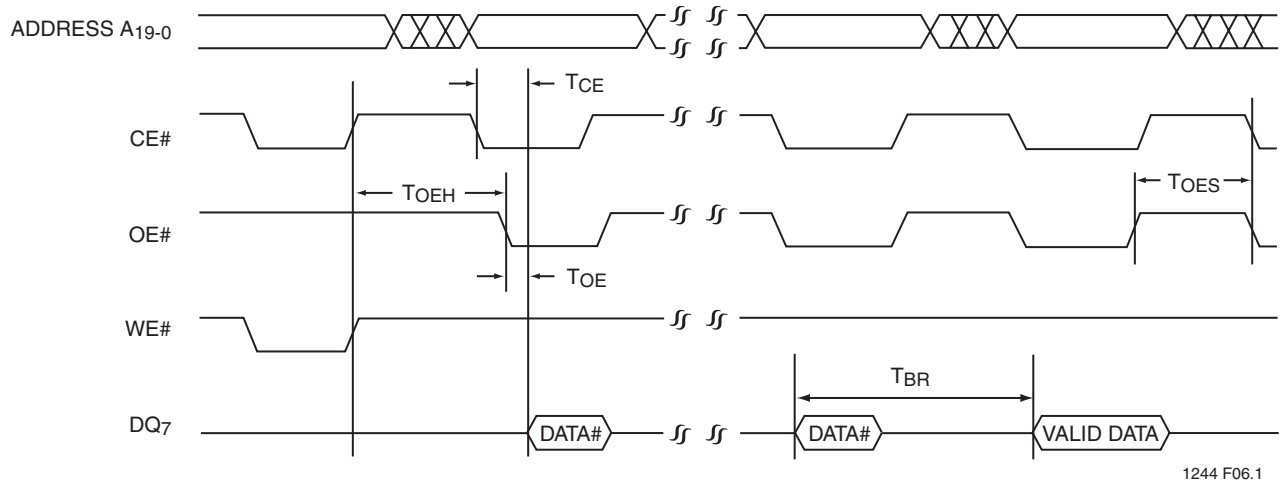


FIGURE 7: DATA# POLLING TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A_{-1} = ADDRESS INPUT)

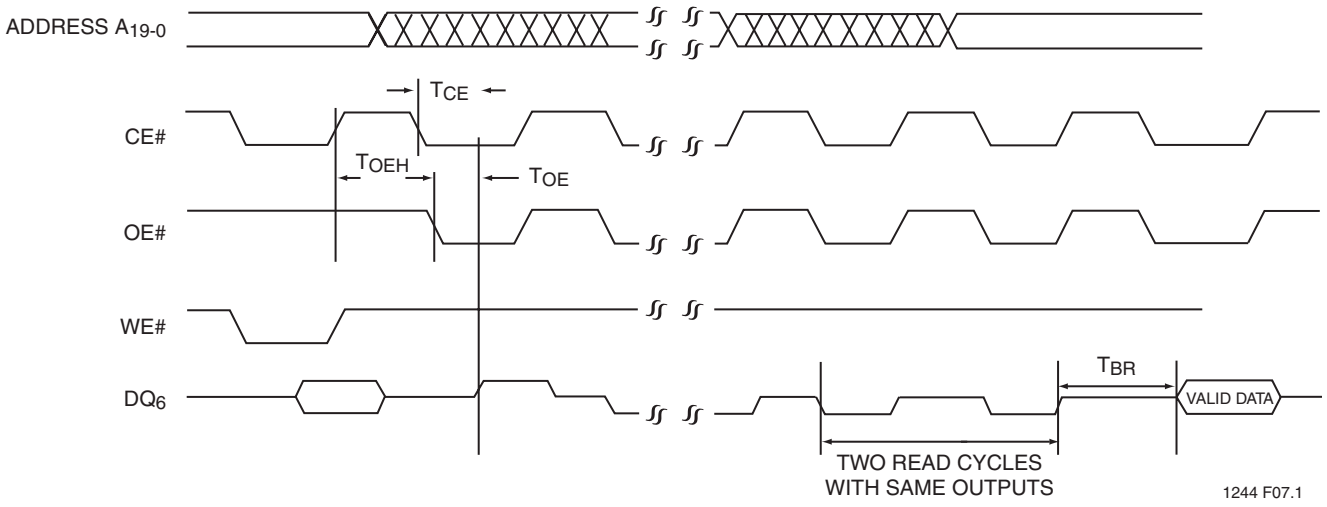
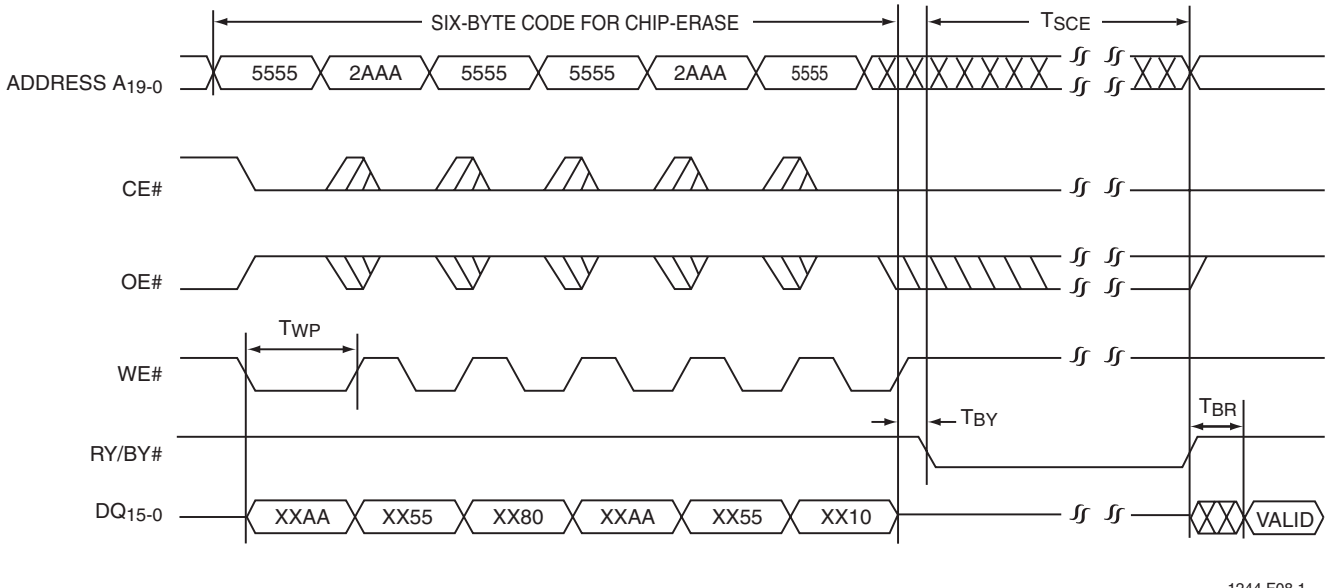
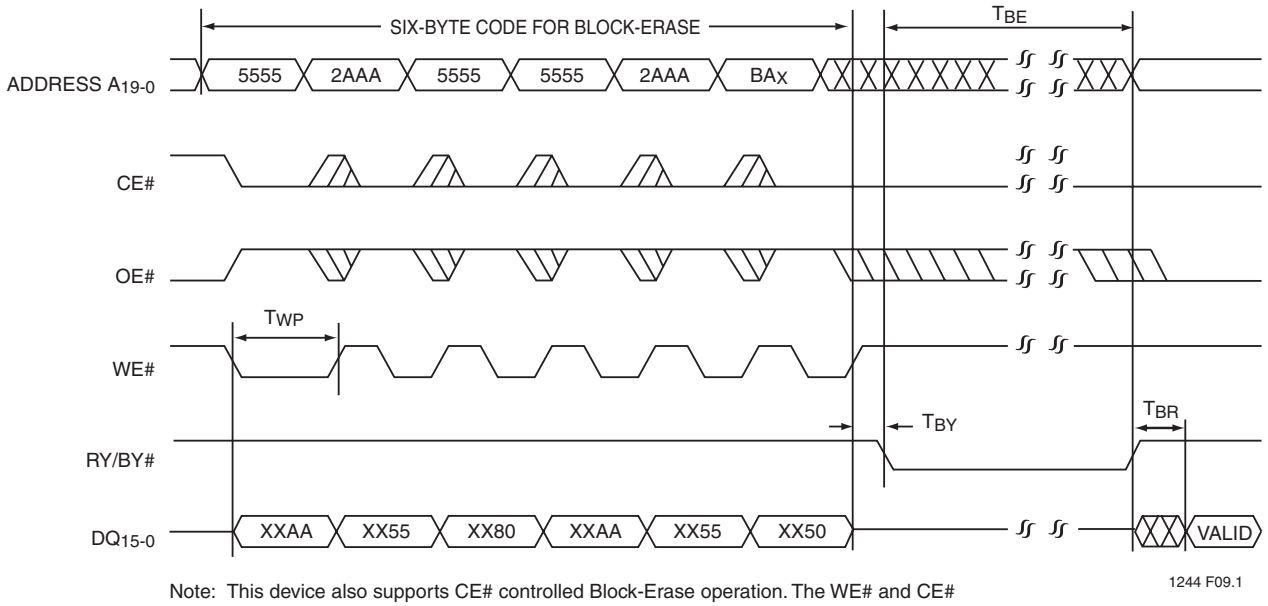


FIGURE 8: TOGGLE BIT TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A_{-1} IS DON'T CARE)



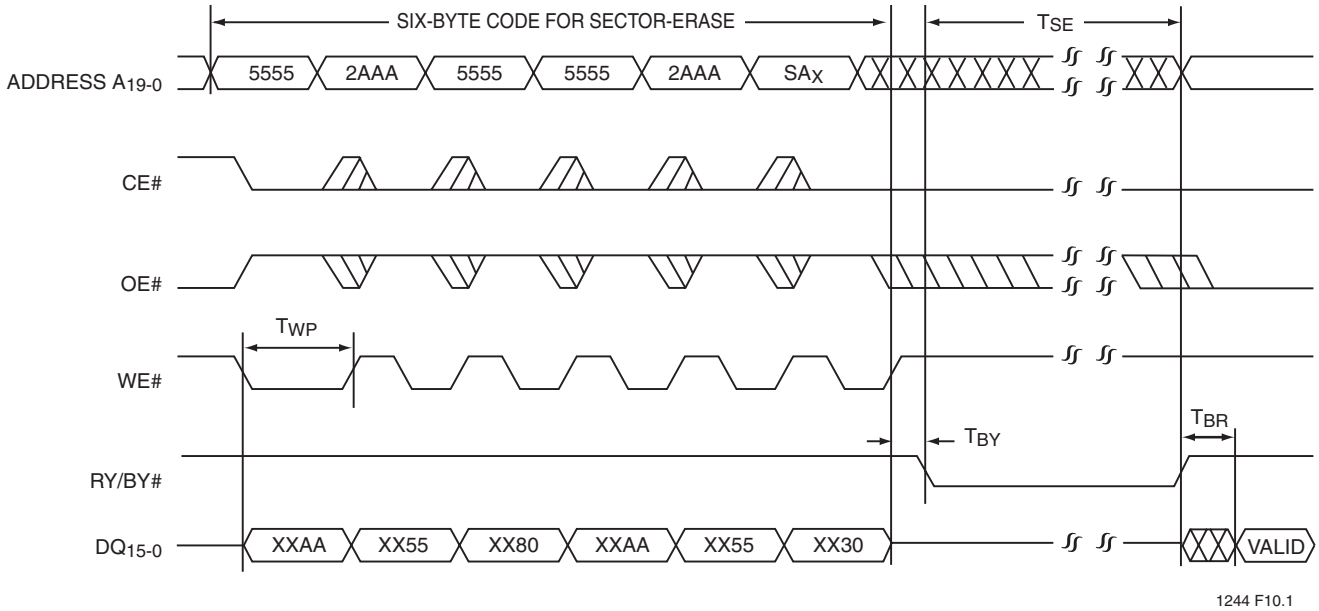
Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 9: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A_{-1} IS DON'T CARE)



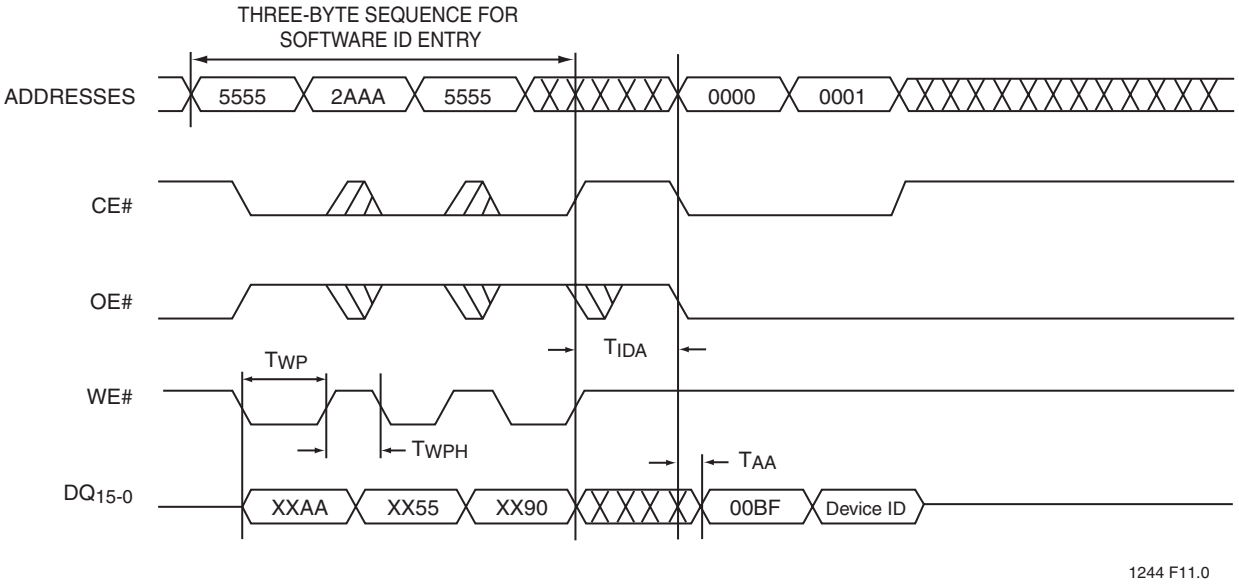
Note: This device also supports CE# controlled Block-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 10)
BA_X = Block Address
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 10: WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A_{-1} IS DON'T CARE)



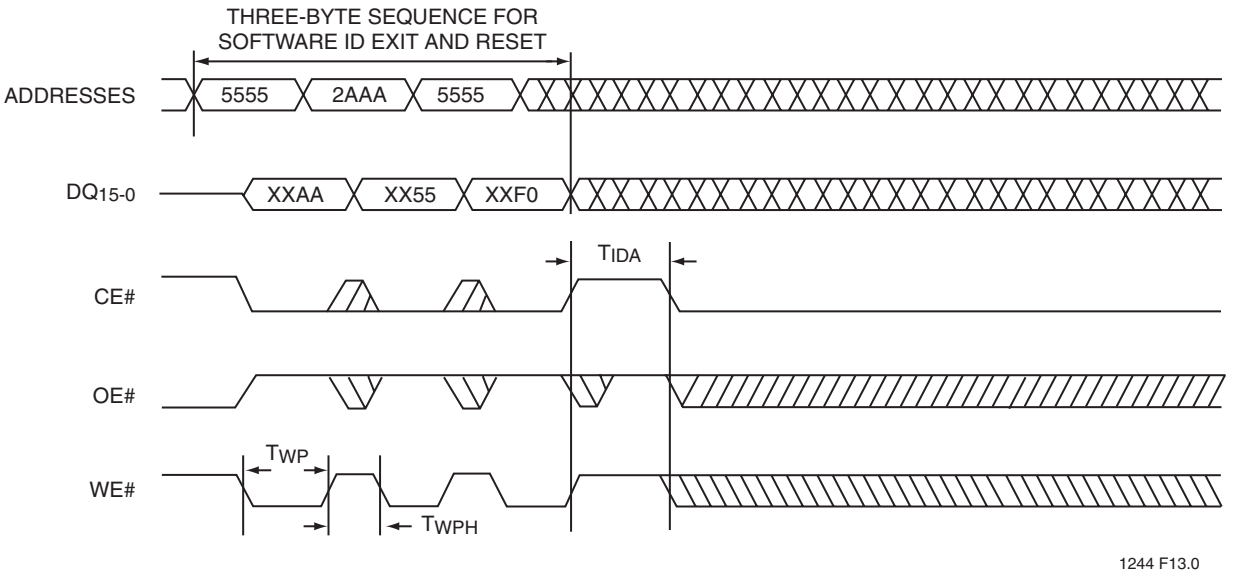
Note: This device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 10)
SA_X = Sector Address
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 11: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A_{-1} IS DON'T CARE)



Device ID = 2762H for SST34HF1601B
Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 12: SOFTWARE ID ENTRY AND READ FOR WORD MODE (FOR BYTE MODE A_{-1} = 0)



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 13: SOFTWARE ID EXIT FOR WORD MODE (FOR BYTE MODE A_{-1} = 0)

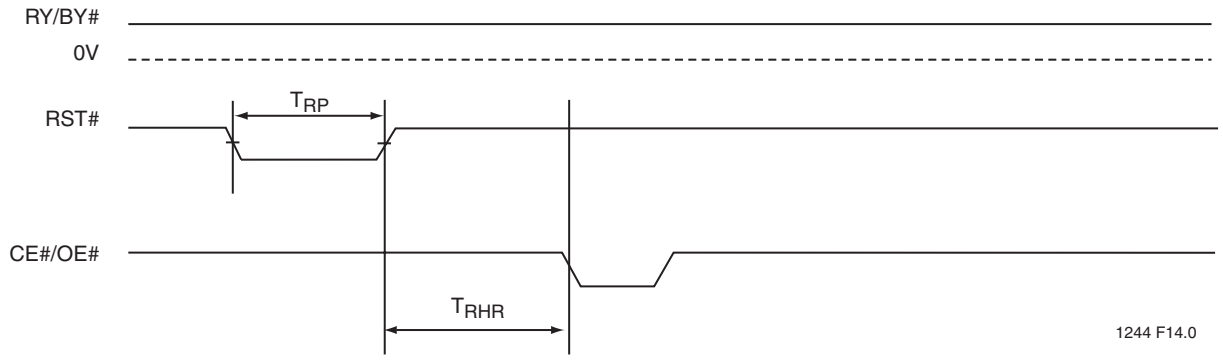


FIGURE 14: RST# TIMING (WHEN NO INTERNAL OPERATION IS IN PROGRESS)

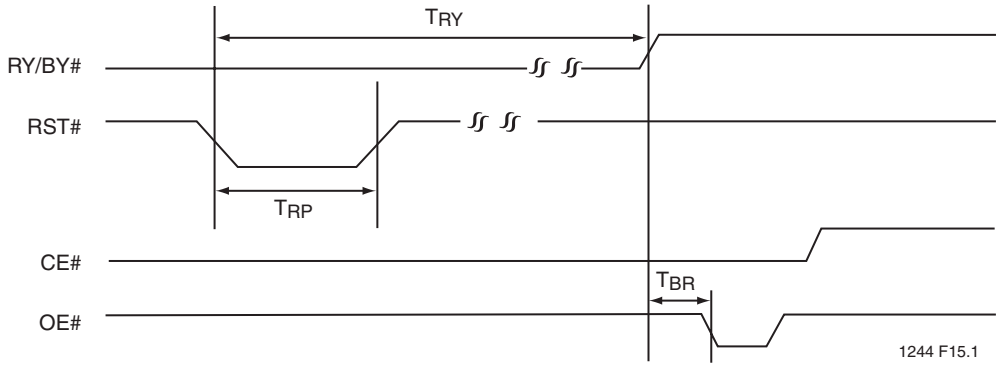
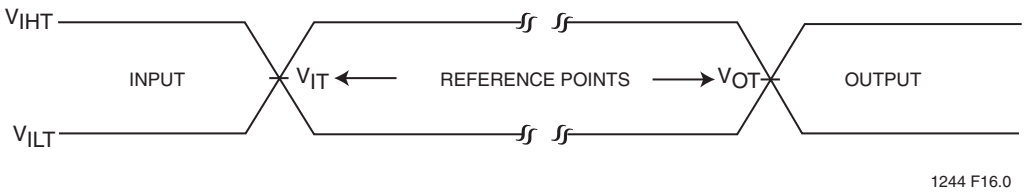


FIGURE 15: RST# TIMING (DURING SECTOR- OR BLOCK-ERASE OPERATION)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 16: AC INPUT/OUTPUT REFERENCE WAVEFORMS

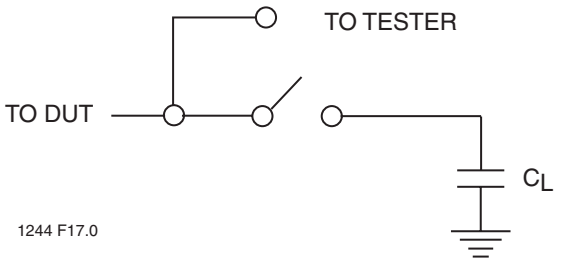
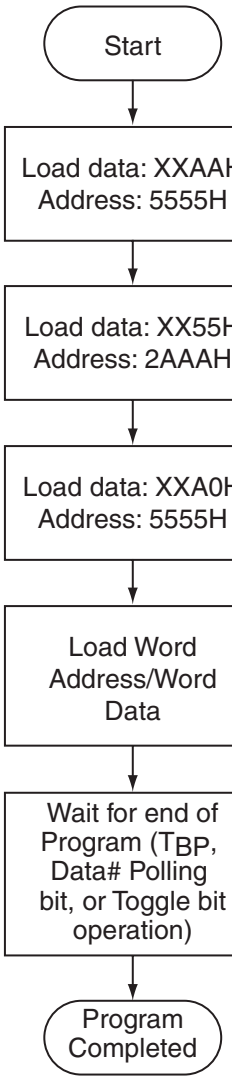


FIGURE 17: A TEST LOAD EXAMPLE



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 18: WORD-PROGRAM ALGORITHM

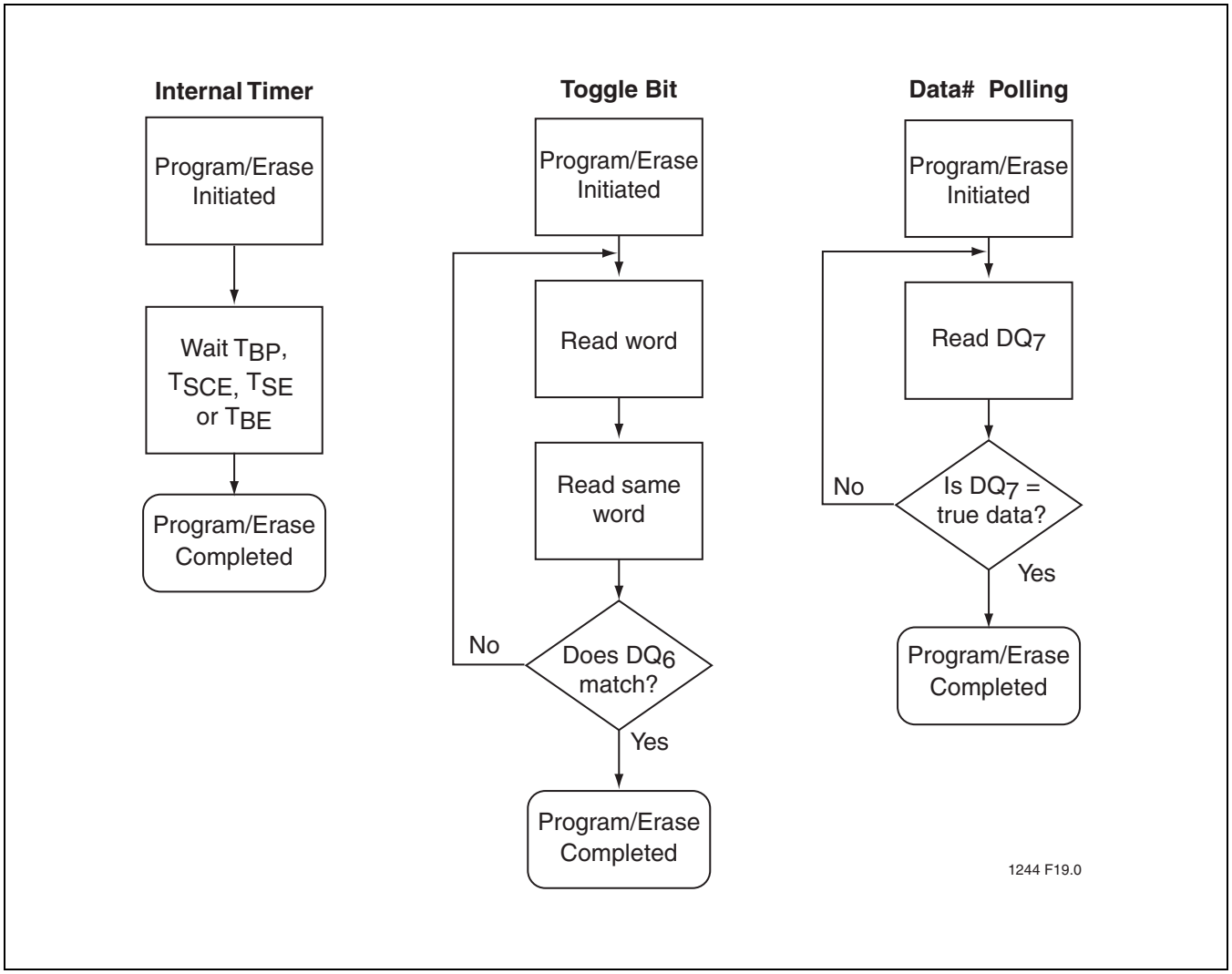
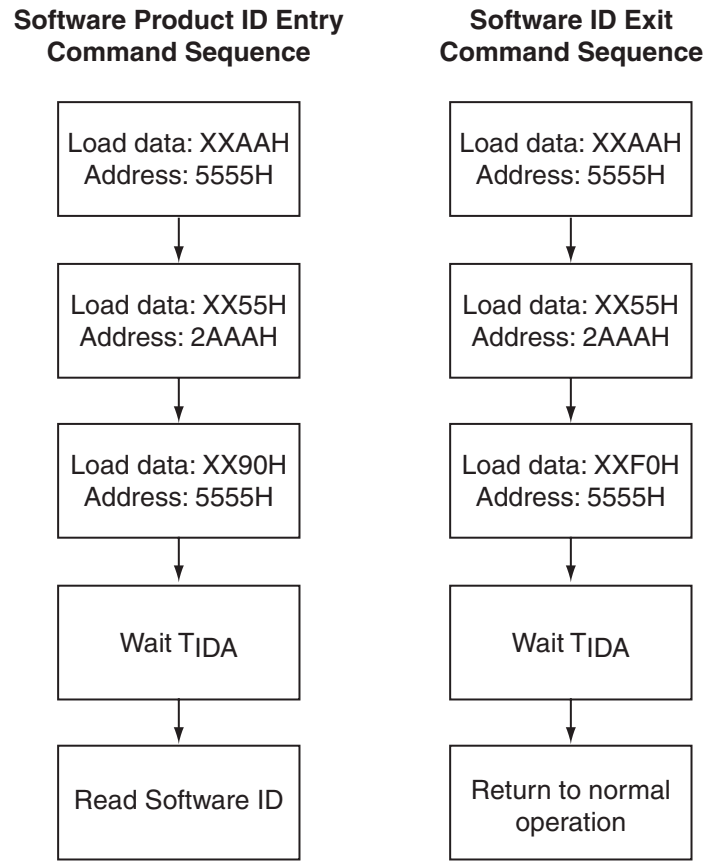


FIGURE 19: WAIT OPTIONS



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 20: SOFTWARE PRODUCT ID COMMAND FLOWCHARTS

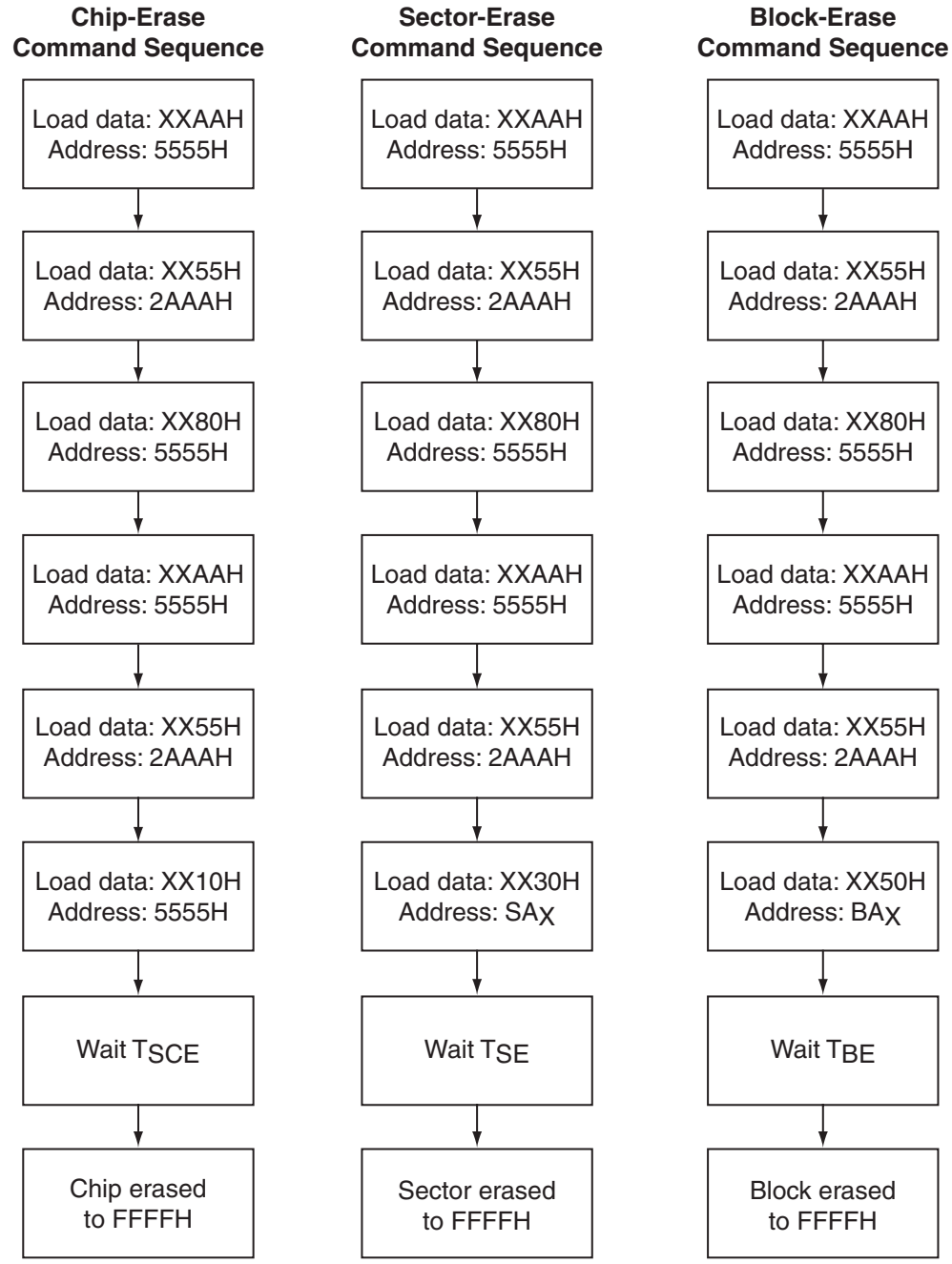
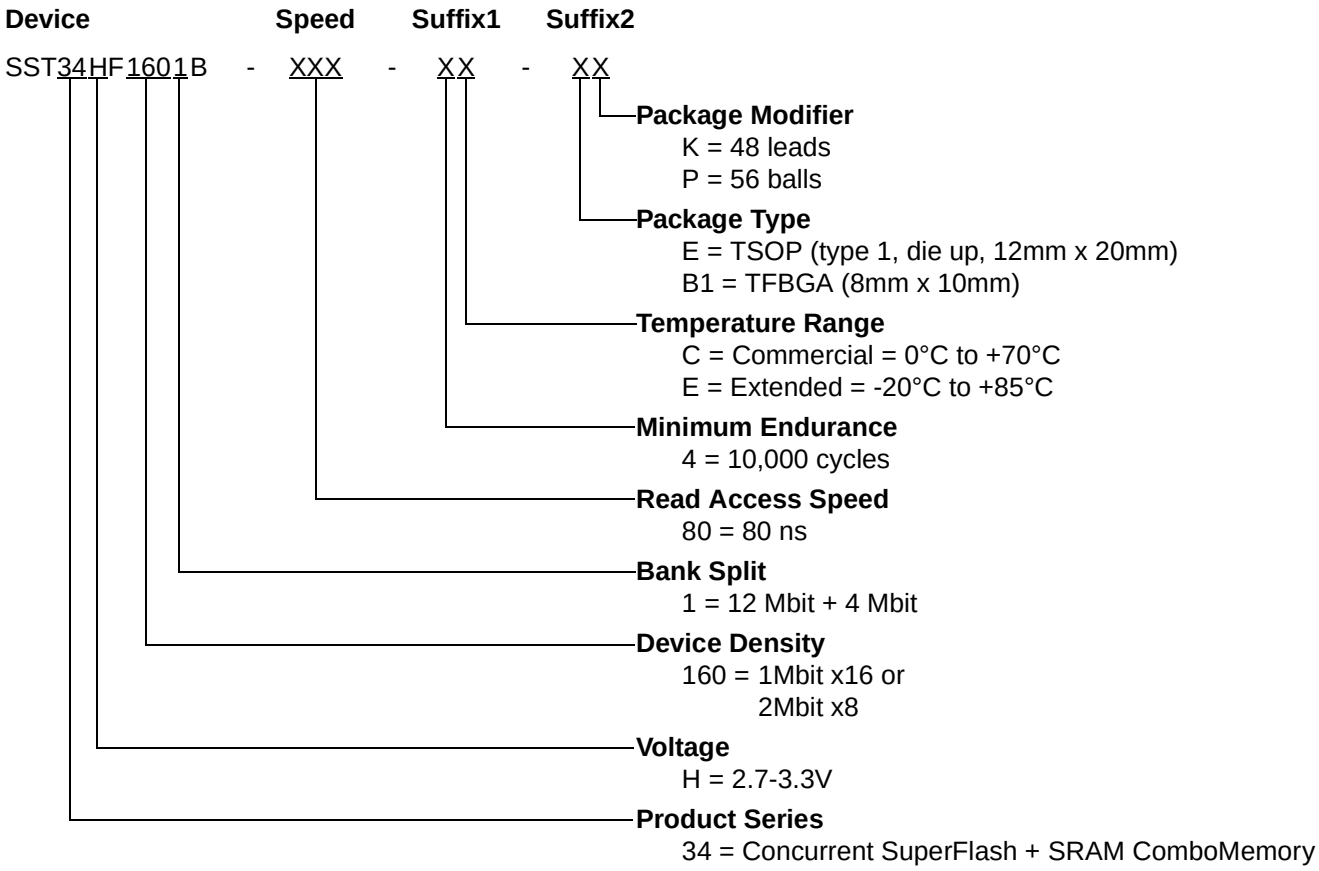


FIGURE 21: ERASE COMMAND SEQUENCE

PRODUCT ORDERING INFORMATION



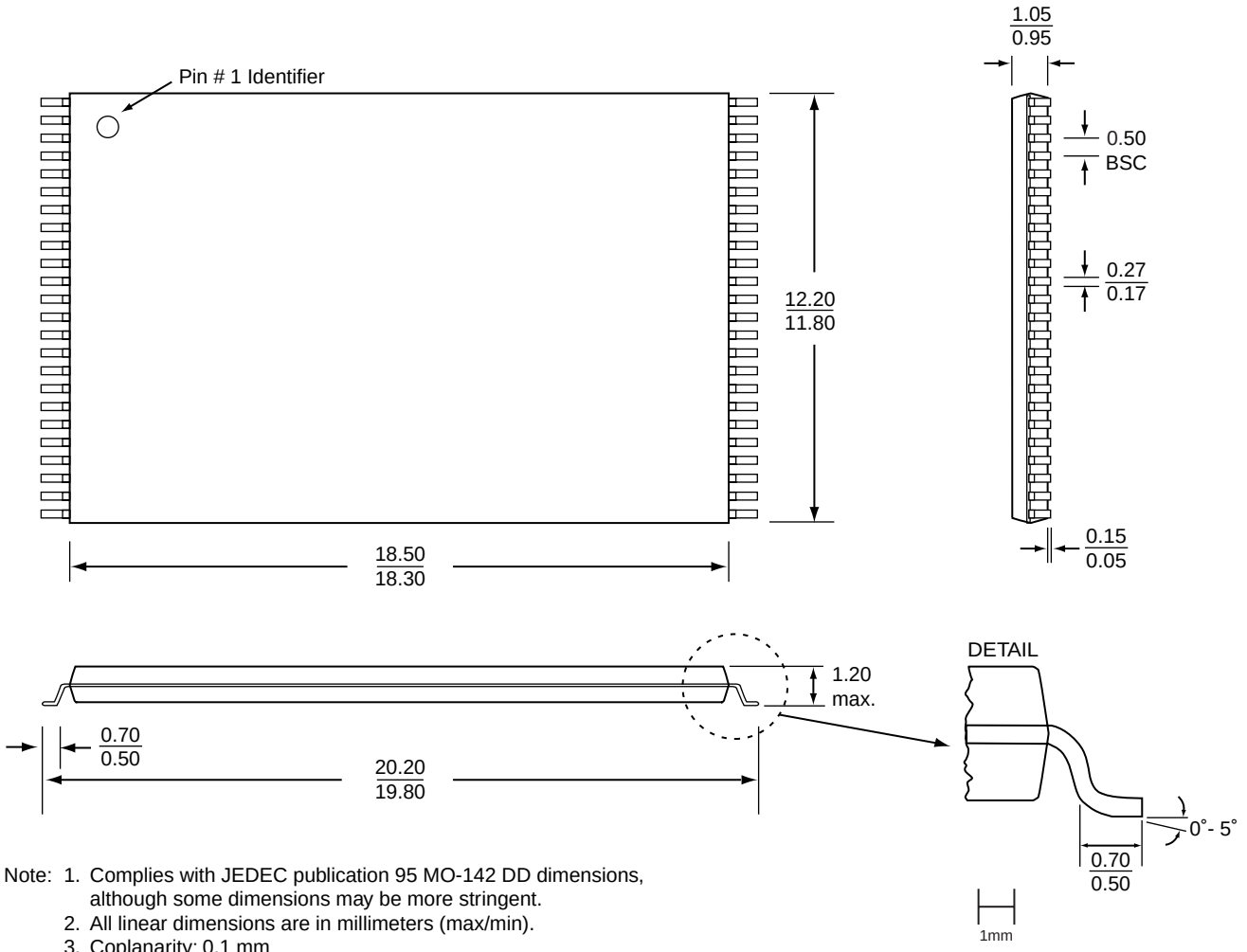
Valid combinations for SST34HF1601B

SST34HF1601B-80-4C-EK SST34HF1601B-80-4C-B1P
SST34HF1601B-80-4E-EK SST34HF1601B-80-4E-B1P

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

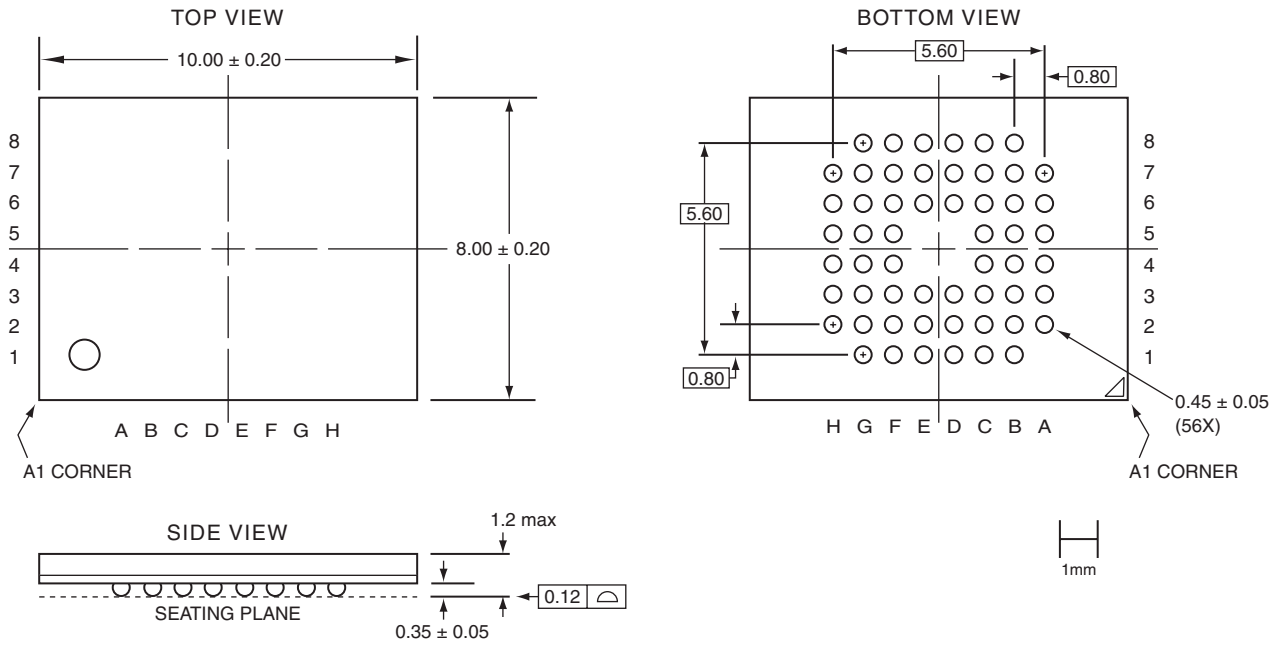
Preliminary Specifications

PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-142 DD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

48-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 12MM X 20MM
SST PACKAGE CODE: EK



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (± 0.05 mm)

56-tfbga-B1P-8x10-450mic-1

56-BALL THIN-PROFILE, FINE-PITCH BALL GRID ARRAY (TFBGA) 8MM X 10MM
SST PACKAGE CODE: B1P

TABLE 11: REVISION HISTORY

Number	Description	Date
00	• Initial release	Jun 2003
01	• 2004 Data Book • Updated B1P package diagram	Nov 2003