National Semiconductor

29F52•29F53
8-Bit Registered Transceiver

General Description

The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The A_0–A_7 output pins are guaranteed to sink 24 mA (20 mA mil.) while the B_0–B_7 output pins are designed for 64 mA.

The 29F53 is an inverting option of the 29F52. Both transceivers are AMD Am2952/2953 functional equivalents.

Features

- 8-bit registered transceivers
- Separate clock, clock enable and TRI-STATE output enable provided for each register
- AMD Am2952/2953 functional equivalents
- Both inverting and non-inverting options available
- 24-Pin slimline package

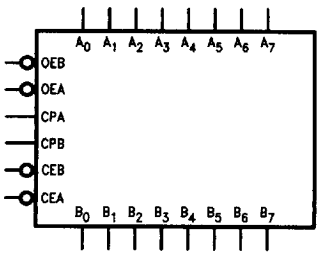
Ordering Code: See Section 11

Commercial	Package Number	Package Description
29F52SPC	N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
29F52SC (Note 1)	M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
29F53SPC	N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

Logic Symbols

29F52



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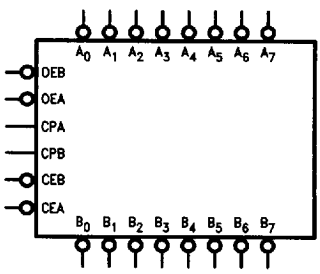
29F53



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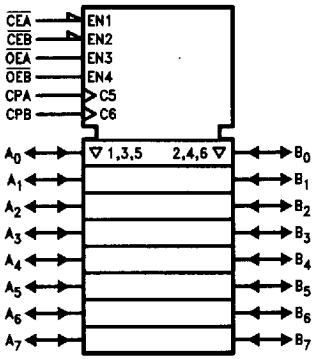
Logic Symbols (Continued)

IEEE/IEC
29F52



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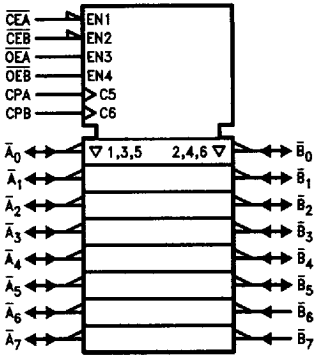
IEEE/IEC
29F53



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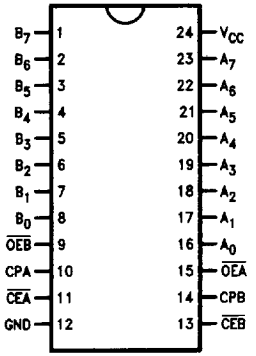
Connection Diagrams

Pin Assignment
for DIP and SOIC
29F52



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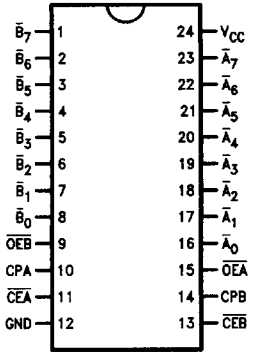
Pin Assignment
for DIP
29F53



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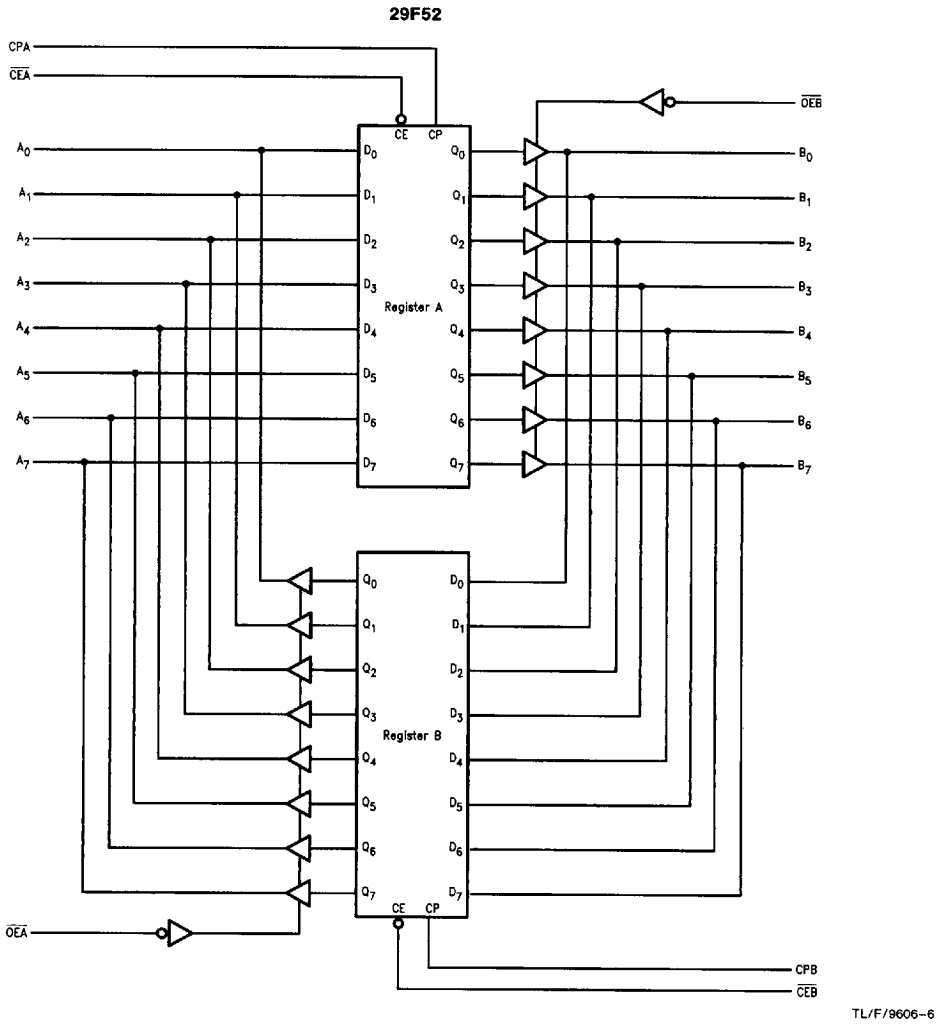
Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_7	A-Register Inputs/	3.5/1.083	70 μA/0.65 mA
	B-Register TRI-STATE Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
B_0–B_7	B Register Inputs/	3.5/1.083	70 μA/0.65 mA
	A-Register TRI-STATE Outputs	600/106.6 (80)	−12 mA/64 mA (48 mA)
$\overline{OEA}$	Output Enable A-Register	1.0/1.0	20 μA/−0.6 mA
CPA	A-Register Clock	1.0/1.0	20 μA/−0.6 mA
$\overline{CEA}$	A-Register Clock Enable	1.0/1.0	20 μA/−0.6 mA
$\overline{OEB}$	Output Enable B-Register	1.0/1.0	20 μA/−0.6 mA
CPB	B-Register Clock	1.0/1.0	20 μA/−0.6 mA
$\overline{CEB}$	B-Register Clock Enable	1.0/1.0	20 μA/−0.6 mA

Block Diagrams



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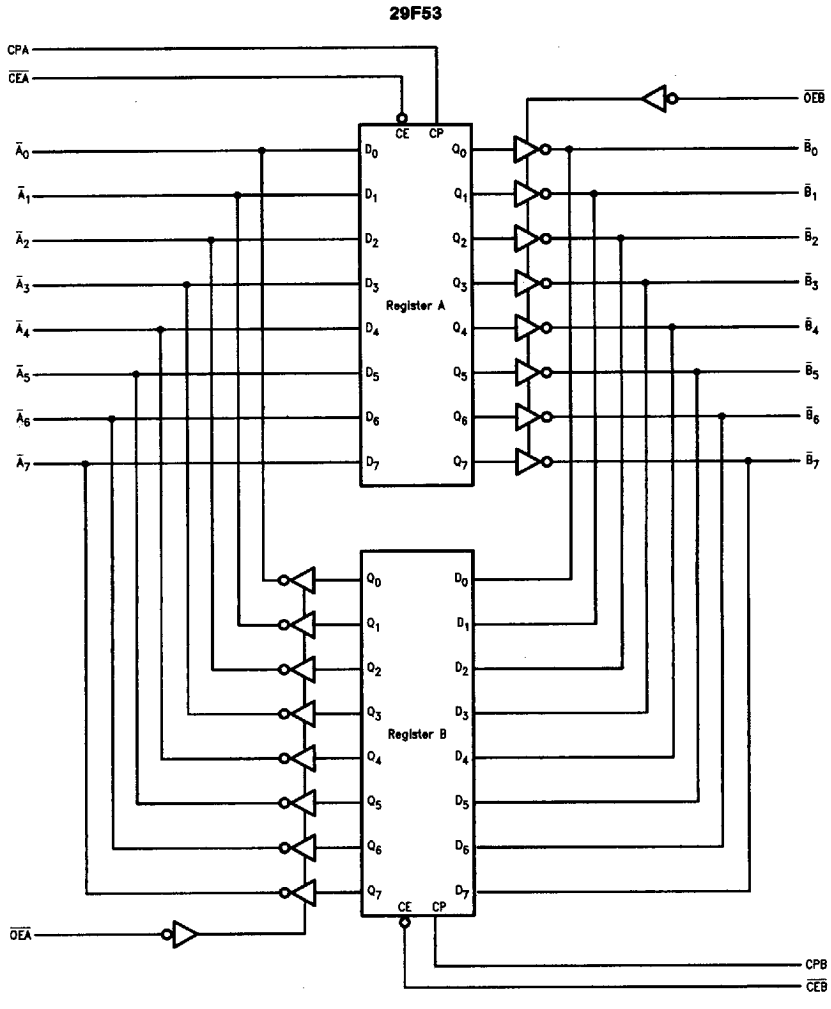
Block Diagrams (Continued)



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Output Control

OE	Internal Q	Y-Output 29F52	Y-Output 29F53	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

Register Function Table (Applies to A or B Register)

Inputs D	Inputs CP	Inputs CE	Internal Q	Function
X	X	H	NC	Hold Data
L	⌐	L	L	Load Data
H	⌐	L	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (A_n)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_n, B_n)
		54F 10% V_{CC}	2.0					I_{OH} = −12 mA (B_n)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (A_n)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_n, B_n)
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA (B_n)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (A_n)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (A_n)
		54F 10% V_{CC}			0.55			I_{OL} = 48 mA (B_n)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA (A_n)
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA (B_n)
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				1.0	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V (A_n)
			−100		−225			V_{OUT} = 0V (B_n)
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current			130	190	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				190	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current				190	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPA or CPB to A_n or B_n	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	2–3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 2.5	6.5 5.5	9.0 7.5			2.0 2.0	10.0 8.5	ns	2–5

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to CPA or CPB	4.0 4.0				4.5 4.5		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to CPA or CPB	2.0 2.0				2.5 2.5		ns	2–6
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	1.0 4.0				1.5 4.5		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	2.0 2.0				2.5 2.5		ns	2–6
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0				3.5 3.5		ns	2–4