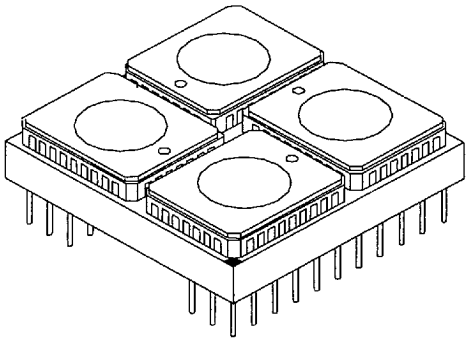
1 Megabit UVEPROM

DPV3232VA

DESCRIPTION:

The DPV3232VA is a 66-pin Pin Grid Array (PGA) consisting of four 32K x 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.6" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing four 0.1µf decoupling capacitors.

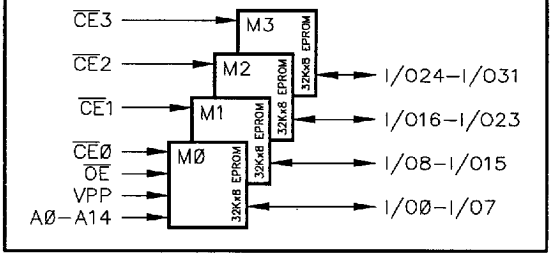


FEATURES:

- Organizations Available:
  128K x 8, 64K x 16 or 32K x 32
- Access Times:
  55*, 70, 90, 120, 150, 170, 200, 250ns (max.)
- Fully Static Operation
  - No clock or refresh required
- Programming Voltage 13.0 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm
  (100µs Pulses Typ.)
- Common Data Inputs and Outputs
- TTL-Compatible Inputs and Outputs
- 66-Pin PGA (Pin Grid Array) Package
- Upward Pin Compatible with DPV12832VA, 128K X 32 VERSAPAC EPROM
- Same Package as other Versapac Versions (EEPROM, SRAM and MIXED)
- Module Weight is 15 grams

* Commercial and Industrial only.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A14	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE}$0 - $\overline{CE}$3	Chip Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+ 5V)
V_{SS}	Ground
V_{PP}	Programming Voltage
N.C.	No Connect

PIN-OUT DIAGRAM

1	I/08	12	N.C.	23	I/014			34	I/024	45	VDD	56	I/03Ø
2	I/09	13	$\overline{CE}$1	24	I/013			35	I/025	46	$\overline{CE}$3	57	I/029
3	I/01Ø	14	VSS	25	I/012			36	I/026	47	N.C.	58	I/028
4	A13	15	I/015	26	I/011			37	A6	48	I/031	59	I/027
5	A14	16	A1Ø	27	$\overline{OE}$			38	A7	49	A3	6Ø	AØ
6	N.C.	17	A11	28	N.C.	(TOP VIEW)		39	VPP	5Ø	A4	61	A1
7	N.C.	18	A12	29	N.C.			4Ø	A8	51	A5	62	A2
8	N.C.	19	VDD	3Ø	I/06			41	A9	52	N.C.	63	I/022
9	I/ØØ	2Ø	$\overline{CE}$Ø	31	I/05			42	I/016	53	$\overline{CE}$2	64	I/021
1Ø	I/01	21	N.C.	32	I/04			43	I/017	54	VSS	65	I/02Ø
11	I/02	22	I/07	33	I/03			44	I/018	55	I/023	66	I/019

ABSOLUTE MAXIMUM RATINGS 1			
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [2]	-0.5 to +7.0	V
$V_{I/O}$	Input/Output Voltage [2]	-0.5 to +7.0	V
V_{PP}	Programming Voltage [2]	-0.5 to +14.0	V

RECOMMENDED OPERATING RANGE 2					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage[4]	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		$V_{DD}+1.0$	V
V_{IL}	Input LOW Voltage	-0.2		0.8	V
V_{DDP}	Supply Voltage (Programming)	6.25	6.50	6.75	V
V_{PP}	V_{PP} Supply Voltage 5	12.75	13.0	13.25	V

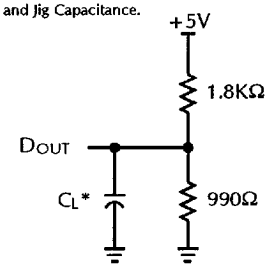
CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	15	pF	V_{IN} = 0V
C_{ADR}	Address Input	50		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	25		

AC TEST CONDITIONS: Including Programming	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

Output Load		
Float	C_L	Parameters Measured
1	100 pF	except t_{DF} and t_{DFP}
2	5 pF	t_{DF} and t_{DFP}

Figure 1. Output Load

* Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS 6: Over operating ranges										
Symbol	Characteristics	Test Conditions		X8		X16		X32		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	$V_{IN} = V_{DD}$		-40	40	-40	40	-40	40	µA
I_{OUT}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{IN} = V_{DD} or V_{SS}		-40	40	-20	20	-10	10	µA
I_{CC}	V_{DD} Operation Current, Read	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA; Cycle = min. Duty = 100%	150-250ns		35		60		100	mA
			55-120ns		160		180		220	
I_{SB1}	V_{DD} Standby Current I_{OUT} = 0mA (TTL)	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	150-250ns		15		15		15	mA
			55-120ns		140		140		140	
I_{SB2}	V_{DD} Standby Current (CMOS)	$\overline{CE}$ = V_{DD} ± 0.3V, I_{OUT} = 0mA	120-250ns		800		800		800	µA
		$V_{IN} \geq V_{DD}$ -0.3V or $V_{IN} \leq$ 0.3V	55-120ns		120		120		120	mA
I_{PP1}	V_{PP} Supply Current Programming	$\overline{CE}$, = V_{IL}, $\overline{OE}$ = V_{IH}			30		60		120	mA
I_{PP3}	V_{PP} Supply Current Read [4]	$\overline{CE}$, $\overline{OE}$ = V_{IL}, I_{OUT} > 0mA			80		80		80	µA
V_{OL}	Output LOW Voltage	I_{OUT} = 2.1mA			0.45		0.45		0.45	V
V_{OH1}	Output HIGH Voltage	I_{OUT} = -400µA		2.4		2.4		2.4		V
V_{IL}	Input LOW Level			-0.2	0.8	-0.2	0.8	-0.2	0.8	V
V_{IH}	Input HIGH Level			2.2	$V_{DD}+1$	2.2	$V_{DD}+1$	2.2	$V_{DD}+1$	V

FUNCTIONS AND PIN CONNECTIONS						
Mode \ Function		$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	I/O0 - I/O31
Read Operations	Read	L	L	5V	5V	Data Out
	Output Deselect	L	H			High Impedance
	Standby	H	X			High Impedance
Program Operations (T_A = +25 ± 5°C)	Program	L	H	13.0V	6.5V	Data In
	Program Inhibit	H	H			High Impedance
	Program Verify	H	L			Data Out

L = LOW, H = HIGH and X = Don't Care

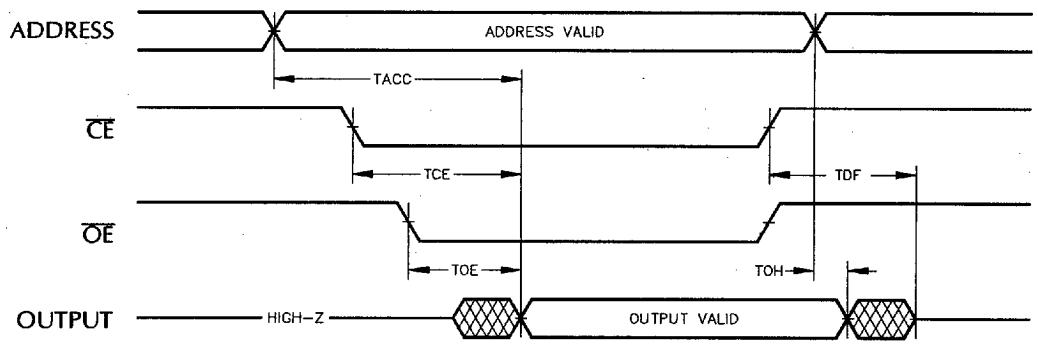
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges											
No.	Symbol	Parameter	55ns*		70ns		90ns		120ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address Access Time [8]		55		70		90		120	ns
2	t_{CE}	Chip Enable to Output Valid [7]		55		70		90		120	ns
3	t_{OE}	Output Enable to Output Valid [7, 8]		25		30		30		50	ns
4	t_{DF}	$\overline{OE}$ or $\overline{CE}$ HIGH to Output Float [3, 9]		25		30		30		45	ns
5	t_{OH}	Output Hold from Address Change		0		0		0		0	ns

* Commercial and Industrial only.

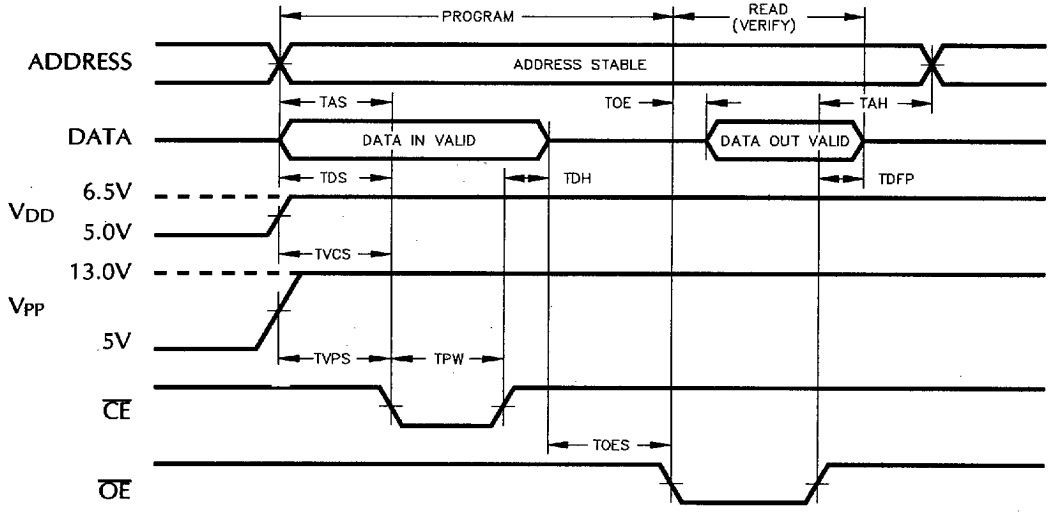
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges											
No.	Symbol	Parameter	150ns		170ns		200ns		250ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address Access Time [8]		150		170		200		250	ns
2	t_{CE}	Chip Enable to Output Valid [7]		150		170		200		250	ns
3	t_{OE}	Output Enable to Output Valid [7, 8]		60		70		75		100	ns
4	t_{DF}	$\overline{OE}$ or $\overline{CE}$ HIGH to Output Float [3, 9]		50		50		55		60	ns
5	t_{OH}	Output Hold from Address Change		0		0		0		0	ns

AC PROGRAMMING CONDITIONS AND CHARACTERISTICS: Over operating ranges					
No.	Symbol	Parameter	Min.	Max.	Unit
6	t_{AS}	Address Set-up Time	2		µs
7	t_{OES}	Output Enable Set-up Time	2		µs
8	t_{DS}	Data Set-up Time	2		µs
9	t_{VCS}	V_{DD} Set-up Time [5]	2		µs
10	t_{VPS}	V_{PP} Set-up Time [5]	2		µs
11	t_{AH}	Address Hold Time	0		µs
12	t_{DH}	Data Hold Time	2		µs
13	t_{DFP}	Output Enable HIGH Output Float Delay [3]	0	130	ns
14	t_{PW}	Programming Pulse Width [10]	95	105	µs

READ TIMING



PROGRAMMING TIMING [4]



PROGRAMMING AND ERASING INFORMATION

Programming

Upon delivery from Dense-Pac, or after erasure *(See Erasure section)*, the DPV3232VA contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV3232VA through the procedure of programming. A 0.1µF capacitor between V_{PP} and V_{SS} is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.5V and +13.0V to be applied to V_{DD} and V_{PP} respectively.

Individual bytes or address locations can be selected and programmed by using the programming algorithm shown in Figure 2. In the programming mode, $\overline{OE}$ is set at V_{IH}, V_{DD} is set at +6.5V, and then V_{PP} is set at +13.0V. After the applied address and input data signals are stable, programming is accomplished by a 100µs V_{IL} pulse on the $\overline{CE}$ pin *(refer to the Programming Timing Diagram)*.

First program each address with a 100µs pulse on the $\overline{CE}$ without verification. Then return to first address and start a verification loop verifying each address. If an address location fails verification, apply up to 10 consecutive 100µs $\overline{CE}$ pulses with a verification after each pulse.

If the device fails to program after 10 attempts, the programming is considered failed. After the byte is verified, continue the algorithm through all the required addresses. Lower V_{PP} to 5.0V and then lower V_{DD} to +5.0V and compare the data programmed with the original data to determine if the device passes. A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

Erasure

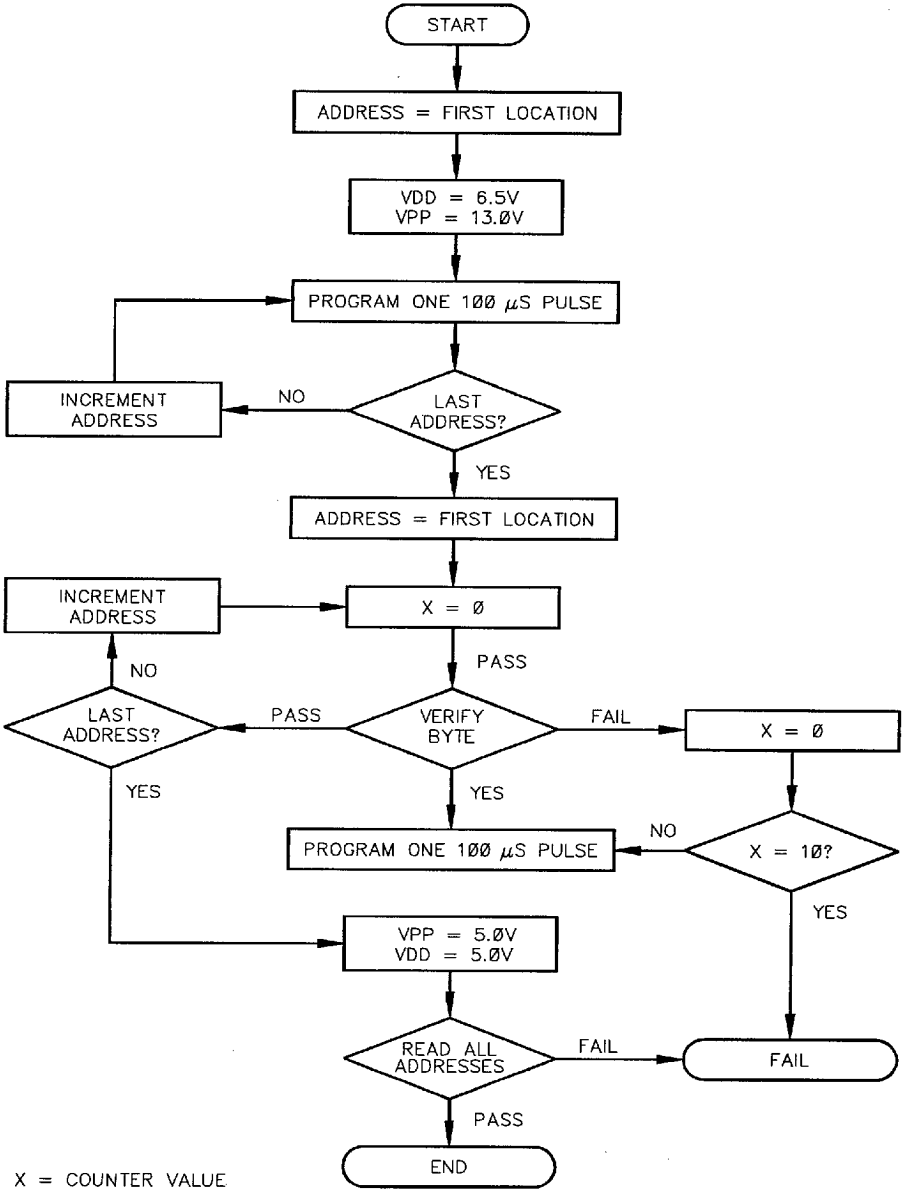
To clear all locations of their programmed contents it is necessary to expose the DPV3232VA to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase a DPV3232VA. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å) with an intensity of 12,000µW/cm^2] for 20 minutes.

The DPV3232VA and similar devices can be erased by light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV3232VA. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are with respect to V_{SS}.
3. This parameter is guaranteed and not 100% tested.
4. V_{DD} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP}.
5. V_{PP} must not be greater than 14.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with V_{PP} = 13.0V. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from 5.0V to 13.0V or vice-versa.
6. t_A = -55°C to +125°C, V_{DD} = 5.0V ± 0.5V, and V_{PP} = V_{DD} reading. t_A = +25°C ± 5°C, V_{DD} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V programming.
7. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the following edge of $\overline{CE}$ without impact on t_{CE}.
8. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the following Address is valid without impact on t_{ACC}.
9. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
10. Program Pulse Width Tolerance is 100µs ± 5%.

Figure 2. Programming Flow Chart



30A014-60
REV. C

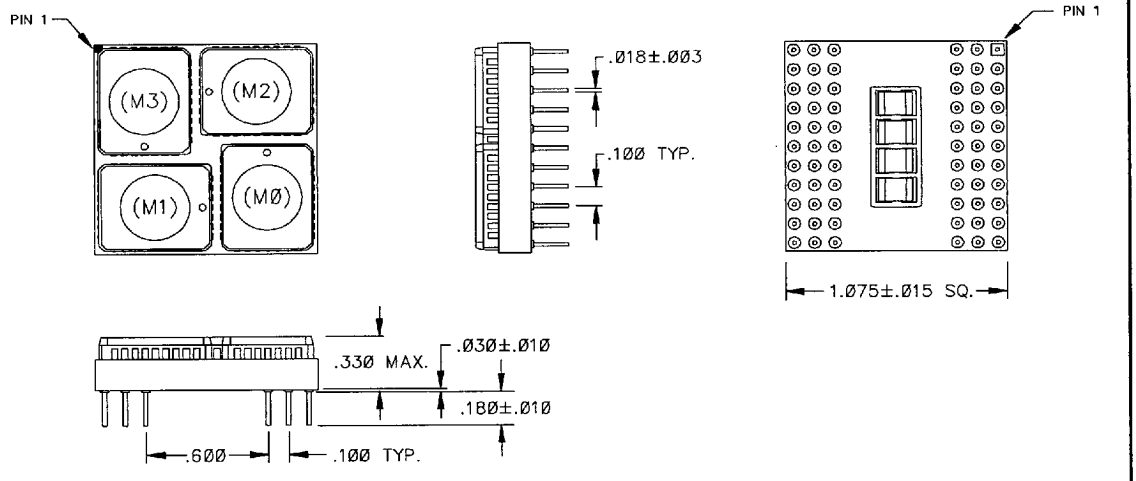
ORDERING INFORMATION

DP V3232 V A – XX X
PREFIX DEVICE TYPE PACKAGE DESIG. SPEED GRADE

C	COMMERCIAL	0° to +70°C
I	INDUSTRIAL	−40° to +85°C
M	MILITARY	−55° to +125°C
B *	MIL−PROCESSED	−55° to +125°C
55	55ns ("C" & "I" GRADE ONLY)	
70	70ns	
90	90ns	
12	120ns	
15	150ns	
17	170ns	
20	200ns	
25	250ns	
A	DPV12832VA PIN−OUT COMPATABLE	
V	66−PIN PGA VERSAPAC	
	UVEPROM 128KX8, 64KX16 OR 32KX32	

* B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAMS



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