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- Viterbi Decoders – 256 Kbps to 25 Mbps Maximum Data Rates
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- Low Data Rate Vocoder
- VCOs

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- Digital Open Satellite Networks
- Digital Audio Broadcast
- Microwave Point-to-Point
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- Direct Broadcast Systems (BDS)
- Digital Video Reception
- High-Speed Data Communications

GENERAL DESCRIPTION

Forward Error Correction (FEC) techniques provide higher throughput data rates with improved bit error rate performance for power-limited (and in some cases bandwidth-limited) digital communication channels. Convolutional encoding of data combined with Viterbi decoding at the receiving node is the industry FEC standard for digital channels, especially those concerned with errors caused by the introduction of additive white Gaussian noise (AWGN). Satellite communication channels are examples of this noise environment (figure 1).

The QUALCOMM Q1601 Viterbi Decoder provides the ideal solution for high-volume, cost-sensitive systems which require the coding gain of the Viterbi algorithm. The capabilities of this single-chip device have been optimized for modern digital communication channels. Figure 2 provides an overall block diagram of the decoder functions of the Q1601 FEC system.

The Q1601 device processes data using the industry standard rate ½ constraint length (k) equals seven algorithm. The Q1601 decoder provides built-in synchronization capability for standard binary phase shift keying (BPSK), quartenary phase shift keying (QPSK), and offset quartenary phase shift keying (OQPSK) modems and operates with either 1-bit hard-decision data or 3-bit soft-decision encoded data.

The Q1601 device includes two powerful built-in techniques for monitoring synchronization status and performing channel bit error rate (BER) measurements. In addition, the Q1601 includes a processor interface to facilitate control and status monitoring functions while keeping device pinout to a minimum.

The Q1601 Viterbi Decoder is packaged in a 68-pin plastic leaded chip carrier (PLCC) package and is implemented in fully static CMOS logic to reduce power consumption. The Q1601 Viterbi Decoder also uses fully parallel circuit architecture to negate the requirement for a high speed computation clock as found in most Viterbi decoder implementations.

The Q1601 device is well suited for many commercial satellite communications networks. The same FEC

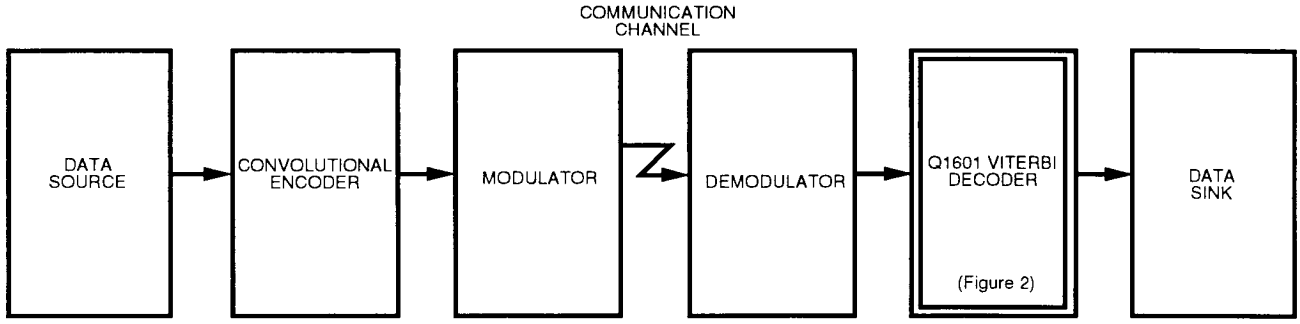


Figure 1. Typical Application of the Q1601 in a Communication System

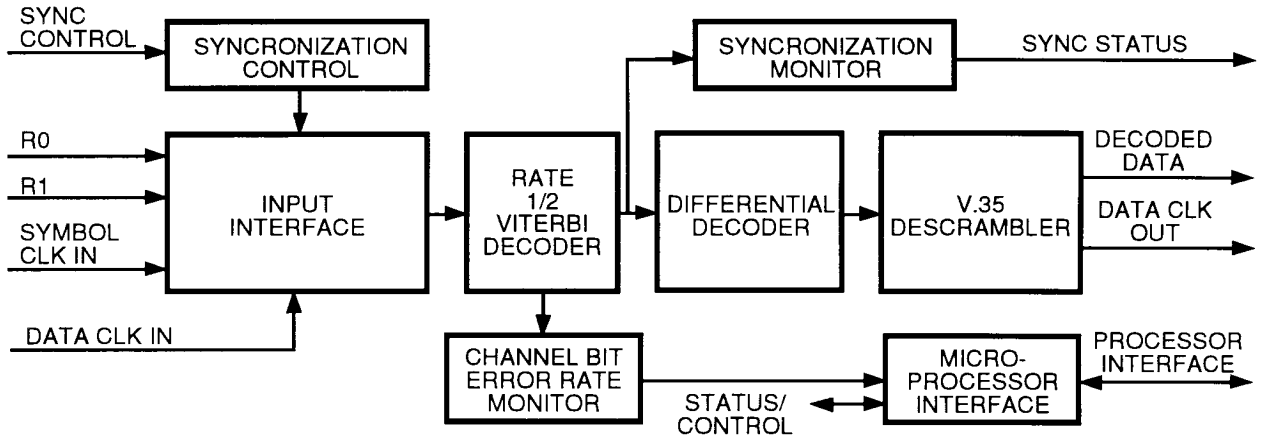


Figure 2. Q1601 Decoder Block Diagram

technique is also used in many military and NASA communications systems. The low cost and high performance of the Q1601 decoder also makes it ideal for FEC requirements in systems such as direct broadcast satellite (DBS), very small aperture terminal (VSAT), digital modems, and high-speed data communications.

THEORY OF OPERATION

Convolutional Encoding

Convolutional codes have been studied and used for FEC in digital communications systems since the 1950s. A convolutional code maps a number (n) of information bits into a number (m) of single-bit "code words" to be transmitted over the channel, where m>n. The ratio of $^{n}/_{m}$ is referred to the code rate. For instance, a commonly used convolutional code transforms each information bit (i.e., n=1) to two code words (i.e., m=2) prior to transmission over the noisy channel. This is a rate ½ code.

The transformation from information bits to code words for transmission is accomplished by a time convolution of the information data with a finite-memory windowing function, commonly referred to as a generating function. In the case of rate ½, two generating functions (G0 and G1) are convolved with the information data stream such that each time a new information data bit is considered, the G0 and G1 generating functions create one output bit or code word each (i.e., C0, C1, respectively).

The length of the finite memory of the convolutional generating function is the "constraint length" of the code. Figure 3 shows the encoder generating functions of the rate ½ code used in conjunction with the Q1601 Viterbi Decoder. As the diagram shows, the memory length of the encoder is six previous bits plus the current input bit; thus, this is a constraint length seven

code (commonly denoted as k=7). The generating functions of the convolutional code are identified by denoting the "taps" of each convoluting function. For the rate ½ k=7 code, the generating functions are denoted as G0=1111001 (binary) or 171 (octal) and G1=1011011 (binary) or 133 (octal). This algorithm provides the best error correcting performance of all rate ½ k=7 codes.

Viterbi Decoding

While the implementation of a convolutional encoder is simple, the decoding of such a coded data stream at the receiving node is quite complex. In the late 1960s, Dr. A. J. Viterbi described a maximum likelihood decoding technique that greatly reduced the circuit sophistication of previous approaches. In spite of this advance, the circuit complexity of such a decoder prevented high-speed, single-chip implementations of the Viterbi algorithm until the mid-1980s when QUALCOMM introduced the Q1401 Viterbi Decoder. The introduction of the Q0256 and Q1650 Viterbi Decoders in 1990 offered higher speeds and more efficient operation. Now, the Q1601 Viterbi Decoder is the most cost-effective, single-chip implementation of the Viterbi algorithm.

Viterbi decoding consists fundamentally of three processes. The first step is to generate a set of correlation measurements, known as "branch metrics," for each "m" grouping of code words input from the communication channel (where "m" is 2 for rate ½). These branch metric values indicate the correlation between the received code words and the 2^m possible code word combinations.

A Viterbi decoder determines the state of the 7-bit memory at the encoder, using a maximum likelihood technique. Once the value of the encoder memory is determined, the original information is known (since the encoder memory is simply the information that has been stored in the memory).

In step two, the encoder state is determined through the generation of a set of 2^{k-1} "state metrics" (remember that "k" is the constraint length) which are occurrence probabilities for each of the 2^{k-1} possible encoder memory states. As state metrics are computed, a binary decision is formed for each of the 2^{k-1} possible states as to the probable path taken to arrive at that particular state. These binary decisions are stored in a "path memory."

In step three, the decoded output data is computed. To do this, the "path" from the current state to some point in the finite past is traced back by "chaining" the binary decisions stored in the path memory from state to state. The effects caused by noise to the one

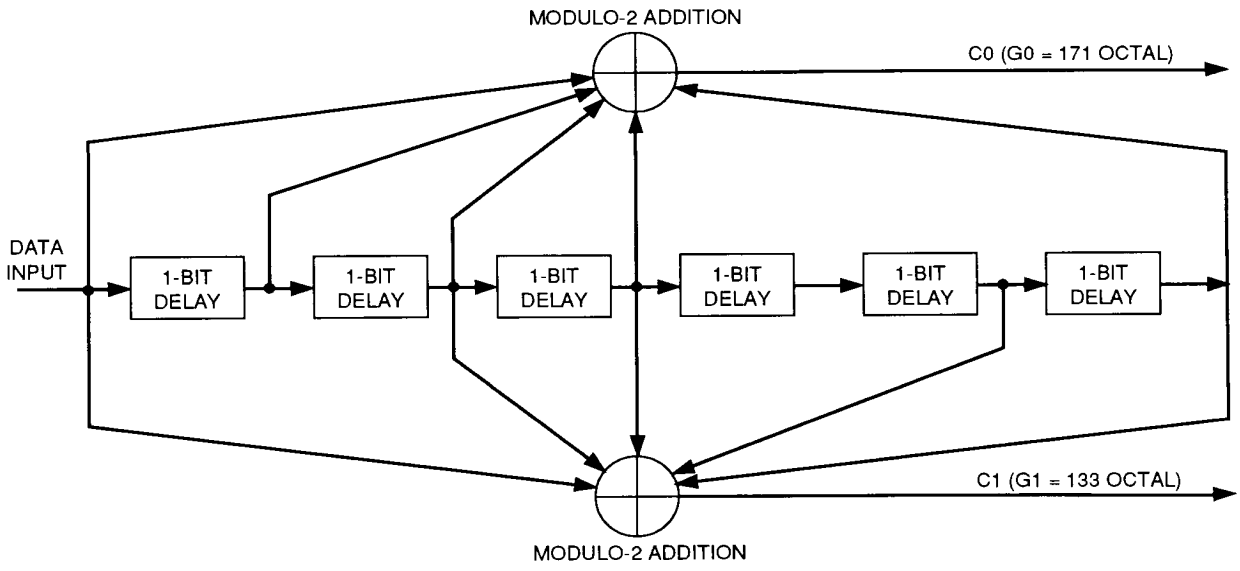


Figure 3. Constraint Length Seven (K=7) Convolutional Encoder

and only correct result are mitigated as the paths within the "chainback" memory converge after some history. The greater the "depth" of the chainback process, the more likely that the final decoded result is error-free. As a result, higher code rates and constraint lengths require longer chainback depth for best performance. The chainback memory in the Viterbi decoder traces the history of the previous states to arrive at the most probable state of the encoder in the past and thus determines the transmitted data.

FUNCTIONAL OVERVIEW

Interfacing

Interfacing with the Q1601 Viterbi Decoder is straightforward. All data inputs are provided to the device synchronously with externally sourced clocks. Data signals are clocked into the device on the rising edge of the decoder clock inputs. Data outputs change on the rising edge of the decoder clock output. The Q1601 decoder requires two externally generated clock inputs, specifically a data rate clock and a channel rate clock. The frequency relationship of these two clocks varies according to data input format (i.e., serial or parallel).

Most control and status information is provided to and from the Q1601 decoder through a bus-oriented processor interface. This interface uses an 8-bit data bus and a 5-bit address bus along with read, write, and chip-select signals to read from status ports and write to control ports in the Q1601 decoder. In addition, the decoder input and output data can be written and read directly using the processor interface. In this mode, the Q1601 device acts as a peripheral for forward error correcting of data processed by a host processor.

Coding Performance

The Q1601 device provides coding performance very near the theoretical limits for the optimal k=7 rate ½ Viterbi decoding algorithm (figure 4). A coding gain of 5.2 dB is achieved when operating at a code rate of ½ and a decoded BER of 10^{-5} with a BPSK or QPSK optimal soft-decision modem.

Monitoring Channel Bit Error Rate

The Q1601 provides two powerful means to monitor the performance of the Viterbi decoder. The first technique monitors the channel BER (i.e., the "symbol error rate"). This monitor works on a re-encode and compare principle (see figure 5). Specifically, if a data stream {A} is first convolutionally encoded to be a data stream {A'} and then Viterbi decoded without errors injected by the transmission channel, the resulting data stream will be the original {A}. If the output data stream of the decoder was re-encoded using the same convolutional encoding algorithm as the original stream, then the encoded stream {A'} is again generated. Delaying the input data stream to the decoder by the exact delay associated with the decoder and re-encoder and then comparing this delayed input with the re-encoded stream on a bit-by-bit basis results in a constant equal comparison if the channel introduces no errors. However, if the channel introduces bit errors to the received data stream {A'}, this bit-by-bit comparison will indicate a miss whenever these channel bit errors occur. The monitor tracks the errors to generate a highly accurate estimate of the channel BER. Of course, the BER monitor also indicates errors when the decoder fails to correct an information bit error. However, the probability of an error occurring in a decoder output bit is at least two orders of magnitude below the probability of a channel error during normal operating conditions. Therefore, the effect of decoder errors on the accuracy of the BER measurement is minimal.

The bit error outputs of the re-encode and compare circuit can be monitored using the on-chip BER monitor circuit (figure 6). The on-chip BER monitor circuit is a flexible and powerful technique for determining the channel error rate. This circuit consists of two accumulators acting as counters. The first accumulator counts decoder input code words (i.e., code word count accumulator). The second accumulator counts code word errors detected by the re-encode and compare circuit (i.e., code word error accumulator). The period of BER measurement is determined by programming the two's complement 24-bit binary value into the code word count accumulator. This value is entered into the Q1601 via the processor interface (write addresses 0A, 0B, and 0CH). The loaded value is multiplied by 1,000, yielding the actual number of code words to be monitored in the BER measurement.

The BER measurement operates whenever the clock signal DECOUTCLK (pin 19) is active (i.e., toggling). During the BER measurement period, the detected errors are accumulated in the code word-error accumulator (also called the BER Measurement Output Register). This 16-bit binary accumulator is reset at the beginning of each BER measurement period. Once the 24-bit period of the BER measurement is entered, the loaded value is activated by writing any value to the "BER Test Value Enable" processor interface port (write address 18 H). The BER

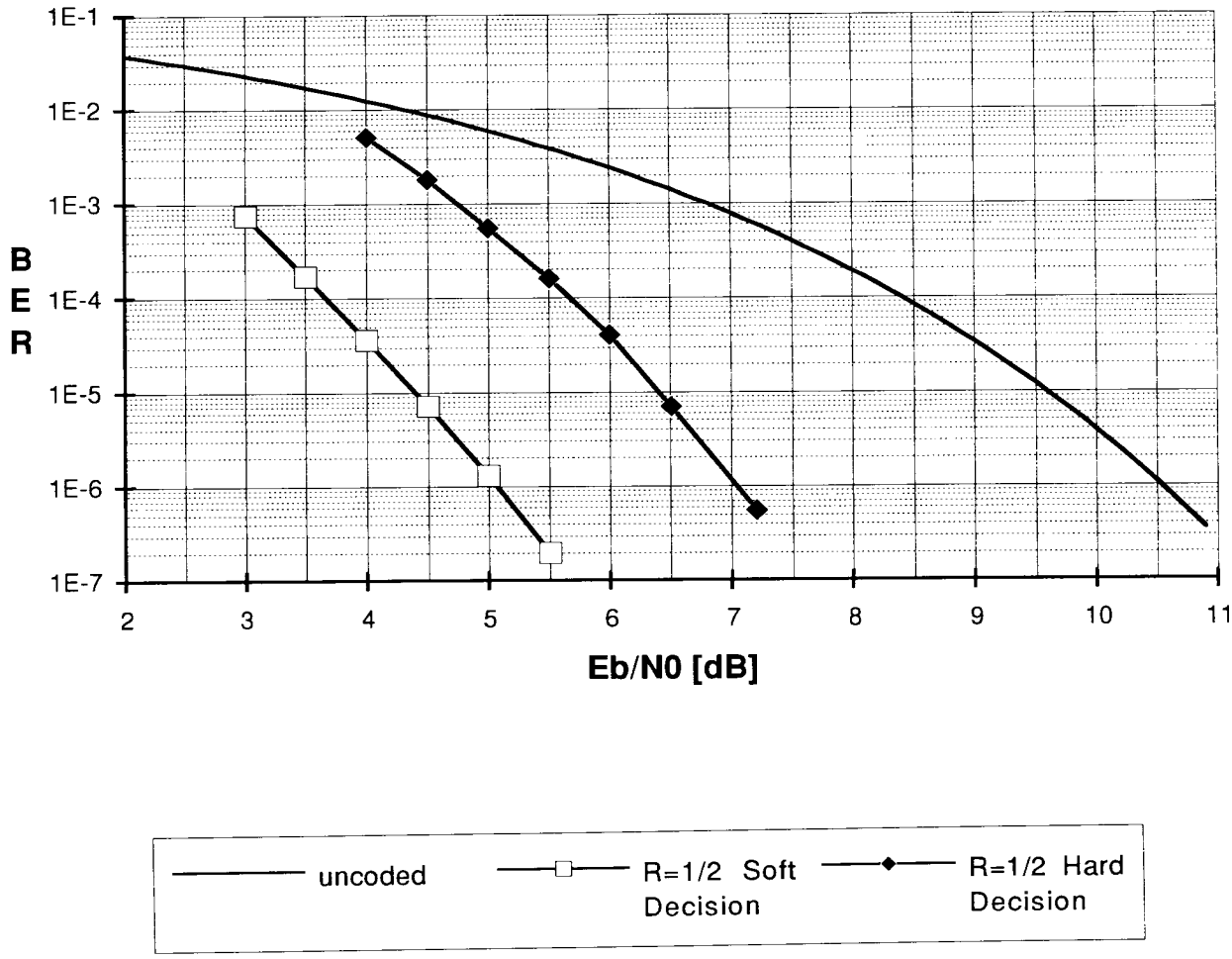


Figure 4. Q1601 Coding Performance

measurement is completed when the code word-count accumulator completes its count. At this point the number of detected code word errors recorded in the code word-error accumulator is transferred to a parallel 16-bit buffer register.

The completion of the BER measurement period is indicated by BERDONE (pin 39), which goes to logic high for two periods of DECOUTCLK (pin 19). The BERDONE signal can be used as an interrupt or polled status bit to a controlling processor. The accumulated error value then can be read via the processor interface. The actual measured bit error count is found from the following formula:

$$\text{Actual Error Count} = (\text{Register Value} - 1)\times 8$$

where "Register Value" is the value read from the 16-bit BER measurement register (read address 03 and 04 H). That is, if no errors are recorded, the BER measurement register will have a value of "1" stored. If the number of errors exceeds the limit of the 16-bit register, the BER measurement will read as "0000H."

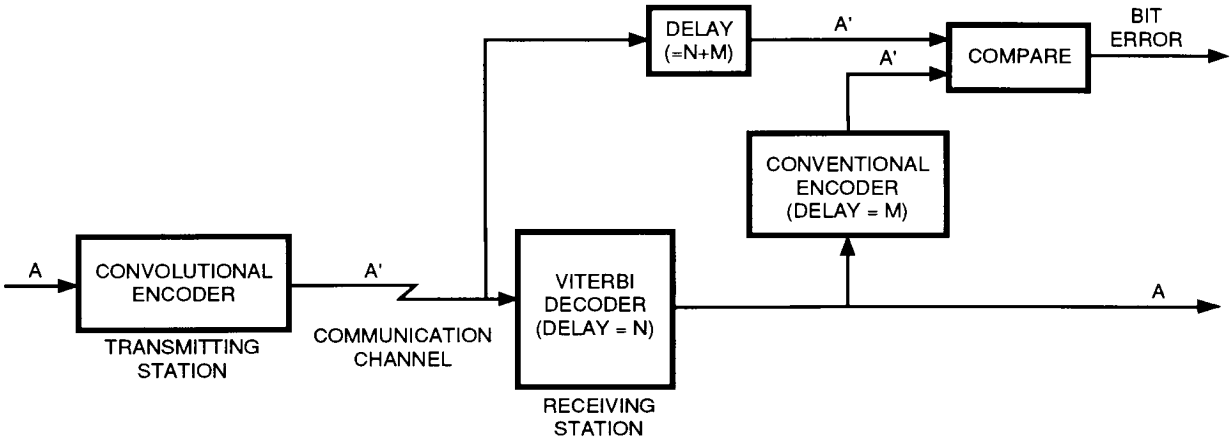


Figure 5. Re-Encode and Compare Circuit

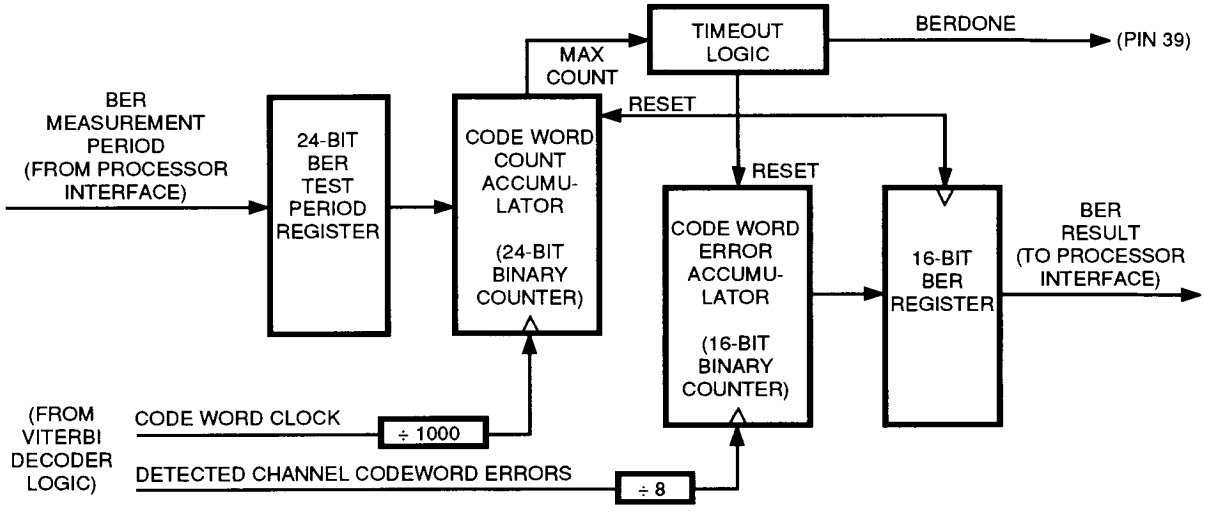


Figure 6. Channel Bit Error Rate Measurement Circuit

The BER test continues running and stores the next test value in the 16-bit BER measurement register upon completion of each test.

The actual symbol BER is computed by dividing the measured error quantity by the number of code words in the test. This measurement division is facilitated if the measurement period is a power of 10, such as 10,000 or 100,000 code words long. In this case, the binary number recorded by the error accumulator is the mantissa of the symbol BER, and the exponent of the BER value is determined by the measurement period. For example, if the test period is set to 100,000 ($= 10^5$) code words and 250 errors are recorded during the measurement period, the measured symbol BER is 2.5×10^{-3}.

In the event that more than 2^{19} code word errors are recorded in the measurement period, the code-word error accumulator saturates at an "all-zeros" value. If this condition is indicated at the completion of a BER measurement, the period of the measurement should be reduced until a value less than saturation is recorded.

For an accurate measurement of the symbol BER, at least 100 errors should be detected within a given test period. If fewer than 100 errors are recorded, the statistical variance of such a measurement will be high. In this case, the measurement period should be increased until more than 100 code word errors are detected during the BER test.

The on-chip BER monitor can be used for measurements other than simply the symbol BER. For example, by setting the measurement period to the code word rate (i.e., code words per second), the test period becomes equal to exactly one second in time. The BER monitor therefore becomes a straightforward means for monitoring error-free seconds, which is frequently a useful error statistic. If no errors are recorded during the one second period this is an error-free second. External hardware or software can record the percentage of error-free seconds for error statistics purposes.

Normalization Rate Monitor Operation (Synchronization Status Monitor)

The second performance monitor built into the Q1601 is the normalization rate monitor. The normalization rate monitor monitors the rate at which the internal state metrics of the Viterbi algorithm increase in value. Rapidly increasing state metric values indicate that the decoder may be out of synchronization with the phase or symbol grouping associated with the input symbols. When all state metrics in the Q1601 Viterbi Decoder reach a certain numeric value, a normalization circuit reduces the value of all metrics by a fixed amount to prevent metric overflow. The Q1601 monitors the rate that these normalizations occur while decoding data. The system designer determines an acceptable normalization rate threshold and programs this threshold into the Q1601 device. The designer controls both the metric normalization monitoring time as well as the number of normalizations allowed during that time. These two numbers, which provide for more than 65,000 possible settings, are programmed into the device using the microprocessor interface.

The on-chip normalization circuit (figure 7) consists of two counters that are similar in operation to the channel BER monitor previously described. The system designer controls the periods of these two counters. The first counter (T) measures the number of decoded bits. The second counter (N) measures the number of state metric normalizations. The normalization rate monitor circuit outputs two signals, OUTOFSYNC and INSYNC. The INSYNC signal indicates that the programmed normalization rate threshold was not exceeded. The OUTOFSYNC signal indicates that the programmed normalization rate threshold was exceeded and suggests a loss of synchronization.

The normalization rate threshold is determined by taking the ratio of the count of normalizations (the N counter) and the time period (the T counter). Each of these 8-bit-wide binary counters is pre-loaded using the processor interface registers.

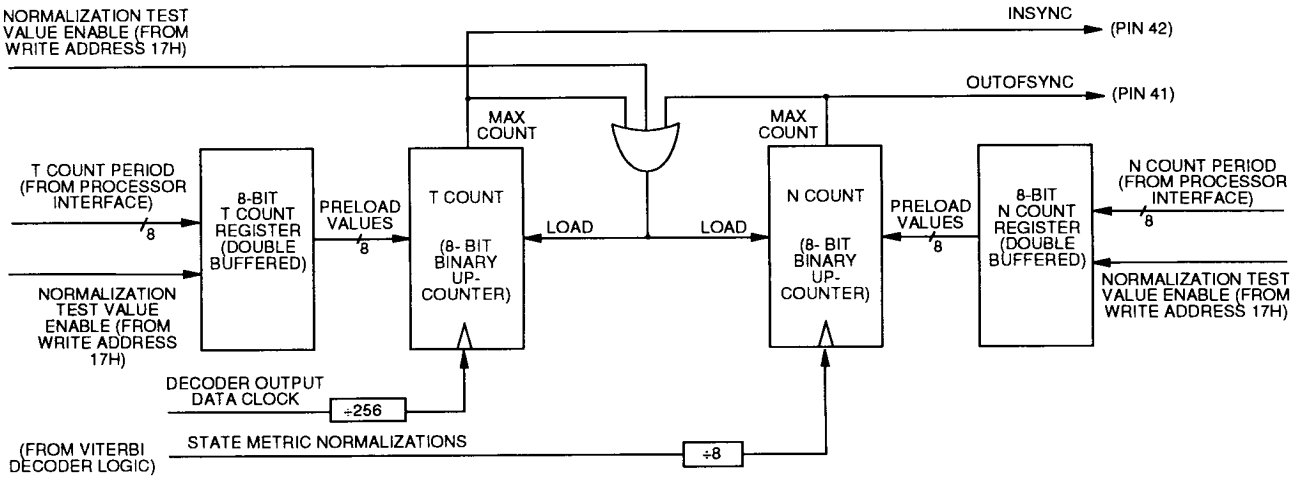


Figure 7. Normalization Rate Monitor Circuit

Both the N and T counters are loaded with binary values that are the two's complement of the actual count value. The count value loaded into the T counter is multiplied by 256 to determine the actual number of decoded bits in the normalization test period. That is:

$$t = 256xT$$

where "t" is the actual number of decoded bits counted and "T" is the two's complement value of the 8-bit number loaded into the T counter (write address 08H).

The actual count of the N counter is determined by the following formula:

$$n = (N-1) \times 8+4$$

where "n" is the actual number of normalizations allowed, and "N" is the two's complement value of the 8-bit number loaded into the N counter (write address 09H). With this programming capability, the system designer selects the normalization rate threshold for determining an in-sync or out-of-sync condition, as well as the period of the measurement. For example, when operating with rate ½ decoding, a normalization rate threshold of about 10% reliably detects a loss of synchronization.

To avoid false detection of synchronization loss due to a noise burst, the normalization measurement should detect at least 20-30 normalizations before declaring a loss of synchronization. As an example, the system designer may specify 50 as the number of normalizations to be detected. By loading the 8-bit two's complement value of seven (i.e., F9H) into the N counter register, the actual number of normalizations allowed in a test period without indicating a loss of synchronization would be $(7-1) \times 8+4 = 52$. The value for the T counter must be approximately ten times the value in the N counter; that is, loading the T counter with the two's complement value of 2 (i.e., FEH) the actual count value for the T counter will be $(2 \times 256) = 512$. Therefore, the actual normalization rate threshold will be $52/512 = 10.2\%$. This is an appropriate threshold for reliable synchronization when operating with rate ½ coding.

Synchronization

The Q1601 Viterbi Decoder can automatically synchronize incoming data streams. Synchronization may require on-chip offsetting for bit and phase alignment, depending on the particular mode of operation of the decoder. The synchronization technique is a two-step process. First, the decoder quality state is constantly monitored using the "state metric normalization rate" circuit described previously. The user programs an "in-sync/out-of-sync" threshold for this internal circuit. The success or failure of this test for each test period is indicated on Q1601 output pins 42 (INSYNC) and 41 (OUTOFSYNC). This synchronization monitor function is operational whenever the decoding function of the Q1601 device is processing data.

The second step of the automatic synchronization process attempts to correct an indicated out-of-sync condition by offsetting the data input to the decoder just prior to the actual decoding process. The particular offsetting technique depends on the specific mode of operation selected. In all cases, the effects of the out-of-sync condition can be compensated for by either a timing re-alignment or a permutation of the decoder input data. Wiring the OUTOFSYNC output pin (pin 41) directly to the SYNCCHNG input pin (pin 12) on the Q1601 device provides a feedback path between the synchronization monitor and the synchronization correction circuit. When an out-of-sync condition is indicated, the input processor switches synchronization states. The synchronization monitor test continues and indicates whether the offsetting action taken by the decoder input processor has corrected the out-of-sync condition.

If an out-of-sync condition is indicated after all possible synchronization states have been attempted, the Q1601 device repeats the process of stepping through all the possible states until the out-of-sync indication is no longer received (i.e., an in-sync condition exists). The particular synchronization state attempted for each operating mode is described below (see Modes of Operation). When automatic synchronization is not required, the SYNCCHNG input should be set to a logic "0."

Decoder Input Data Formats

The Q1601 Viterbi Decoder provides the highest coding gain performance (figure 4) when processing multiple bit "soft-decision" values for the R0 and R1 code words. The optimal soft-decision values are linearly quantized 3-bit values for each code word. Refer to QUALCOMM Application Note AN1650-2, *Setting Soft-Decision Thresholds for Viterbi Decoder Code Words from PSK Modems* for techniques on optimizing the soft decision for demodulator output samples. The

3-bit soft-decision values can be input to the Q1601 decoder inputs (R0 and R1) in either sign-magnitude or offset-binary notation. The encoding of soft-decision values for each of these two formats is given in table 7, Decoder Control Register 2. The selection of the input format is made via the microprocessor interface.

When using the Q1601 Viterbi Decoder with hard-decision (single-bit) values for R0 and R1, the decoder input format should be set to sign-magnitude notation. The Rx[0] "magnitude" bits (R0[0] and R1[0]) should be set to logic "1" (logic high). The Rx[1] "magnitude" bits (R0[1] and R1[1]) should be set to logic "0" (logic low). The hard-decision code word should be input on the "sign" signal pins (R0[2] and R1[2]) as appropriate.

Reset Circuit Operation

A reset operation should be performed when the Q1601 device is initially configured and whenever a change occurs in the mode of operation.

The reset operation can be performed using either the external input pin DECRESET (pin 11) or the reset bit in Decoder Control Register 3 of the processor interface. The operation of external input pins and processor-controlled bits is identical.

When a decoder reset is asserted, either by setting the input pin to logic high or setting the processor interface bit to "1," the reset is latched synchronously into the Q1601 decoder. Both input clocks of the decoder must be operational during reset. The reset operation is edge-triggered, and the actual reset occurs only during the first clock periods after the reset line is asserted. Continuing to hold the reset line or bit to the logic high or "1" condition does not cause a continuous reset.

A reset affects the internal state of the synchronization circuits. Resetting the decoder does not set the internal states of the path memory to a fixed value.

Data Scrambling

The Q1601 Viterbi Decoder includes an on-chip data descrambling circuit that can be enabled or disabled via the processor interface. Data scrambling is used frequently in conjunction with FEC techniques to guarantee minimum transition densities in transmitted signals for purposes such as timing loop synchronization. The Q1601 device implements two versions of a descrambling algorithm specified in CCITT Recommendation V.35. The first version meets the CCITT specification exactly. The second version is a slight modification of the CCITT specification, which complies with a *de facto* scrambling standard used in several leading communications networks, including the INTELSAT Business Services (IBS) and INTELSAT Intermediate Data Rate (IDR) services. The details of these algorithms are described in QUALCOMM Application Note AN1650-1, *Data Scrambling Algorithms Implemented in the Q1650 Viterbi Decoder.* The particular descrambling algorithm is selected via the microprocessor interface.

Data descrambling is performed after Viterbi decoding and differential decoding in the Q1601 (see figure 2).

One system consideration, when designing with the data scrambling feature enabled, is the multiplication of output bit errors from a Viterbi decoder. Error multiplication occurs because data descrambler output bits are affected by several bits input to the descrambler. If a single bit error occurs at the output of a Viterbi decoder, the data descrambler theoretically will generate up to three output errors due to the multi-output influence of the single bit error. In actuality, the error statistics at the output of a Viterbi decoder are such that the error multiplication is reduced to a factor between 1.5 and 2. This equates to a coding gain loss of only about 0.2 to 0.3 dB. This loss is an acceptable tradeoff for the advantages of the data scrambling function in many systems.

Device Throughput Delay

The input-to-output delay through the decoder depends on the selected operating mode. When operating in rate ½ parallel mode, the delay through the decoder is 102½ periods of the DECINCLK clock, which is the same frequency as the DECOUTCLK signal. The throughput delay is the same for operation in both direct and peripheral modes. The delay will increase by one clock period if the data descrambler is enabled.

In the serial data mode, the delay in terms of the input clocks are identical to the parallel data mode. However, the exact relation between the input and output clock phasing increases or decreases the throughput delay by as much as one clock period.

Chainback Memory

The minimum chainback memory of the Q1601 Viterbi Decoder is 48 states. This memory depth achieves near theoretical coding gain of 5.2 dB at 10^{-5} BER.

Direct vs. Peripheral Data Mode Operation

The Q1601 Viterbi Decoder interfaces with data via dedicated signal pins or the processor interface. The direct data mode interfaces with all data via the dedicated pins and is most commonly used with synchronous data channels. The peripheral data mode interfaces with all data signals, including R0 and R1, via processor interface registers. This mode is used when the Q1601 device is used as an error control peripheral to the processor system. When operating in peripheral data mode, the functions of the R0 (pins 24, 22, 15), R1 (pins 23, 18, 14), R0ERASE (pin 26), R1ERASE (pin 25), DECINCLK (pin 9), DECOUTCLK (pin 19), and DECRESET (pin 11) signals are provided by writing to port addresses. In this mode, all of the above pins must be connected to logic "0." The selection of the direct or peripheral data mode is made by setting bit 3 in Decoder Control Register 2 of the processor interface (0 = Direct, 1 = Peripheral).

When the Q1601 device operates in the peripheral mode, each data bit handled by the decoder requires four processing steps. First, the input data to the decoder is written to the appropriate register using the processor interface (see tables 4 through 7). Second, the processor-controlled activation of DECINCLK is performed by writing to the appropriate processor interface address. Third, processor-controlled activation of DECOUTCLK is performed by writing to the appropriate processor interface address. Finally, the output data is read from the appropriate register. This cycle repeats for each bit processed by the Q1601 decoder.

MODES OF OPERATION

The Q1601 Viterbi Decoder supports various user-selected modes and functions. In particular, the Q1601 device can operate in rate ½ parallel mode and rate ½ serial mode. The mode of operation is selected using the processor control registers described in the following sections. All possible combinations of functions and modes are summarized in table 1. Also identified are the internal synchronization techniques used for each mode (when enabled).

Rate ½ Parallel Mode Operation

When operating the Q1601 device in rate ½ parallel mode, two code words (R0 and R1) are input to the decoder for every bit output from the decoder. The R0 and R1 code words are clocked into the decoder during the rising edge of the DECINCLK clock input signal. The R0 input corresponds to the 171 (octal) generating polynomial, while the R1 input corresponds to the 133 (octal) generating polynomial (see figure 3). In this mode, the frequency of DECOUTCLK should equal the frequency of DECINCLK.

When operating with parallel input data, the synchronization states of the decoding function assume operation with a QPSK demodulation system. In these types of systems, the 171 (octal) code word of the rate ½ encoded output is commonly transmitted on the in-phase or quadrature channel of the QPSK modulator, while the 133 (octal) code word is transmitted on the remaining channel. In this case, the synchronization state machine on the Q1601 decoder must resolve one of two possible values. The initial synchronization state, upon device reset, connects the R0 code word inputs to the internal R0 data lines, and the R1 code word inputs to the R1 data lines. This is referred to as the "normal" synchronization state. When the synchronization state of the Q1601 decoder changes due to the assertion of the SYNCCHNG signal, the "alternate" synchronization state occurs in which the R0 code word input is used internally as the R1 code word and vice versa. In addition, this mode inverts the R0 value.

The alternate synchronization state offsets the effects of a 90° phase ambiguity associated with QPSK demodulators. A QPSK demodulator actually can synchronize in one of four phase states. However, two of the four states are related to the other two in that they are inversions of both the R0 and R1 values. The effects of this data inversion can be offset by enabling the on-chip differential decoder circuit on the Q1601 decoder.

Thus, the Q1601 device needs only to differentiate between the "normal" and the "alternate" synchronization states to synchronize to QPSK demodulators as long as the differential decoding function is enabled or some other means is provided by the system to offset the effects of the data inversion.

When operating in rate ½ parallel data mode and offset QPSK (OQPSK) modulation, an additional step is required when in the alternate synchronization state. In this case, the R1 input data is delayed by one period of the DECINCLK signal prior to the "swap and invert" of the alternate synchronization state described for QPSK demodulators. This delay is useful for correcting the time offset of the in-phase (I) and quadrature (Q) channels of the OQPSK system.

Rate 1/2 Serial Mode Operation

When operating the Q1601 device in rate ½ serial mode, all encoded data is clocked into the R0 input pins on the rising edge of DECINCLK. It is necessary to transmit the R0 (171 octal) portion of an encoded pair before the R1 (133 octal) portion. In this mode, the frequency of DECOUTCLK should be one-half the frequency of DECINCLK.

In the rate ½ serial mode, the Q1601 device adjusts for the symbol grouping of the input serial code words. That is, since the two code words for the rate ½ encoded symbol are input one at a time, the Q1601 decoder must group these inputs prior to the actual decoding process. The input signals are grouped (paired) in one of two ways, and only one pairing sequence is correct: pairing the R0 input code word with the next input, which would be the associated R1 code word. When the R0 code word is paired incorrectly with the R1 code word (i.e., pairing the R1 input of an encoded symbol with the next input, which would be the R0 code word from the next symbol), the automatic synchronization circuit will detect the incorrect alignment. When this happens, the assertion of the SYNCCHNG signal will adjust the input stream by stopping the input grouping circuit for one period of the DECINCLK signal. This will correctly pair the code words.

In the serial mode, the ROACTIVE/ signal can be used to specify the explicit location of the R0 input. That is, setting the ROACTIVE/ input to logic "0" during the DECINCLK clock period that an input code word is received will force the decoder to treat this code word as the R0 code word.

CONFIGURATION EXAMPLES

Rate 1/2 Parallel Mode Example

In a typical configuration of the Q1601 Viterbi Decoder for QPSK modulation (figure 8), the I and Q demodulator outputs each are quantized by a 3-bit analog-to-digital (ADC) converter to generate the R0 and R1 soft-decision inputs. In this configuration, DECINCLK and DECOUTCLK are the same frequency and should be connected together.

The Q1601 decoder is programmed for rate 1/2 parallel operation by writing to the processor interface. An example initialization sequence is shown in table 2.

Rate 1/2 Serial Mode Example

In a typical configuration of the Q1601 Viterbi Decoder for BPSK modulation (figure 9), the demodulator output is quantized by a 3-bit ADC to generate the R0 soft-decision input. In this configuration, DECOUTCLK is one-half the frequency of DECINCLK.

The Q1601 device is programmed for rate 1/2 serial mode operation by writing to the processor interface. An example initialization sequence is shown in table 3.

Rate 1/2 Encoder

The Q1601 is intended for low-cost, high-volume receiver applications. Therefore, no encoder is provided on the Q1601. The design of a rate 1/2 k=7 convolutional encoder that uses the 171 (octal) and 133 (octal) generating polynomials, can be implemented using several EX-OR gates and six D flip-flops (figure 10). The use of a programmable logic device (PLD) would make it possible to include the entire encoder design on a single device. Applications which require both an encoder and a decoder in a single package can use the Q0256 (less than 800 kbps) or the Q1650 Viterbi decoder.

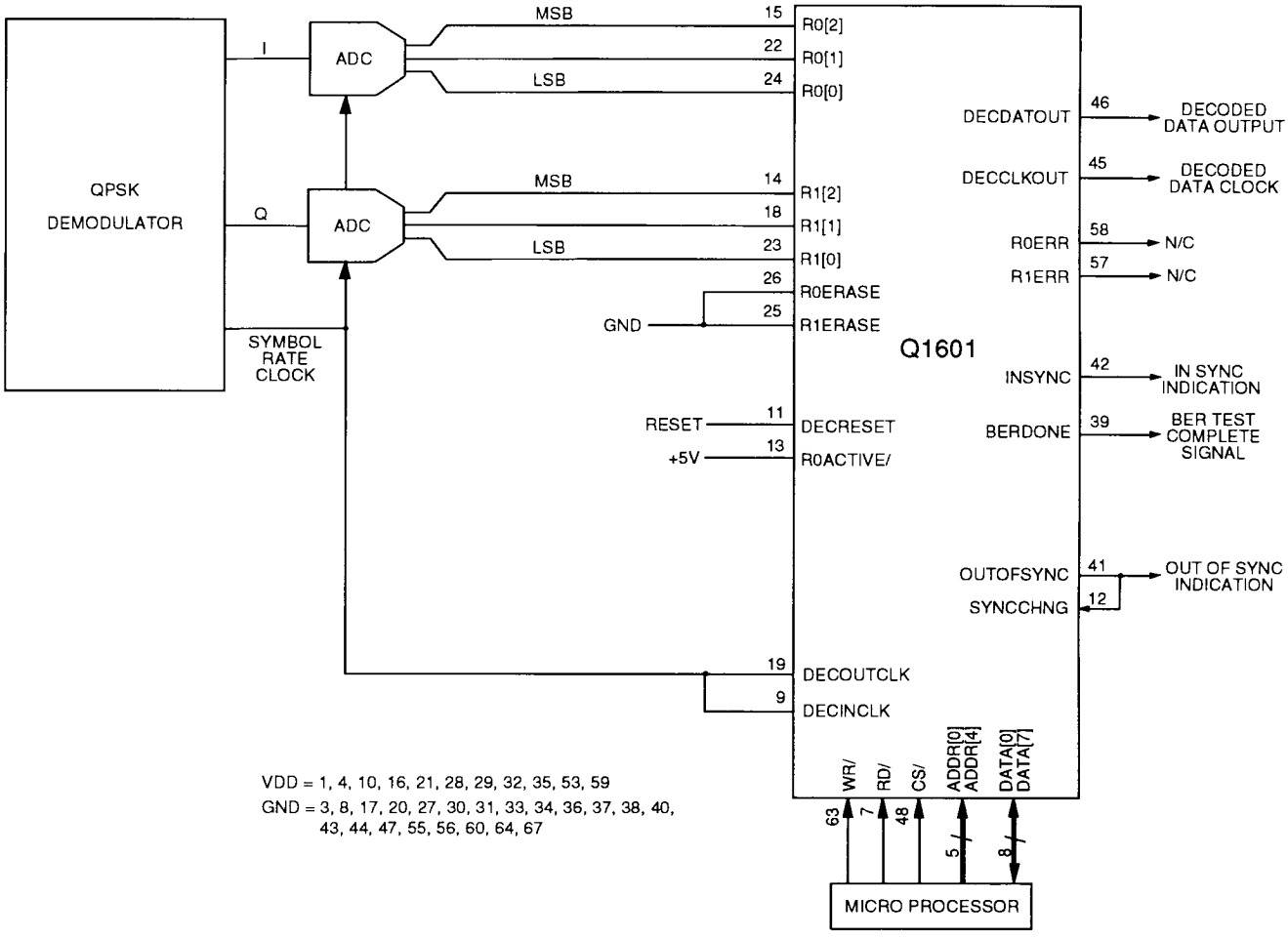


Figure 8. Rate 1/2 Parallel Mode Configuration Example

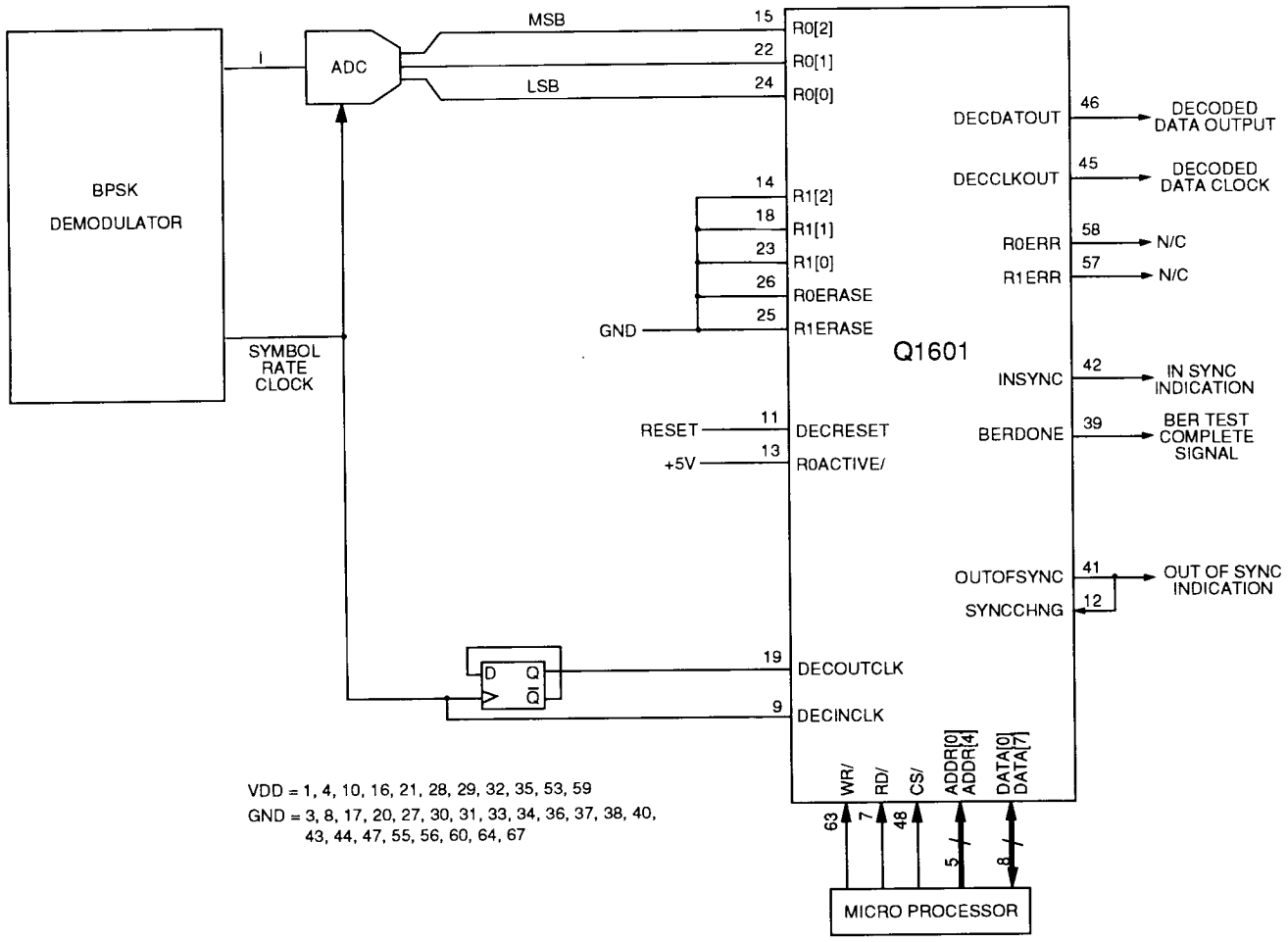


Figure 9. Rate 1/2 Serial Mode Configuration Example

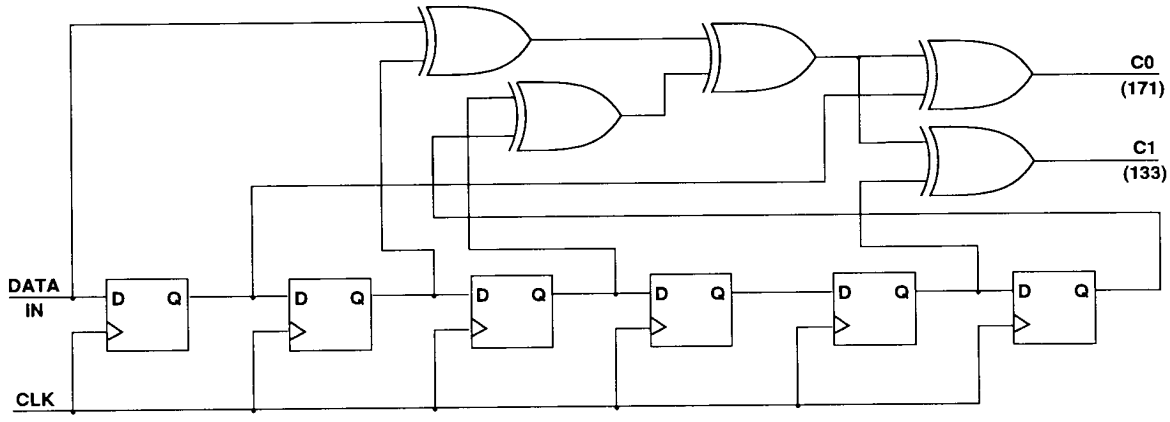


Figure 10. Rate 1/2 Encoder Schematic

Table 1. Q1601 Modes of Operation

			Control Register Bits				Notes	
Code Rate	Data Mode	Modulation	SERIAL ENABLE	OQPSK	PHASE SYNC	SWAP ERASE	Internal Synchronization Methods	Erase Bit Sync
1/2	Ser	BPSK	1	–	–	0	1	N/A
1/2	Par	QPSK	0	0	0	0	2	A
			0	0	0	1	2	B
			0	0	1	0	3	A
			0	0	1	1	3	B
1/2	Par	OQPSK	0	1	0	0	4	A
			0	1	0	1	4	C
			0	1	1	0	5	A
			0	1	1	1	5	C

NOTES

Internal Synchronization Methods

1. Shifts input grouping pattern by one code word.
2. Edge actuation of SYNCCHNG signal toggles between alternate decoder input mapping states:
   State 1: $R0_N$ -->$R0_N$, $R1_N$--> $R1_N$
   State 2: $R0_N$ -->$R1_N$/, $R1_N$--> $R0_N$
3. Level activation of SYNCCHNG signal forces one of two decoder input mapping states:
   State 1 (SYNCCHNG = 0): $R0_N$ –>$R0_N$, $R1_N$--> $R1_N$
   State 2 (SYNCCHNG = 1): $R0_N$ –>$R1_N$/, $R1_N$--> $R0_N$
4. Edge actuation of SYNCCHNG signal toggles one of two decoder input mapping states:
   State 1: $R0_N$ -->$R0_N$, $R1_N$--> $R1_N$
   State 2: $R0_N$ -->$R1_N$/, $R1_{N-1}$--> $R0_N$
5. Level actuation of SYNCCHNG signal forces one of two decoder input mapping states:
   State 1 (SYNCCHNG = 0): $R0_N$ –>$R0_N$, $R1_N$--> $R1_N$
   State 2 (SYNCCHNG = 1): $R0_N$ –>$R1_N$/, $R1_{N-1}$--> $R0_N$

Erase Bit Synchronization

A. R0ERASE and R1ERASE inputs follow R0 and R1 data signal synchronization methods.
B. R0ERASE and R1ERASE inputs do not follow R0 and R1 data signal synchronization methods.
C. R0ERASE input is not affected by synchronization methods. R1ERASE is delayed by one input code word when in synchronization state 2.

Table 2. Q1601 Rate 1/2 Parallel Mode Initialization Example

Step	Register Name	Address	Value	Comments
1	Reserved Register	15H	00H	Reserved register must be set to 0 for correct operation.
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	04H	Parallel mode, QPSK demodulator
4	Decoder Control Register 2	03H	01H	Sign-magnitude, direct data mode, no differential decoder, no descrambler
5	Decoder Control Register 3	04H	00H	Clear reset bit
6	Decoder Control Register 3	04H	04H	Set reset bit (resets decoder)
7	Decoder Control Register 3	04H	00H	Clear reset bit*
8	Normalization Test Bit-Count Input Register	08H	FEH	T count - Threshold set for 10% (See *Normalization Rate Monitor Operation*)
9	Normalization Test Normalize-Count Input Register	09H	F9H	N count - Threshold set for 10% (See *Normalization Rate Monitor Operation*)
10	BER Period Input Register LS Byte	0AH	FCH	LS byte of 24-bit value of period of on-going chip BER monitor (Example period is 4000 symbols.)
11	BER Period Input Register CS Byte	0BH	FFH	CS byte of 24-bit value of period of on-chip BER monitor
12	BER Period Input Register MS Byte	0CH	FFH	MS byte of 24-bit value of period of on-chip BER monitor
13	Normalization Test Value-Enable Register	17H	00H	A write of any value to this register begins the normalization test.
14	BER Test Value-Enable Register	18H	00H	A write of any value to this register begins the BER test.

* After a minimum of 2 DECINCLK=DECOUTCLK clock periods.

Table 3. Q1601 Rate 1/2 Serial Mode Initialization Example

Step	Register Name	Address	Value	Comments
1	Reserved Register	15H	00H	Reserved register must be set to 0 for correct operation.
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	05H	Serial mode, BPSK demodulator
4	Decoder Control Register 2	03H	01H	Sign-magnitude, direct data mode, no differential decoder, no descrambler
5	Decoder Control Register 3	04H	00H	Clear reset bit
6	Decoder Control Register 3	04H	04H	Set reset bit (resets decoder)
7	Decoder Control Register 3	04H	00H	Clear reset bit*
8	Normalization Test Bit-Count Input Register	08H	FEH	T count - Threshold set for 10% (See *Normalization Rate Monitor Operation*)
9	Normalization Test Normalize-Count Input Register	09H	F9H	N count - Threshold set for 10% (See *Normalization Rate Monitor Operation*)
10	BER Period Input Register LS Byte	0AH	FCH	LS byte of 24-bit value of period of on-going chip BER monitor (Example period is 4000 symbols.)
11	BER Period Input Register CS Byte	0BH	FFH	CS byte of 24-bit value of period of on-chip BER monitor
12	BER Period Input Register MS Byte	0CH	FFH	MS byte of 24-bit value of period of on-chip BER monitor
13	Normalization Test Value-Enable Register	17H	00H	A write of any value to this register begins the normalization test.
14	BER Test Value-Enable Register	18H	00H	A write of any value to this register begins the BER test.

* After a minimum of 2 DECINCLK=DECOUTCLK clock periods.

TECHNICAL SPECIFICATIONS

Processor Interface

The on-chip processor interface of the Q1601 Viterbi Decoder allows a processor to set the operational mode and monitor the internal status of the device. The interface includes an 8-bit-wide data bus, a 5-bit-wide address bus, and read-enable, write-enable, and chip-select lines. This interface operates with most major microprocessor and signal processor families without wait state logic. It can also be used to write and read data to and from the decoder function. In this mode, the Q1601 device operates as a single-chip FEC peripheral to the processor system.

The Q1601 processor interface has 3 read registers (tables 4 and 6) and 15 write registers (tables 5 and 7). Not all registers are required in every operational mode.

Table 4. Q1601 Read Registers Memory Map

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
		Decoder Data Output Register							
00	00	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	R1ERR	R0ERR	DECDAT-OUT
		BER Measurement LS Byte Output Register							
03	03	Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
		BER Measurement MS Byte Output Register							
04	04	Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)

Table 5. Q1601 Write Registers Memory Map

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
		Decoder Data Input Register 1							
00	00	R0-ERASE	R0[2]	R0[1]	R0[0]	R1-ERASE	R1[2]	R1[1]	R1[0]
		Decoder Control Register 1							
02	02	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 1	OQPSK	MODE SELECT
		Decoder Control Register 2							
03	03	Set to 0	DESCR MODE	DESCR ENABLE	DIFF DEC ENABLE	PERIPR/ DIRECT	SWAP ERASE	PHASE SYNC	SMG/OBN
		Decoder Control Register 3							
04	04	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	S/W DEC RESET	Set to 0	Set to 0
		Normalization Test Bit-Count Input Register							
08	08	TCOUNT Bit 7 (MS)	TCOUNT Bit 6	TCOUNT Bit 5	TCOUNT Bit 4	TCOUNT Bit 3	TCOUNT Bit 2	TCOUNT Bit 1	TCOUNT Bit 0 (LS)
		Normalization Test Normalize-Count Input Register							
09	09	NCOUNT Bit 7 (MS)	NCOUNT Bit 6	NCOUNT Bit 5	NCOUNT Bit 4	NCOUNT Bit 3	NCOUNT Bit 2	NCOUNT Bit 1	NCOUNT Bit 0 (LS)
		BER Period Input Register LS Byte							
10	0A	BERPER Bit 7	BERPER Bit 6	BERPER Bit 5	BERPER Bit 4	BERPER Bit 3	BERPER Bit 2	BERPER Bit 1	BERPER Bit 0 (LS)
		BER Period Input Register CS Byte							
11	0B	BERPER Bit 15	BERPER Bit 14	BERPER Bit 13	BERPER Bit 12	BERPER Bit 11	BERPER Bit 10	BERPER Bit 9	BERPER Bit 8
		BER Period Input Register MS Byte							
12	0C	BERPER Bit 23 (MS)	BERPER Bit 22	BERPER Bit 21	BERPER Bit 20	BERPER Bit 19	BERPER Bit 18	BERPER Bit 17	BERPER Bit 16
		Processor Decoder Input Clock Register							
14	0E	DECINCLK Bit 7	DECINCLK Bit 6	DECINCLK Bit 5	DECINCLK Bit 4	DECINCLK Bit 3	DECINCLK Bit 2	DECINCLK Bit 1	DECINCLK Bit 0
		Processor Decoder Output Clock Register							
15	0F	DECOUT-CLK Bit 7	DECOUT-CLK Bit 6	DECOUT-CLK Bit 5	DECOUT-CLK Bit 4	DECOUT-CLK Bit 3	DECOUT-CLK Bit 2	DECOUT-CLK Bit 1	DECOUT-CLK Bit 0

Table 5. Q1601 Write Registers Memory Map (Continued)

ADDRESS DEC	ADDRESS HEX	DATA BITS D7	D6	D5	D4	D3	D2	D1	D0
		Reserved Register							
21	15	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
		Reserved Register							
22	16	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
		Normalization Test Value-Enable Register							
23	17	NTVE Bit 7	NTVE Bit 6	NTVE Bit 5	NTVE Bit 4	NTVE Bit 3	NTVE Bit 2	NTVE Bit 1	NTVE Bit 0
		BER Test Value-Enable Register							
24	18	BERTVE Bit 7	BERTVE Bit 6	BERTVE Bit 5	BERTVE Bit 4	BERTVE Bit 3	BERTVE Bit 2	BERTVE Bit 1	BERTVE Bit 0

NOTES
1. Write registers 0Dh, 10h, 13h, and 14h are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to zero or one for proper operation.
3. **Reserved write registers 15h and 16h must be set to 0 for correct operation.**

Table 6. Q1601 Read Registers

READ ADDRESS 00H: DECODER DATA OUTPUT REGISTER

Bit	Name	Function	Same Function as Input Pin
0	DECDATOUT	Decoder data output	46
1	R0ERR	Bit-by-bit indication of detected channel bit errors for R0	58
2	R1ERR	Bit-by-bit indication of detected channel bit errors for R1	57
3-7	–	Reserved –	

READ ADDRESS 03H: BER MEASUREMENT LS BYTE OUTPUT REGISTER

Bit	Name	Function
0-7	BER LS BYTE	Least significant 8 bits of the 16-bit result of the internal bit error rate measurement. Bit 0 is LSB.

READ ADDRESS 04H: BER MEASUREMENT MS BYTE OUTPUT REGISTER

Bit	Name	Function
0-7	BER MS BYTE	Most significant 8 bits of the 16-bit result of the internal bit error rate measurement. Bit 0 is LSB.

Table 7. Q1601 Write Registers

WRITE ADDRESS 00H: DECODER DATA INPUT REGISTER 1

Bit	Name	Control/Input	Same Function as Input Pin
0	R1[0]	LSB of decoder R1 input symbol	23
1	R1[1]	CSB of decoder R1 input symbol	18
2	R1[2]	MSB of decoder R1 input symbol	14
3	R1ERASE	1 erases the R1 symbol	25
4	R0[0]	LSB of decoder R0 input symbol	24
5	R0[1]	CSB of decoder R0 input symbol	22
6	R0[2]	MSB of decoder R0 input symbol	15
7	R0ERASE	1 erases the R0 symbol	26

WRITE ADDRESS 02H: DECODER CONTROL REGISTER 1

Bit	Name	Function
0	Decoder Input Mode Selection	1 puts the decoder in serial data input mode. 0 puts the decoder in parallel data input mode.
1	OQPSK	If: Decoder set to parallel data mode Phase sync enabled Then: 1 makes sync circuit adjust for phase ambiguities of OQPSK demodulators. 0 makes sync circuit adjust for phase ambiguities of QPSK demodulators.
2	–	Set to 1
3-7	–	Set to 0

Table 7. Q1601 Write Registers (Continued)

WRITE ADDRESS 03H: DECODER CONTROL REGISTER 2

Bit	Name	Function
0	SMG/OBN	0 makes the decoder accept offset-binary notation soft-decision inputs at R0 and R1. 1 makes the decoder accept sign-magnitude notation soft-decision inputs at R0 and R1. The following table describes the offset-binary and sign-magnitude data input encoding formats for the soft-decision decoder.

	Encoding Format					
	Offset-Binary			Sign-Magnitude		
R0[x] or R1[x] Bit:	[2]	[1]	[0]	[2]	[1]	[0]
Strongest 1:	1	1	1	1	1	1
	1	1	0	1	1	0
	1	0	1	1	0	1
Weakest 1:	1	0	0	1	0	0
Weakest 0:	0	1	1	0	0	0
	0	1	0	0	0	1
	0	0	1	0	1	0
Strongest 0:	0	0	0	0	1	1

1	PHASE SYNC ENA	If: Decoder set to parallel mode Then: 0 causes the decoder sync state to toggle on every rising edge of SYNCCHNG. 1 causes the sync state to toggle depending on the input to SYNCCHNG (level triggered). If SYNCCHNG is 0, the decoder will be in the normal state. When SYNCCHNG is 1, the decoder is in the swap and invert state. (Phase ambiguity automatic synchronization makes the decoder's automatic synchronization circuits perform symbol "swap-and-invert" operations to synchronize to the PSK phase ambiguities.)
2	SWAP ERASE ENA	If: PHASE SYNC ENA enabled, parallel data input, and external symbol erasure Then: 1 internally "swaps" R0ERASE and R1ERASE with the R0 and R1 data. 0 disables "swapping" input signals R0ERASE and R1ERASE with the data.
3	DECODER PERIPHERAL/ DIRECT DATA MODE	1 makes decoder use processor bus interface for data input/output (peripheral mode). See *Processor Bus Interface Pins* section of *Q1601 Pin Functions* (table 8). 0 makes decoder use dedicated I/O pins for data input/output (direct data mode). See *Decoder I/O Pins* in *Q1601 Pin Functions* (table 8). Signals affected: R0[0-2], R1[0-2], R0ERASE, R1ERASE, and DECDATOUT
4	DIFF DEC ENA	1 enables the differential decoder; 0 disables the differential decoder. (The setting of this bit does not affect the operation of the differential encoder.)
5	DESCRAMB ENA	1 enables the V.35 data descrambler; 0 disables the V.35 data descrambler. (The setting of this bit does not affect the operation of the V.35 data scrambler.)
6	DESCRAMB MODE	If: V.35 data descrambler enabled Then: 1 makes the data descrambler use the exact algorithm specified by CCITT V.35. 0 makes the data descrambler use a slightly modified CCITT algorithm preferred by most systems, including INTELSAT. (See QUALCOMM Application Note AN1650-1.)
7	–	Set to 0

Table 7. Q1601 Write Registers (Continued)

WRITE ADDRESS 04H: DECODER CONTROL REGISTER 3

0-1	–	Set to 0
2	S/W DECODER RESET	A transition from 0 to 1 resets decoder functions (similar to pin 11). Connect pin 11 to logic 0 when using this software-controlled reset. Bit 2 should be set to 0 when using the DECRESET pin.
3-7	–	Set to 0

WRITE ADDRESS 08H: NORMALIZATION TEST BIT-COUNT INPUT REGISTER

Bit	Name	Function
0-7	T COUNT (Bit 0 is LSB)	Determines the length of the synchronization monitor test; requires an 8-bit value. See *Normalization Rate Monitor Operation* for more information.

WRITE ADDRESS 09H: NORMALIZATION TEST NORMALIZE-COUNT INPUT REGISTER

Bit	Name	Function
0-7	N COUNT (Bit 0 is LSB)	Determines the normalization threshold level for the synchronization monitor test; requires an 8-bit value. See *Normalization Rate Monitor Operation* for more information.

WRITE ADDRESS 0AH: BER PERIOD INPUT REGISTER LS BYTE

Bit	Name	Function: Determines BER Period
0-7	BER PERIOD LS Byte (Bit 0 is LSB.)	LS byte of 24-bit (three byte) value of period of on-chip BER monitor. See *Monitoring Channel Bit Error Rate* for more information.

WRITE ADDRESS 0BH: BER PERIOD INPUT REGISTER CS BYTE

Bit	Name	Function: Determines BER Period
0-7	BER PERIOD CS Byte (Bit 0 is LSB.)	CS byte of 24-bit (three byte) value of period of on-chip BER monitor. See *Monitoring Channel Bit Error Rate* for more information.

WRITE ADDRESS 0CH: BER PERIOD INPUT REGISTER MS BYTE

Bit	Name	Function: Determines BER Period
0-7	BER PERIOD MS Byte (Bit 0 is LSB.)	MS byte of 24-bit (three byte) value of period of on-chip BER monitor. See *Monitoring Channel Bit Error Rate* for more information.

WRITE ADDRESS 0EH: PROCESSOR DECODER INPUT CLOCK REGISTER

Bit	Name	Function
0-7	DECINCLK (software-controlled)	Generates (when given any value) a single DECINCLK clock cycle. Connect pin 9 (DECINCLK) to logic 0 when using this software-controlled clock.

Table 7. Q1601 Write Registers (Continued)

WRITE ADDRESS 0FH: PROCESSOR DECODER OUTPUT CLOCK REGISTER

Bit	Name	Function
0-7	DECOUTCLK (software-controlled)	Generates (when given any value) a single DECOUTCLK clock cycle. Connect pin 19 (DECOUTCLK) to logic 0 when using this software-controlled clock.

WRITE ADDRESS 17H: NORMALIZATION TEST VALUE-ENABLE REGISTER

Bit	Name	Function
0-7	Norm Test Values Enable (software-controlled)	Performs two functions (when given any value): 1) Enables the values previously loaded into these registers: Normalization Test Bit-Count Register (write address 08H) Normalization Test Normalize-Count Register (write address 09H) 2) Restarts the normalization rate test

WRITE ADDRESS 18H: BER TEST VALUE-ENABLE REGISTER

Bit	Name	Function
0-7	BER Test Values Enable (software-controlled)	Performs two functions (when given any value): 1) Enables the value previously loaded into the BER Period Register (three bytes–write addresses 0Ah, 0Bh 0Ch) 2) Restarts the BER test

NOTES
1. Write registers 0Dh, 10h, 13h, and 14h are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to zero or one for proper operation.
3. **Reserved write registers 15h and 16h must be set to 0 for correct operation.**

Pin Descriptions

This section describes the functions and operations of the input and output pins of the Q1601 Viterbi Decoder. Figure 11 shows the locations of the pins; table 8 describes the function of each pin.

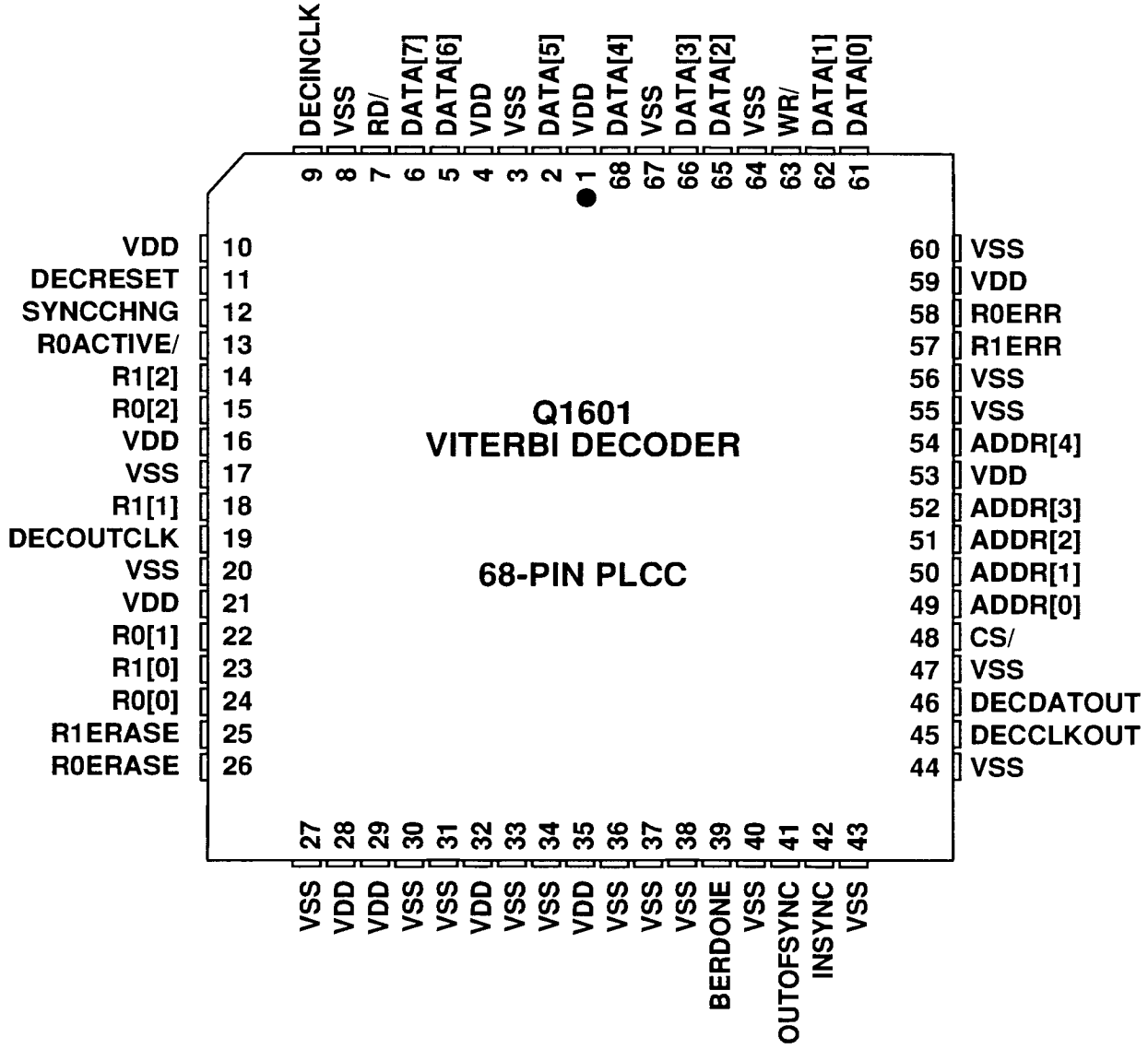


Figure 11. Q1601 Pinout Diagram

Table 8. Q1601 Pin Functions

	Name	Pin	Type	Function
Decoder I/O Pins	R0[0], R0[1], R0[2]	24 (LSB), 22, 15	Input	Decoder R0 input symbol (Note 1)
	R1[0], R1[1], R1[2]	23 (LSB), 18, 14	Input	Decoder R1 input symbol (Note 1)
	R0ACTIVE/	13	Input	Low selects R0 as input (Note 2)
	R0ERASE	26	Input	High erases R0 symbol (Note 7)
	R1ERASE	25	Input	High erases R1 symbol (Note 7)
	DECINCLK	9	Input	Decoder symbol input clock
	DECOUTCLK	19	Input	Decoder data output clock
	DECCLKOUT	45	Output	Decoder data clock output
	DECRESET	11	Input	High master resets decoder circuitry
	SYNCCHNG	12	Input	Decoder sync change control (active high)
	OUTOFSYNC	41	Output	Sync monitor test failure (Note 3)
	INSYNC	42	Output	Sync monitor test pass (Note 4)
	DECDATOUT	46	Output	Decoder data output
	R0ERR	58	Output	Indicates channel bit errors of R0 (Note 5)
	R1ERR	57	Output	Indicates channel bit errors of R1 (Note 5)
Processor Bus Interface Pins	DATA[0]–DATA[7]	61, 62, 65, 66, 68, 2, 5, 6	I/O	Processor interface data bus (DATA[0] is LSB)
	ADDR[0]–ADDR[4]	49 (LSB) , 50, 51, 52, 54	Input	Processor interface address bus
	WR/	63	Input	Processor interface write strobe (active low)
	RD/	7	Input	Processor interface read strobe (active low)
	CS/	48	Input	Processor interface chip select (active low)
	BERDONE	39	Output	BER test indicator (Note 6)
Voltage Supply Pins	VDD (+5V)	1, 4, 10, 16, 21, 28, 29, 32, 35, 53, 59	Power	
	VSS	3, 8, 17, 20, 27, 30, 31, 33, 34, 36, 37, 38, 40, 43, 44, 47, 55, 56, 60, 64, 67	Ground	

NOTES

1. In serial mode, pins 24, 22, and 15 serve as the decoder inputs for all input symbols. Pins 23, 18, and 14 should be connected to VSS.
2. In serial mode, a low on pin 13 indicates that the symbol at R0 is the current decoder input symbol.
3. Pin 41 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test fails.
4. Pin 42 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test passes.
5. Pins 58 and 57 indicate channel bit errors bit-by-bit for R0 and R1, respectively (active high for one period of DECCLKOUT).
6. Pin 39 indicates completion of internal BER measurement test (active high).
7. The R0ERASE (pin 26) and R1ERASE (pin 25) erase inputs must be connected to logic 0 when symbol erasures are not being used.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-65	+150	°C
Operating Temperature	T_A	0	+70	°C
Junction Temperature	T_J		+150	°C
Voltage on any Input Pin		-0.3	Vdd+0.3	V
Voltage on Vdd and on any Output Pin		-0.3	+7.0	V
DC Input Current	I_{IN}	-10	+10	µA

NOTES: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

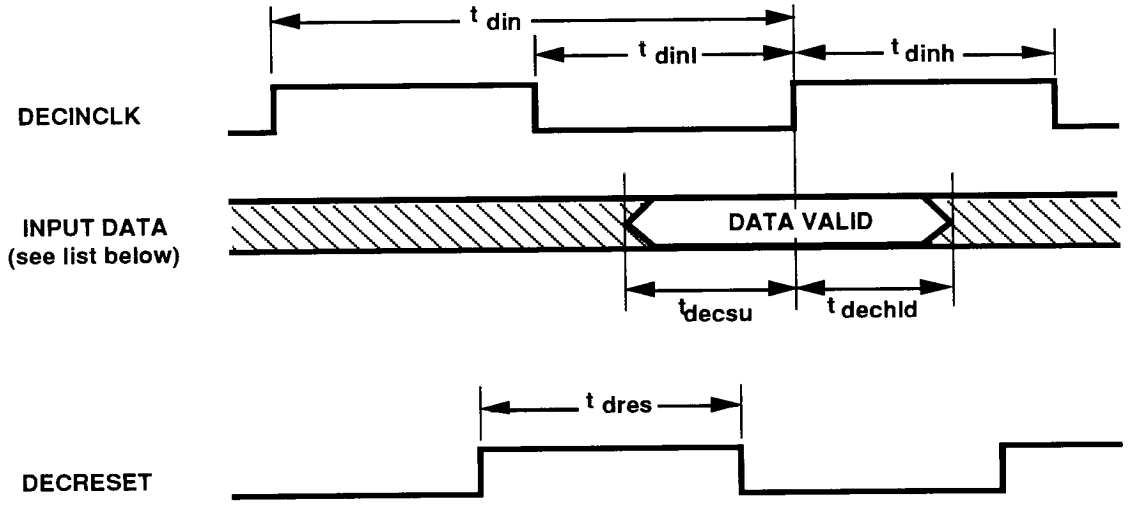
DC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Units	Conditions
Supply Voltage	V_{DD}	4.75	–	5.25	V	
High-Level Input Voltage	V_{IH}	2.0	–	Vdd+0.3	V	
Low-Level Input Voltage	V_{IL}	-0.3	–	0.8	V	
Input Leakage Current	I_{IL}	-1.0	–	–	µA	V_{IN} = 0V, V_{DD} = $V_{DD(MAX)}$
Input Leakage Current	I_{IH}	–	–	1.0	µA	V_{IN} = V_{DD} = $V_{DD(MAX)}$
High-Level Output Voltage (1)	V_{OH}	V_{DD}-1.0	–	–	V	I_{OH} = -16 mA
Low-Level Output Voltage (1)	V_{OL}	–	–	0.4	V	I_{OL} = 16 mA
High-Level Output Voltage (2)	V_{OH}	V_{DD}-1.0	–	–	V	I_{OH} = -8 mA
Low-Level Output Voltage (2)	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
High-Level Output Voltage (3)	V_{OH}	V_{DD}-1.0		–	V	I_{OH} = -1.6 mA
Low-Level Output Voltage (3)	V_{OL}	–		0.4	V	I_{OL} = 1.6 mA
Output Short Circuit Current (4)	I_{OS}	–		300	mA	
Output Capacitance	C_{OUT}			10	pF	
Power Dissipation (Quiescent)	P_D	–	0.1	TBD	W	
Power Dissipation (@10 MHz)	P_D	–	0.8	TBD	W	

NOTES
1. For DECCLKOUT, DECDATOUT, ROERR, RIERR, and DATA[0-7] outputs.
2. For BERDONE, INSYNC, and OUTOFSYNC outputs.
3. For all other outputs.
4. Not more than one output shorted at a time for less than one second.

Timing

Decoder Data Input Timing

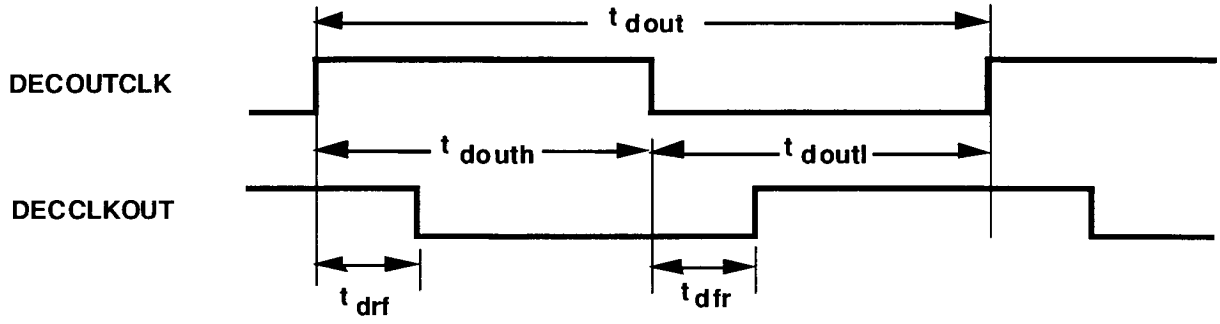


Input data includes: R0[0] R0[1] R0[2] R0ERASE R0ACTIVE/
R1[0] R1[1] R1[2] R1ERASE SYNCCHNG

		Q1601C-10N		
Signal	**Description**	**Min**	**Max**	**Units**
DECINCLK	Max Frequency (=1/tdin)	–	20*	MHz
tdin	Minimum period	50**	–	ns
tdecsu	Data setup to DECINCLK rise	10	–	ns
tdechld	Data hold after DECINCLK rise	5	–	ns
tdinl	DECINCLK low period	15	–	ns
tdinh	DECINCLK high period	15	–	ns
tdres	Minimum reset period	***	–	ns

NOTES
* Maximum frequency for rate 1/2 serial mode.
** Minimum period for rate 1/2 serial mode.
*** The minimum value is 2•DCLK$_{MAX}$, where DCLK$_{MAX}$ = the period of DECINCLK or DECOUTCLK, whichever is greater.

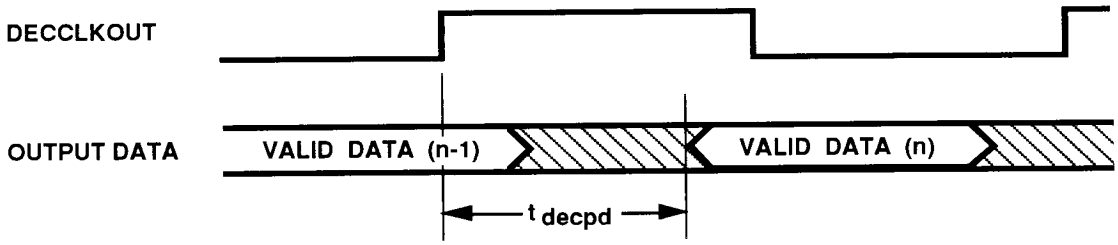
Decoder Clock Timing



		Q1601C-10N		
Signal	**Description**	**Min**	**Max**	**Units**
DECOUTCLK	Max Frequency (=1/tdout)	–	10	MHz
tdout	DECOUTCLK minimum period	100	–	ns
tdoutl	DECOUTCLK low period	40	–	ns
tdouth	DECOUTCLK high period	40	–	ns
tdrf	DECOUTCLK rise to DECCLKOUT fall*	0	22	ns
tdfr	DECOUTCLK fall to DECCLKOUT rise*	0	22	ns

NOTE
*Value assumes a 25 pF load on the output pin.

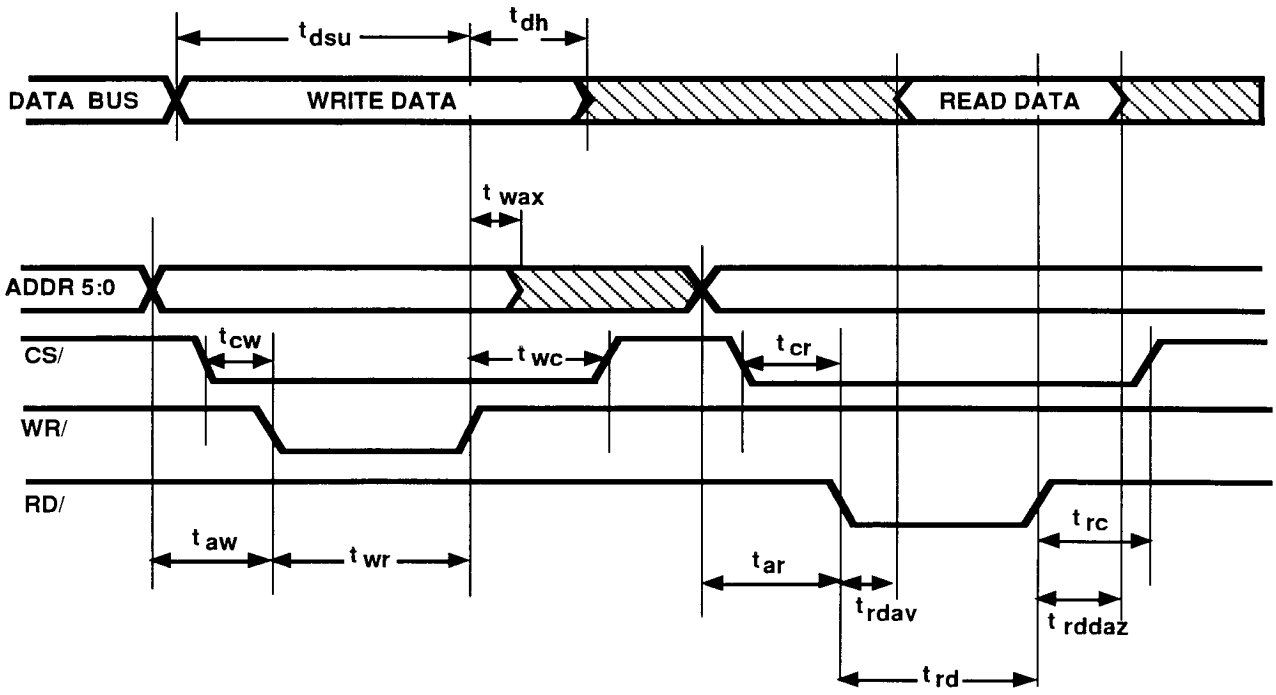
Decoder Data Output Timing



		Q1601C-10N		
Signal	**Description**	**Min**	**Max**	**Units**
t_{decpd}	Data valid after output clock rising	1	18	ns

NOTES
1. Value assumes a 25 pF load on the output data pin.
2. Output data includes R0ERR, R1ERR, DECDATOUT, INSYNC, OUTOFSYNC, and BERDONE.

Processor Interface Timing



Write Signal	Description	Q1601C-10N Min	Max	Units
t_{dsu}	Data setup to WR/ rising	20	–	ns
t_{dh}	Data hold after WR/ rising	5	–	ns
t_{cw}	CS/ falling to WR/ falling	15	–	ns
t_{wax}	Address hold after WR/ rising	5	–	ns
t_{wc}	CS/ hold after WR/ rising	5	–	ns
t_{aw}	Address valid to WR/ falling	20	–	ns
t_{wr}	WR/ period	80	–	ns

Read Signal	Description	Q1601C-10N Min	Max	Units
t_{ar}	Address valid to RD/ falling	20	–	ns
t_{rd}	RD/ period	80	–	ns
t_{cr}	CS/ falling to RD/ falling	15	–	ns
t_{rc}	CS/ hold after RD/ rising	5	–	ns
t_{rdav}	RD/ falling to DATA valid	–	60	ns
t_{rddaz}	Data hold after RD/ rising	0	–	ns

Q1601C-10N PLCC Packaging

The Q1601C-10N device is packaged in a 68-pin plastic leaded chip carrier (PLCC) (figure 12). A suggested socket is AMP P/N 821574-1 (through-hole board mounted) or P/N 822070-4 (surface mounted). Dimensions are given in inches (mm).

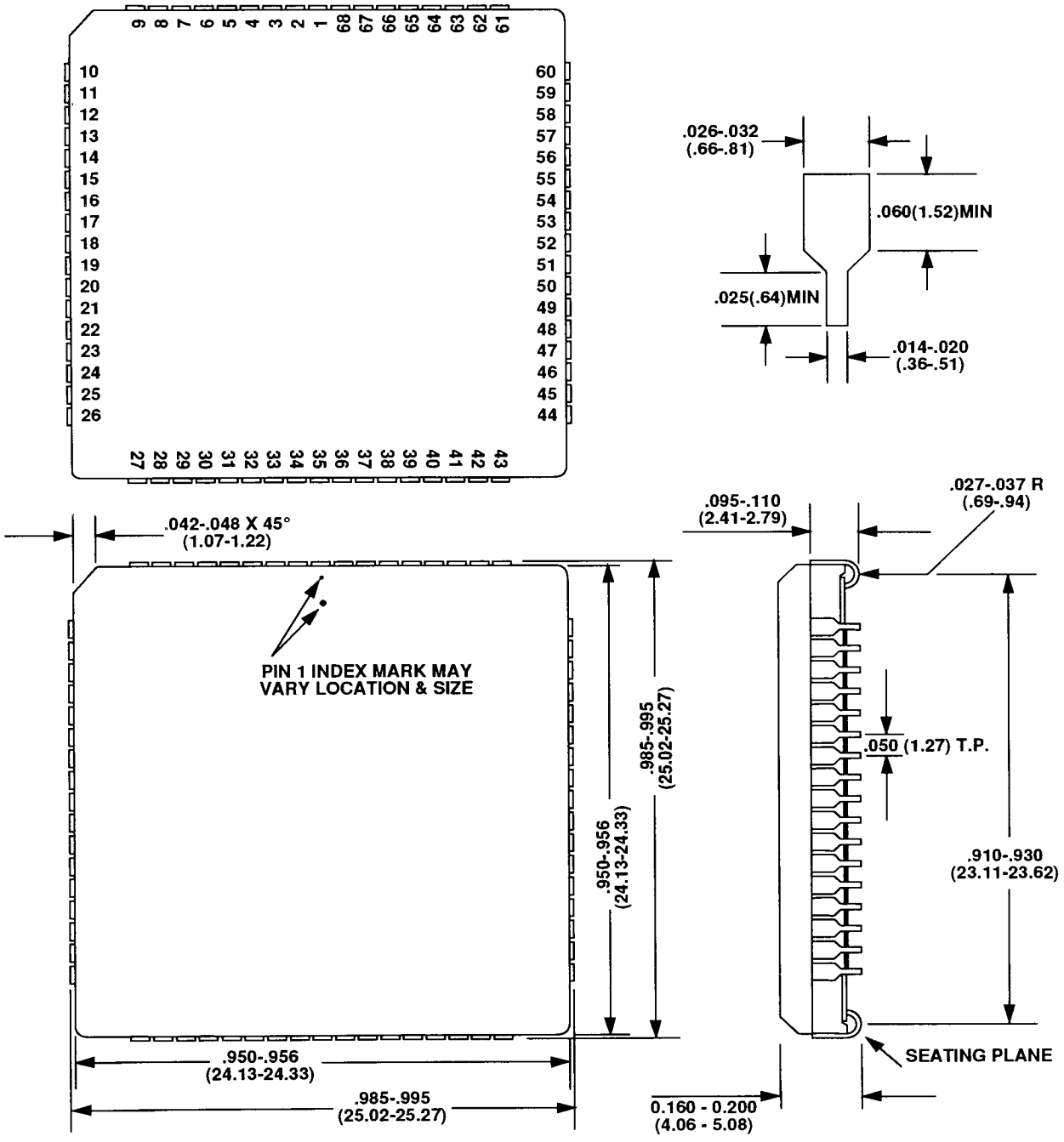


Figure 12. PLCC Packaging

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Viterbi Decoding Theory

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G. C. Clark, Jr. and J. B. Cain, *Error Correction Coding for Digital Communications*, Plenum Press, New York, NY, 1981

G. D. Forney, Jr., "The Viterbi Algorithm," *IEEE Trans. Information Theory*, Vol. IT-15, pp. 177-179.

A. J. Viterbi, "Convolutional Codes and Their Performance in Communication Systems," *IEEE Trans. Communication Technology*, Vol. COM-19, 1971, pp. 751-772.

Data Scrambling Algorithm

CCITT Recommendation *Data Transmission at 48 Kilobits per Second Using 60-108 KHZ group Band Circuits*, Fascicle VIII.1, Rec. V.35, Appx. I

Related Application Notes

AN1650-1, "Data Scrambling Algorithms Implemented in the Q1650 Viterbi Decoder."

AN1650-2, "Setting Soft-Decision Thresholds for Viterbi Decoder Code Words from PSK Modems."

AN1650-4, "Using the Q1650/Q0256 Viterbi Decoders with Externally Provided Branch Metrics."

TB0256-1, "Successful Integration of QUALCOMM VLSI Products into INMARSAT."

S. Morley, "Forward Error Correction Applied to INTELSAT IDR Carriers," *International Journal of Satellite Communications*, VOL. 6, 1988, pp. 445-454.

GLOSSARY

AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keyed
CMOS	Complementary Metallic Oxide Semiconductor
dB	Decibel
DBS	Direct Broadcast System
FEC	Forward Error Correction
k	Convolutional Code Constraint Length
Mbps	Million Bits Per Second; refers to the encoder data input rate and the decoder data output rate
OQPSK	Offset Quartenary Phase Shift Keyed
PLCC	Plastic Leaded Chip Carrier
QPSK	Quartenary Phase Shift Keyed
VSAT	Very Small Aperture Terminal
R0, R1	Decoder input bits or code word
G0, G1	Generating function of the convolutional encoder, described as an octal number

ORDERING INFORMATION

Maximum Data Rate	Plastic Package (PLCC)	Special Packages	MIL883C Screened Version
10 Mbps	Q1601C-10N	Contact QUALCOMM	Contact QUALCOMM

For more information or to place an order, contact your local QUALCOMM Engineering Representative or contact QUALCOMM directly:

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